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Modeling and simulation of power MOSFETs based on 4H-SiC

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Dedication

This work is for you, Dad. As good men you embodied the role of the ideal father in so many ways: in personality, love of family, devotion to the work, and passion for your children. You were well-loved everywhere you served. As you look down from heaven, I hope you're proud of your little boy.

Hichem Bencherif

Abstract

Exploring the attractive electrical properties of the Silicon Carbide (SiC) for power devices, the analysis of 4H-SiC MOSFETs is the main topic of this Ph.D document. In particular, the thesis concerns the investigation using numerical and analytical, physics based models, for accurately replicating the power MOSFET behavior.

At the present, the fabrication of SiC devices with the given performances is not completely obvious. This fact is due to the lack of knowledge still existing in parameters related to SiO_2/4H-SiC interfacial region and the sensitivity of some physical parameters to temperature changes. Therefore, a set of investigative tools, designed especially for SiC devices, cannot be regarded as secondary objective. Following this need, in our research activity firstly predictive, numerical and analytical models, including temperature dependence, are used. This models able to explain the carrier transport in diffused regions and turns also useful for better understanding the influence of physical parameters, which depend in a significant way from the processed material, on device performances. These models are then assumed as objective functions in MOGA to determine the optimized physical and geometrical device parameters for a specific application. The models include also the device characterization at high temperatures to analyze the influence of thermal issues on the overall behavior up to temperature of 250°C. Secondly, with the aim to properly account for a realistic device, a combined model of both defect energy levels inside the 4H-SiC bandgap (deep and tail centers) and oxide-fixed traps has been incorporated in a more general, self-consistent model, allowing the analysis of the device behavior under the temperature and carrier-trapping effects.

Finally, with the imposition of right physical models, it is possible to use the versatility of the 2D Silvaco tool for extending the analysis and obtaining a physical insight on the

effect of a non-uniform p-base doping concentration and the high K materials properties in determining the fundamental 4H-SiC MOSFET figure of merits, both in blocking and forward current regime (i.e. blocking voltage, threshold voltage, channel mobility, drain current, and on-state resistance).

Résumé

Explorant les propriétés électriques attrayantes du carbure de silicium (SiC) pour les dispositifs de puissance, l'analyse des MOSFETs à base de 4H-SiC est le sujet principal de ce document de doctorat. La thèse concerne en particulier la recherche utilisant des modèles numériques et analytiques, pour reproduire avec précision le comportement du MOSFET de puissance.

À l'heure actuelle, la fabrication de dispositifs en SiC avec les performances données n'est pas tout à fait évidente en raison du manque de connaissances concernant les effets des paramètres physiques et géométriques sur les performances du dispositif, en particulier de ceux liés à la région interfaciale SiO2 / 4H-SiC et la sensibilité de certains paramètres physiques aux changements de température. Par conséquent, un ensemble de simulateur conçus spécialement pour l'investigation des dispositifs SiC, ne peut être considéré comme un objectif secondaire. Pour répondre à ce besoin, notre activité de recherche utilise d'abord des modèles prédictifs, numériques et analytiques, y compris la dépendance à la température. Ces modèles capables d'expliquer le transport des porteurs s'avèrent également utiles pour mieux comprendre l'influence des paramètres physiques, qui dépendent de manière significative du matériau traité, sur les performances du dispositif. Ces modèles sont ensuite supposés être des fonctions objectives dans MOGA pour déterminer les paramètres optimisés des dispositifs physiques et géométriques pour une application spécifique. Les modèles incluent également la caractérisation du composant à haute température pour analyser l'influence des problèmes thermiques sur le comportement global jusqu'à une température de 250 ° C. En outre, dans le but de rendre compte correctement d'un dispositif réaliste, un modèle combiné des niveaux d'énergie des défauts à l'intérieur de la bande interdite 4H-SiC (centres profonds et de la queue) et des pièges fixés à l'oxyde a

été intégré, permettant l'analyse du comportement du dispositif sous les effets de la température et des défauts.

Enfin, avec l'imposition de modèles physiques appropriés, il est possible d'utiliser la polyvalence de l'outil 2D Silvaco pour étendre l'analyse et obtenir un aperçu physique de l'effet de la concentration non uniforme de la région p-base et des propriétés de matériaux à K élevé pour déterminer le facteur de mérite fondamental du MOSFET 4H-SiC, (c'est-à-dire tension de blocage, tension de seuil, mobilité de canal, courant de drain et résistance à l'état passant).

ملخص

باستكشاف الخصائص الكهربائية المميزة لكربيد السيليكون (SiC) المستعمل في صناعة عناصر الاستطاعة ، يعتبر تحليل مقحل الاستطاعة الاحادي القطبية 4H-SiC MOSFETs هو الموضوع الرئيسي لأطروحة الدكتوراه. على وجه الخصوص، تتعلق الأطروحة بالبحث المنهجي باستخدام النماذج العددية والتحليلية لتحليل سلوك مقحل الاستطاعة بدقة.

حاليا ،تصنيع مقاحل الاستطاعة باستخدام كاربيد السيليكون بأداء مميز ليس واضحًا تمامًا بسبب نقص المعلومات حول تأثير الخصائص المادية والهندسية على أداءه ، وخاصة تلك المتعلقة بالمنطقة البينية SiO2 / 4H-SiC و حساسية بعض الخصائص لتغيرات درجة الحرارة. لذلك لا يمكن اعتبار التحقيق في هذه التاثيرات على مقحل الاستطاعة هدفًا ثانويًا. بالنظرالى هذه الحاجة ، في نشاطنا البحثي يتم أولاً استخدام نماذج تنبؤية وعددية تحليلية ، بما في ذلك الاعتماد على تاثير درجة الحرارة. هذه النماذج قادرة على شرح عملية النقل وتتحول أيضًا إلى فهم أفضل لتأثير الخصائص المادية على أداء المقحل. ثم يتم افتراض هذه النماذج كوظائف موضوعية في مقاربة التحسين MOGA لتحديد خصائص المقحل المادية والهندسية المثلى لتطبيق معين. تشمل النماذج أيضًا محاكاة للمقحل في درجات حرارة عالية لتحليل تأثير المشكلات الحرارية على السلوك الكلي حتى درجة حرارة 250 درجة مئوية. ثانياً ، بهدف تحليل مقحل واقعي بشكل صحيح ، تم دمج نموذج موحد لمستويات الطاقة المعيبة (مراكز العمق والذيل) والفخاخ الثابتة بالأكسيد في نموذج عام أكثر اتساقًا ذاتيًا ، مما يسمح بتحليل سلوك الجهاز تحت تأثير درجة الحرارة.

أخيرًا ، مع فرض النماذج الصحيحة ، تم استغلال تعدد استخدامات 2D Silvaco لتوسيع التحليل والحصول على رؤية مادية حول تأثير تركيز الاشابة غير المنتظمة في القاعدة p وخصائص المواد عالية النفاذية K في تحديد مزايا المقحل (على سبيل المثال ، توتر الانهيار ، توتر العتبة ، الحركية في القناة والمقاومة).

Contents

General Introduction

During the last decade, use of 4H silicon carbide (4H-SiC)-based metal–oxide–semiconductor field-effect transistors (MOSFETs) for high-power, high temperature, and switching applications has been widely proposed.[1–5] Thanks to its outstanding physical and electronic properties (i.e., mechanical strength, thermal conductivity, and critical electric field) [6,7] silicon carbide has been recognized world wide as a promising material to improve device performance in terms of ON-state resistance, breakdown voltage, and switching capabilities. In particular, SiC MOSFETs are widely used as power devices in on board DC–DC converters for use in specific modules; For example, in Ref. [8], a boost based converter was proposed, describing the design of a zero-voltage zero-current switch (ZVZCS) suitable for high duty cycle and wide load currents; in Ref. [9], dual-SiC MOSFET modules were designed for use in the electric traction context; in Ref. [10], a dual active bridge (DAB) converter was implemented using 10-kV SiC MOSFETs; in Ref. [11] a high-frequency, 1-kW, 800 V output voltage boost DC–DC converter was developed. To meet the specific constraints related to modern power electronics, the design of 4H-SiC MOSFETs requires deployment of intensive modeling effort based in turn on numerical, analytical, and empirical calculations, carefully taking into account the different geometrical and physical parameters that affect device performance.[12–15].

Thesis outline

The aim of the work is to investigate, by means of a careful numerical simulation study, the electrical characteristics of a 4H-SiC MOSFET designed for low voltage ratings (150 V) over a wide range of temperatures. Without loss of generality with respect to different designs dimensioned for higher blocking voltages, explicit interface trap effects

due to a detailed density of states in the inversion region and to a fixed trap density in the oxide are considered referring to literature data. Preliminary results at room temperature and neglecting defect and trap effects were presented in [16, 17] in order to emphasize, as stated previously, the use of fast and rugged 100-V-class switches. The obtained results clarify the role of the interface traps in reducing the carrier mobility in the channel region.

In the first chapter, we will present the state of the art of power MOS transistors with both vertical and lateral structures. The theoretical limit, called the "limit of silicon", the calculated specific on state resistance as a function of the breakdown voltage will be given in each case.

The second chapter describes the fundamental physical models taken into account during the simulations of the investigated 4H-SiC MOSFET and their reference parameters.

The third chapter will be devoted to the investigation of an optimized design of a 4H-SiC dual implanted MOSFET (DMOSFET) well suited for a specific application by means of a multiobjective genetic algorithm (MOGA). In more detail, starting from combined analytical and numerical analysis of the device current–voltage (ID–VDS) characteristic, both analytical and numerical models are used as objective functions in MOGA to determine fundamental design parameters that minimize the ON-state resistance of a device dimensioned for a blocking voltage (BVDS) in the range from 150 V to 800 V.

The fourth chapter will be devoted to the investigation, by means of a careful numerical simulation study, the electrical characteristics of a 4H-SiC MOSFET designed for low voltage ratings (BVDS = 150 V) over a wide range of temperatures. Without loss of generality with respect to different designs dimensioned for higher blocking voltages,

explicit interface trap effects due to a detailed density of states in the inversion region and a fixed trap density in the oxide are considered referring to literature data.

In chapter 5, after a short overview on the High-K material physics, a comparative evaluation of the gate deielectrics effect on the 4H-SiC MOSFET performances is carried out. This study is focused on the impact of thickness and fixed charge density. For this purpose, 2-D numerical simulations using a commercial two- dimensional (2D) technology computer-aided design (TCAD) physical simulator that provides the solution of Poisson's equation and carrier continuity equations is performed.

We will conclude this manuscript by presenting some perspectives concerning the electrical modeling study of the 4H-SiC power MOSFET (Super Junction, Trench MOSFET,..).

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CHAPTER 1:

State of the Art of Power MOSFET Devices

Chapter1

State of the Art of Power MOSFET Devices

I.1. Introduction

In power electronics, bipolar transistors and thyristors were the first controllable power devices used in several power applications. However, these bipolar devices are not suitable for switching applications high frequency and require a complex control circuit providing non-energy negligible. The evolution of technologies in the field of MOS integrated circuits has allowed the development of families of power MOS transistors able to operate in high Frequency with simplified control through a grid insulated by a thin oxide. The conventional structure silicon power MOS transistor is a unipolar device which is widely used in high frequency switching power applications for breakdown voltages not exceeding 250 volts. The current in the power MOS transistor is a conduction current of a single type of carriers (the majority), there is therefore no evacuation delay due to the stored charge or to the recombination of the minority carriers as in the case of bipolar devices. Consequently, the switching speed of the power MOS transistors is much greater than that of the bipolar transistors. this property that makes the power MOS transistor the preferred device for high frequency switching applications.

The power MOS transistor consists of a multitude of elementary cells in parallel to allow the device to switch very large currents. Unlike bipolar transistors, paralleling MOS cells. Elementary is possible thanks to the coefficient of positive thermal drift of the on-state resistance of these cells. Therefore, the direct current distribution remains homogeneous between the constituent cells of the power MOS transistor. With respect to the power MOS technology, the power MOS transistor is fabricated using the P and N^+ type planar dual diffusion process to realize the channel base P and N^+ source areas. Moreover, the name of these DMOS transistors is drawn directly from this double diffusion process, that is to say carrying out a P and N^+ double diffusion through the same window using the polysilicon gate as the masking edge . This technique of self-

alignment of these diffusions makes it possible to adjust and control the length of the channel of the DMOS transistor to submicron dimensions.

For the first commercially available MOS power transistors, the power semiconductor manufacturers proposed several geometrical configurations of the source P cells of the transistor. The aim was to find the geometric shape of the source P scatter that allowed for the highest density of integration - the Z / S ratio of the perimeter to the surface of the chip - and hence the largest current per unit surface [1], [2]. For the same widths and depths of the source P diffusions, Hu [1] has demonstrated that the optimum resistances, representing the different zones of the passage of the current in the on state in the VDMOS structure, obtained by these different geometrical shapes are approximately the same if the ratios between the surface of the diffusion P and the surface of the cell are identical. On the other hand, technological progress has been made enabling the integration density to be increased by reducing the size of the constituent elementary cells of the power MOS transistor. There may be mentioned for example: the trench MOS transistor, also called UMOS [3] and the Motorola High Speed TMOS (HDTMOS) transistor [4].

In this chapter, we will discuss the main features of different power DMOS structures in the case of integrated and discrete devices. Specifically, we will give the so-called silicon limit that connects the breakdown voltage to the specific pass resistance, which is the product of the resistance in the on state by the active surface of the component, power DMOS transistors. Finally, given the technological progress made in the process of obtaining substrates made of wide-band gap semiconductor materials with better performances at very high temperatures, it seemed useful to recall here the impact of the use of these new materials on the compromise "specific pass resistance / breakdown voltage" of vertical power MOS transistors.

I.2. Power MOS device structures and operating principle

There are two types of power DMOS transistors: discrete transistors (vertical structures) and integrated transistors (lateral structures in general). LDMOS lateral structures (lateral DMOS) are used for low power radio frequency voltages applications [5].

I.2.1. Power MOS devices

I.2.1.1. VDMOS transistor

Figure I.1 shows an elementary cell of the VDMOS transistor. This transistor is manufactured using the MOS dual diffusion process. The source and the gate are located on the surface of the chip while the drain is at the back of the chip. In the on state, the gate-source voltage V_{gs} is greater than the threshold voltage V_T and an *N*-type inversion channel is thus formed on the surface of the zone of the channel allowing the flow of current between the drain and the source. This current passes, in large part, in the volume of the structure through the *N*- drift zone. Part of this current goes to the surface in the channel and depends on the mobility of the electrons in the inverted layer. The inversion channel resistance is an additional limitation in the case of low voltage VDMOS transistors and is also important in the case of new power MOS made from silicon carbide because of the low mobility in the inverted layer. [6].

The N-drift zone assures the VDMOS transistor the ability to block the voltage in the off state. For a well optimized VDMOS structure [7, 8], the breakdown voltage depends on the doping and the thickness of the drift zone. In fact, to block very high voltages, the drift zone must be weakly doped and sufficiently wide to allow the space charge zone to expand. As a result, this wide and weakly doped zone becomes, in the on state, a very great resistance which can only be reduced by increasing the active surface of the device or by using new concepts such as the concept of superjunction by example. The use of high energy ionization materials can also to be a very good solution to this problem. There is therefore a compromise between the on-state resistance and the breakdown voltage of the VDMOS power transistors.

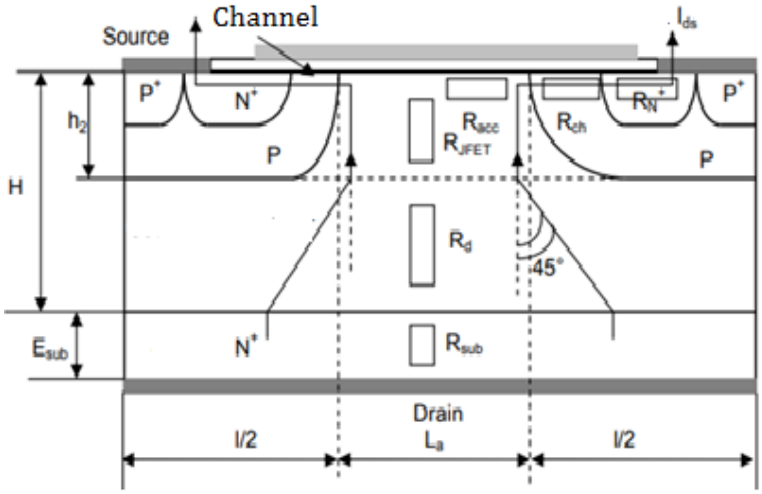

Figure I.1: Schematic section of a cell of the VDMOS transistor [8].

It may also be noted that the gate electrode here acts as a field plate and reduces the electric field at the surface of the "P-body / N-drift" junction. This is not without consequence because this gate electrode spread over the entire intercellular surface between the P source diffusions introducing a parasitic MOS capacitance between the gate and the drain. This capacitance, known as the Miller capacitance, causes a feedback between the output and input of the device and significantly reduces the transistor's transition frequency. To remedy this problem, it is possible for example to remove a portion of the grid [8, 9] above the epitaxial layer N-. In this case, a significant increase in the transition frequency of the transistor can be obtained. However, this elimination of a part of the gate causes a reduction in the breakdown voltage of the device, because of the strong electric field at the end of the gate metallization, and an increase in on state resistance because the length of the accumulated area is reduced. On the other hand, the equivalent resistance of the VDMOS transistor is composed of several resistors in series: channel resistance, accumulated resistance at the surface of the drift zone between the adjacent source P diffusions, JFET resistance of the region between the adjacent source P diffusions, resistance of the N-drift volume region, substrate resistance and contact resistances. The resistive effect of the JFET zone between the source P diffusions is all the greater as the doping of the epitaxial zone is weak, in the case of transistors intended to operate at high voltages, or if the distance between the source diffusions P is very weak. It is this last phenomenon, increasing the JFET resistance by decreasing the intercellular distance, which limits the integration density of power MOS devices

I.2.1.2. The trench MOS transistor

One solution to the problem of increasing the JFET resistance, limiting the integration density of the VDMOS structure, is the innovative structure, called the trench MOS structure, proposed by Ueda et al [10].to eliminate the JFET area and increase the integration density of the MOS elementary cells. This structure is widely used in the case of MOS low-voltage power transistors to reduce the on-resistance of the device and, therefore, increase the autonomy of nomadic systems of low power.

Figure I.2 shows a schematic section of the trench power MOS transistor. This structure is also called UMOS because of the U-shape of the buried grid under the source metallization. This structure makes it possible to increase the perimeter of the channel and to reduce the part of the N-drift zone under the source P diffusion which does not contribute to the passage of the current to the on state (problem of defocusing of the current lines, Figure I.1). Thus, the resistance of low voltage trench MOS transistors is very small, compared with VDMOS transistors of conventional structure with the same breakdown voltage.

The manufacturing technology of this type of transistor comes directly from the technology R.I.E (Reactive Ion Etching) [11] used in the manufacturing process of the memories DRAM.

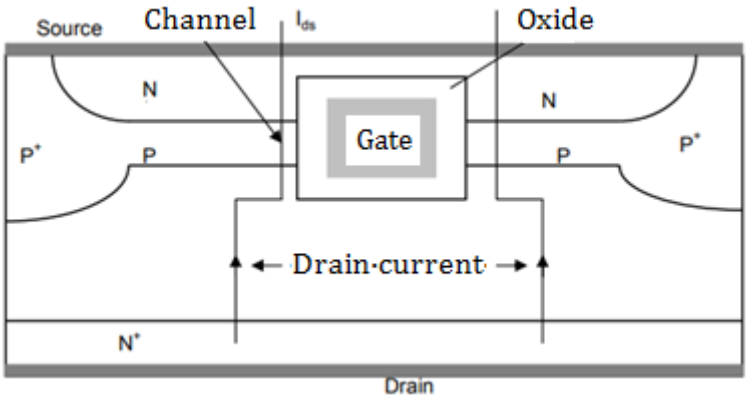

Figure I.2: Schematic section of a cell of the trench MOS transistor [10].

The trench MOS transistor has a vertical configuration and current flows through the volume along the inverting channel which is now vertical. As in the case of the VDMOS transistor, the trench MOS transistor has a N-lightly doped zone to support the off-state voltage and is constituted by the paralleling of several MOS cells ensuring the passage of a strong current. in the passing state. At the level of the dynamic performances, one can notice that there is no improvement at the level of the Miller grid-drain capacity because of the part of grid, above the drain, buried under the diffusion P source. For the two types of vertical transistors mentioned here, there is no current limitation and it is possible, a priori, to set up as many elementary MOS cells in parallel to ensure the passage of the desired current in the on state. With regard to the breakdown voltage, there is no fundamental limitation, but the resistive effect of the drift zone, broad and

weakly doped in the case of high voltage MOS, can cause conductive losses which can cause the destruction of the power transistor.

I.2.2. Integrated devices

The advantage of these coplanar structures is that they can be integrated with the processing part of the analog or digital signal for the development of the system on a chip (System-on-Chip: SoC). The advantage of this integration lies in the elimination of parasitic elements due to the connecting wires in the discrete circuits, suppression of interface circuits between the power and the control and the reduction of the weight and the cost of the power electronic function performed on a chip. The most known technologies are: '' SmartMOS '' used by Freescale and ST Microelectronics. The most used integrated device is LDMOS because it is able to operate at very high frequencies [5] and because its three electrodes are at the surface, which facilitates its integration.

I.2.2.1. LDMOS transistor

Figure I.3 shows a schematic section of the conventional LDMOS transistor. The breakdown voltage is limited in this structure at voltages of the order of 250 volts. Indeed, the breakdown in this structure usually occurs at the end of the gate metallization (because of the small thickness of the gate oxide) or at the PN-cylindrical junction. It depends mainly on the doping of the drift zone and the distance Ld between the end of the gate metallization and the beginning of the opening of the drain diffusion [12, 13].

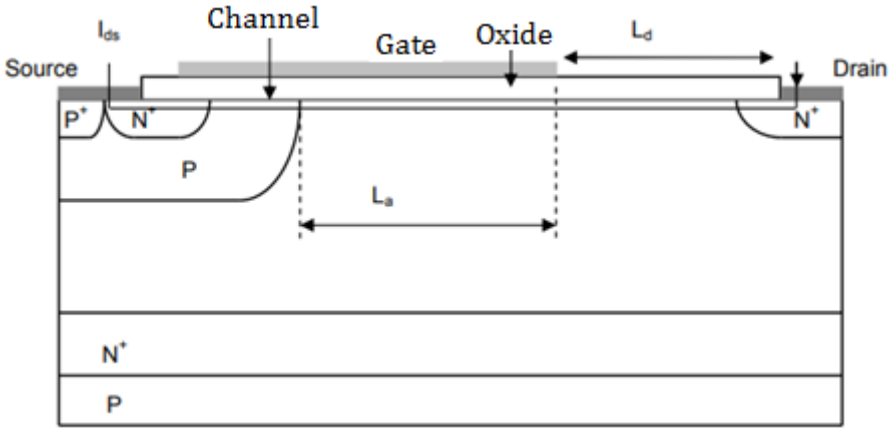

Figure I.3: Schematic section of a conventional LDMOS transistor [8].

In addition, the presence of the three electrodes on the upper face of the chip does not facilitate the densification of the cells in parallel to form the power LDMOS transistor. The source and the drain are most often in the form of interdigitated parallel bands. The buried layer N + makes it possible to limit the extension of the space charge area in the region N- and to avoid the piercing of the substrate P. It can also make it possible to cancel the gain of the parasitic transistor PNP between the substrate and the source P diffusion of the power MOS transistor. The electric current passes on the surface of the structure and depends on the distance Ld; this distance is also called the length of the drift zone. The lower the distance, the weaker the resistance of the component. Unfortunately, the breakdown voltage decreases as Ld decreases and it has been demonstrated by two-dimensional numerical simulations [13] that there is an optimum drift distance providing a maximum breakdown voltage for a given drift doping. This therefore limits the integration density because the choice of the drift distance, which is on the surface of the structure, will be imposed by the compromise between the breakdown voltage and the specific passing resistance. Thanks to a very low Miller capacity compared to the vertical structure, the LDMOS is the device of choice for radio frequency applications [14].Many variants of the structure of the LDMOS transistor have been proposed to improve its breakdown voltage; we can cite for example:

a) LOCOS LDMOS transistor (LOCal Oxidation in Silicon): in this structure, the electric field at the end of the gate metallization is greatly reduced by local oxidation of the silicon. The major problem of this structure is the degradation of the current passing surface in the on state and, therefore, a significant increase in specific pass resistance compared to that of conventional LDMOS structures.
b) The LDMOS Resurf (Reduced Surface Field) (Figure I.4): this structure is obtained by replacing N-epitaxy on substrate N + by an N- epitaxial layer on a P- substrate.

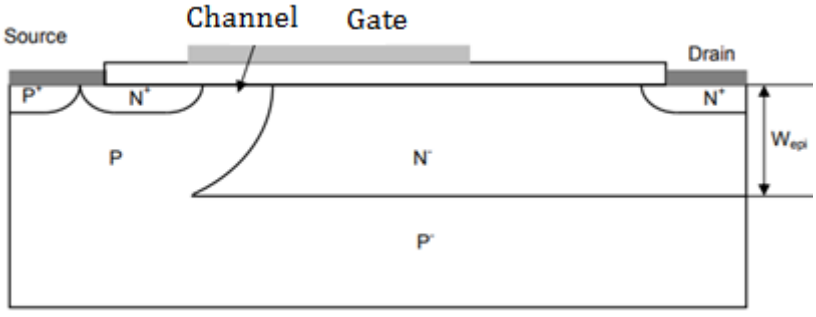

Figure I.4: Schematic section of a Resurf LDMOS transistor [8].

The substrate P^- must be connected to the source, through the source P diffusion, so that the plane diode thus formed is polarized in reverse and supports, under certain conditions, the drain source voltage. If the Resurf structure is well designed, the N- zone must be completely depleted before the surface area has a point where the field reaches the critical breakdown field. If, in addition, the distance between the source and the N^+ drain diffusion is such that the drilling of the N + drain zone is effective, the breakdown can take place at the plane junction NP - thus making it possible to significantly improve the voltage of breakdown compared to the classic LDMOS structure. Another advantage of this structure is that the resistance in the on state remains identical to that of the conventional LDMOS structure while the breakdown voltage is significantly improved. This technique has allowed monolithic power ICs to exceed 250 Volts breakdown voltages.

I.2.2.2. The VDMOS transistor up-drain

The structure of the VDMOS up-drain transistor (Figure I.5) resembles the structure of the vertical NPN bipolar transistor with the drain acting as the collector. This solution has been proposed to solve the problems of insulation appearing between two VDMOS manufactured on the same plate. In this structure, the current passes, in large part, between the drain and the source vertically. The buried layer N + serves to collect the electrons and drain them to the drain on the surface of the chip through the well N + of the drain. Unfortunately, this too long electron path increases the on-state resistance of this type of power MOS transistor and, therefore, the conduction losses of the component.

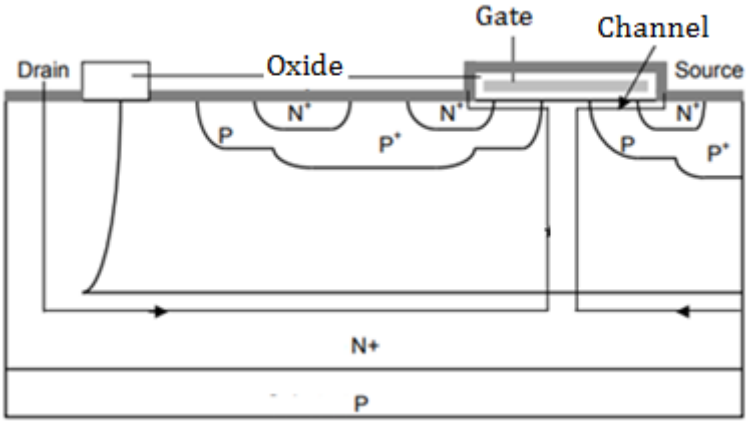

Figure I.5: Schematic section of an up-drain VDMOS transistor [8].

I.2.2.3. LUDMOS transistor

In order to improve the breakdown voltage of lateral MOS structures, M. Zitouni [13] proposed an LDMOS structure integrating an oxide trench in the drift zone at the end of gate metallization. This structure (figure I.6), called LUDMOS, makes it possible to reduce the electric field on the surface. Zitouni then proposed, trying to reduce the specific pass resistance, several variants [13] of this structure by eliminating the distance between the trench and the drain (structure 2), then filling the trench with the gate polysilicon (structure 3).) and, finally, by overdoping the surface of the drift zone (structure 4).

Despite the path length of the current flow, this structure makes it possible to obtain a better compromise between the specific on resistance and the breakdown voltage compared to a conventional DMOS structure with the same breakdown voltage. Using two-dimensional simulations, it has been shown [13] that for a breakdown voltage of 60 volts, the specific pass resistance is only 0.6 mΩ.cm 2 against 1.57 mΩ.cm 2 for a conventional 60 V LDMOS structure, a reduction of more than 60%.

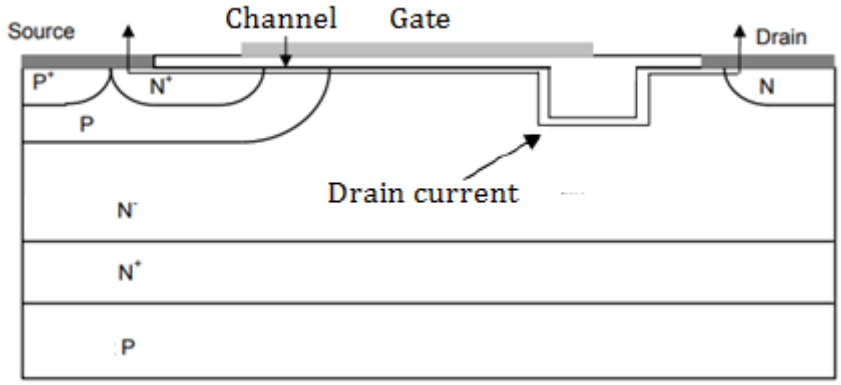

Figure I.6: Schematic section of a LUDMOS transistor [13].

I.3. Static and dynamic characteristics of power VDMOS transistor

As in the case of the other silicon power structures, the power MOS transistor must integrate in its structure a weakly doped zone, N- in the case of the N-channel VDMOS transistor, to support the voltage in the off state. The breakdown voltage depends on the thickness and doping level of this N-drift zone.

In this paragraph, we will focus on the study of the breakdown voltage, called the first breakdown voltage, equivalent to the maximum drain-source voltage Vds for a gate-

source voltage Vgs zero. The transistor is in the off state and no current flows between the drain and the source. Because doping of the source P diffusion is greater than doping of the N-drift zone, the depletion zone extends mainly in the weakly doped N - drift zone. If the structure is well designed [7, 8], we can consider that the breakdown takes place at the plane junction "P-body / N- drift '. In this case, we can assimilate the structure of the transistor VDMOS with a reverse biased PN^-N^+ diode.

I.3.1. Breakdown voltage

In the off state and for a zero V_{gs} voltage, the drain voltage cannot evolve beyond a maximum voltage known as the first breakdown voltage. At the approach of this limit, the breakdown occurs by avalanche and the drain current increases inconsiderately.

The breakdown of the VDMOS structure has multiple origins -figure I.7-: 1) lateral zones where the effects of curvatures of the junctions are predominant, 2) frontal zones where the extension of the space charge can be or not be limited, 3) surface areas of the lightly doped region covered with gate oxide and 4) the oxide itself. These problems have been largely addressed by [7]. Several junction guarding techniques are used to avoid premature breakdown of the structure by attempting to minimize the surface effects and to lengthen the radius of curvature of the junctions, inevitable in the case of diffusions, to try to reach the theoretical breakdown. of the planar junction [7, 15, 16].It should be noted that the gate electrode spread over the entire intercellular surface also reduces the field to the surface of the structure. In addition, by a judicious choice of the intercellular distance, self-shielding can be obtained to protect the gate oxide [7, 8].In practice, junction guarding techniques are used to allow the structure to hold up to 90% of the breakdown voltage of the plane junction [7].

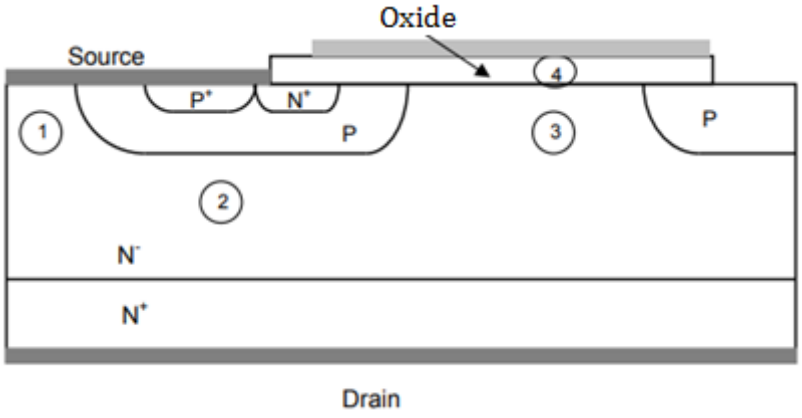

Figure I.7: Breakdown zones of a VDMOS structure [7].

For a well-designed VDMOS structure, it can therefore be considered that the breakdown takes place in the volume of the structure at the plane junction "P-body / N-drift". This breakdown voltage depends on the thickness and the doping of the drift zone. For an inverse polarized one-dimensional PN diode, the breakdown conditions are governed by the avalanche multiplication mechanism. It is considered that these conditions are satisfied when the ionization integral (I_n or I_p) is equal to unity, ie:

$$I_n = \int_0^W \alpha_n \exp\left(\int_W^X (\alpha_n - \alpha_p)dx'\right)dx \tag{I.1}$$

$$I_p = \int_0^W \alpha_p \exp\left(\int_0^X (\alpha_n - \alpha_p)dx'\right)dx \tag{I.2}$$

where α_n and α_p are respectively the ionization coefficients of electrons and holes. These coefficients α_n and α_p represent the probable number of ionizing collisions experienced by an incident carrier, hole or electron, per unit of path length. According to Sze [17], these two equations are strictly equivalent as regards the determination of breakdown voltages; one or the other of them can be used indifferently because they reach unity for the same tension. For the VDMOS transistor that interests us, and using a two-dimensional simulation software such as ATLAS (SILVACO tool), the breakdown voltage is determined by calculating the ionization integral from the α_n coefficients. and α_p whose values are different, depending on the model chosen.

For the analytical calculation, one of the major problems is that of the formulation of the ionization coefficients. Indeed, these coefficients are expressed as a function of the electric field in the following form:

$$\alpha_i = \alpha_i^{\infty} \exp\left(-\frac{E_i^{crit}}{|E|}\right)_{i=n,p} \tag{I.3}$$

To facilitate this task, Mac Kay [18] has shown that the ionization coefficients can be approximated by simpler functions which are polynomial expressions of the type:

$$\alpha_n\left(cm^{-1}\right) = A'.E^7 \tag{I.4}$$

$$\alpha_p\left(cm^{-1}\right) = A''.E^7 \tag{I.5}$$

where A' and A" are two constants whose values have been proposed respectively by:

$$A' = A'' = A = 1{,}8.10^{-35} \tag{I.6}$$

$$A' = 3{,}6.10^{-35} \tag{I.7}$$

$$A'' = 0{,}3.10^{-35} \tag{I.8}$$

Note that the proposed values for A' and A'' by Fulop are identical. On the other hand, Gharbi proposes two different values for A' and A'' Other authors have proposed different values but we will retain the values proposed by Gharbi because they represent an average for these proposed values.

There are two cases before the breakdown of the PN-N^+ diode :

1) case of the infinite junction in non-limiting or non-piercing (NPT): in this case, the space charge area is less than the thickness of the N- zone and the shape of the electric field is triangular -figure I.8-:

2) Punch-through case (PT): The space charge area is greater than the thickness of the N- zone and the shape of the electric field can be considered as' 'trapezoidal' -Figure I.9-.

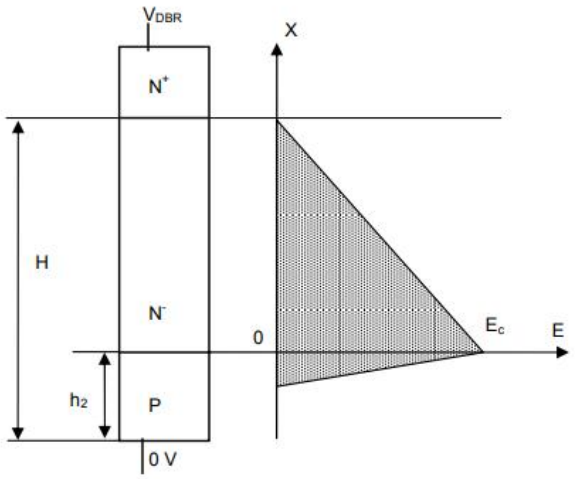

Figure I.8: Case of the infinite junction with "No Punch Through" (NPT) limitation [8].

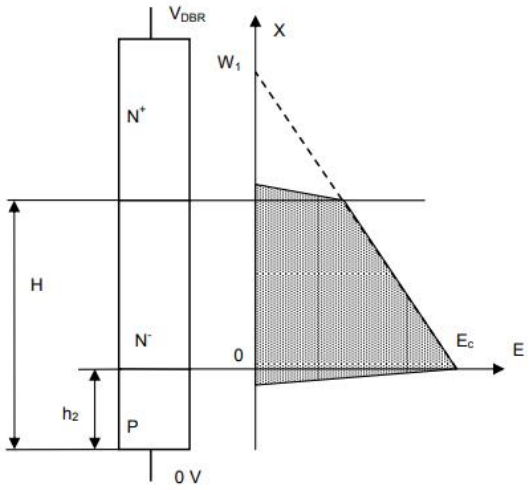

Figure I.9: Case of limit junction or "Punch Through" (PT) drilling [8].

I.3.1.1. Case of an infinite plane junction in non-limitation '' No Punch Through ''

In the hypothesis of an abrupt flat P^+ N dissymmetrical junction, the integration of the Poisson equation makes it possible to determine the expression of the electric field:

$$E(x) = \frac{q.N_d}{\varepsilon_n.\varepsilon_{si}}\left[x - (H - h_2)\right] \tag{I.9}$$

(H-h_2) is, in this case, considered to be the maximum extension of the space charge area (SCA) of an infinite plane junction -figure I.8-

Based on equations (I.4), (I.5) and (I.9), the calculation of the ionization integral using equation (I.1) or (I. 2) makes it possible to express the breakdown condition of the PN junction as a function of the parameters of the structure:

$$\ln\left(\frac{A'}{A''}\right) = \frac{A' - A''}{8}.\left(\frac{q.N_d}{\varepsilon_0.\varepsilon_{si}}\right)^7.(H - h_2) \tag{I.10}$$

On the other hand, the maximum extension (H-h_2) of the space charge of the abrupt plane NP junction, that is to say at the moment of breakdown, is given by [17]:

$$(H - h_2) = \left(\frac{2.\varepsilon_0.\varepsilon_{si}}{q.N_d}.V_{DBR}\right)^{\frac{1}{2}} \tag{I.11}$$

By combining the expressions (I.10) and (I.11), the extension of the maximum space charge (H-h_2) is thus obtained as a function of the breakdown voltage V_{DBR}:

$$(H - h_2) = \left[16.\frac{A' - A''}{\ln\left(\frac{A'}{A''}\right)} \right]^{\frac{1}{6}} .(V_{DBR})^{\frac{7}{6}} \tag{I.12}$$

Then the breakdown voltage V_{DBR} as a function of the N_d doping:

$$V_{DBR} = \left[\frac{1}{2.(A' - A'')} . \left(\frac{\varepsilon_0 . \varepsilon_{si}}{q.} \right)^3 . \ln\left(\frac{A'}{A''}\right) \right]^{\frac{1}{4}} (.N_d)^{-\frac{3}{4}} \tag{I.13}$$

Using the values of A 'and A' 'proposed by Gharbi, we can calculate the expressions of the breakdown voltage and the maximum extension of the space charge as a function of the doping for an infinite plane junction with no limitation of the space charge area:

$$V_{DBR}(Volts) = 5{,}72.10^{13}.N_d^{-\frac{3}{4}} \tag{I.14}$$

$$W(cm) = H - h_2 = 2{,}7.10^{10}.N_d^{-\frac{7}{8}} \tag{I.15}$$

I.3.1.2. Case of a plane junction in '' Punch Through '' limitation

Given relations (I.4) and (I.5), the integral (I.2) can be written as:

$$I_p = \int_0^W A''.E^7 . \exp\left[-\int_0^x (A'' - A').E^7 dx' \right] dx \tag{I.16}$$

W is the space charge extension, in this case it is equal to (H-h_2), according to figure I.9. The electric field E is obtained by the one-dimensional integration of the Poisson equation and is written in the form:

$$E(x) = \frac{q.N_d}{\varepsilon_0 . \varepsilon_{SI}} .(W_1 - x) \tag{I.17}$$

W_1 is the maximum extension of the space charge defined in Figure I.9 in the case of a plane junction with no limitation.

Since the integral (I.16) is equal to unity, its resolution leads to the following breakdown criterion:

$$W_1^8 - \left[W_1 - \left(H - h_2\right)\right]^8 = \frac{8.\left(\varepsilon_0.\varepsilon_{si}\right)^7}{\left(A' - A''\right).\left(q.N_d\right)^7}.\ln\left(\frac{A'}{A''}\right) \tag{I.18}$$

For convenience of writing, we assume:

$$W' = H - h_2 \cdots et \cdots C = \frac{8.\left(\varepsilon_0.\varepsilon_{si}\right)^7}{\left(A' - A''\right).\left(q.N_d\right)^7}\ln\left(\frac{A'}{A''}\right) \tag{I.19}$$

Equation (I.18) can then be written as:

$$W_1^8 - \left(W_1 - W'\right)^8 = C \tag{I.20}$$

The expression (I.20) does not admit a "direct" analytical solution. To solve it, we use the following iterative procedure:

At first order: for $W_1 = W'$ we get the solution:

$$W_1\Big|^1 = C^{\frac{1}{8}} \tag{I.21}$$

Second order: replace the first solution in equation (I.20), which gives:

$$W_1\Big|^2 = \left[C + \left(C^{\frac{1}{8}} - W'\right)^8\right]^{\frac{1}{8}} \tag{I.22}$$

In the third order, replace the second relation in equation (I.20). We obtain as follows:

$$W_1\Big|^3 = \left\{C + \left[\left[C + \left(C^{\frac{1}{8}} - W'\right)^8\right]^{\frac{1}{8}} - W'\right]^8\right\}^{\frac{1}{8}} \tag{I.23}$$

Which gives order n the following solution:

$$W_1\Big|^{n+1} = \left[C + \left(W_1\Big|^n - W'\right)^8\right]^{\frac{1}{8}} \tag{I.24}$$

To study the influence of this method of resolution on the resistance in tension, we calculate the curves of the resistance in tension as a function of the doping and this for several values of the thickness of epitaxial. The one-dimensional resolution of the Poisson equation leads to the following expression:

$$V_{DBR} = \frac{q.N_d}{\varepsilon_0.\varepsilon_{si}}.\frac{H-h_2}{2}.\left[2.W_1 - (H-h_2)\right] \quad \text{(I.25)}$$

figure I.10 shows the characteristics of the breakdown voltage as a function of doping and epitaxial thickness (H-h_2) in the case of the planar junction in limitation. The curves plotted for n = 1 have maxima whose existence is related to the approximation made on the order of the solution. When the order n increases, the curves have a horizontal asymptote which is the limit solution (n -> ∞), which can also be calculated analytically by extending the term of the Nd doping towards zero:

$$V_{DBR} = \left[\frac{1}{A'-A''}\ln\left(\frac{A'}{A''}\right)\right]^{\frac{1}{7}}.H^{\frac{6}{7}} \quad \text{(I.26)}$$

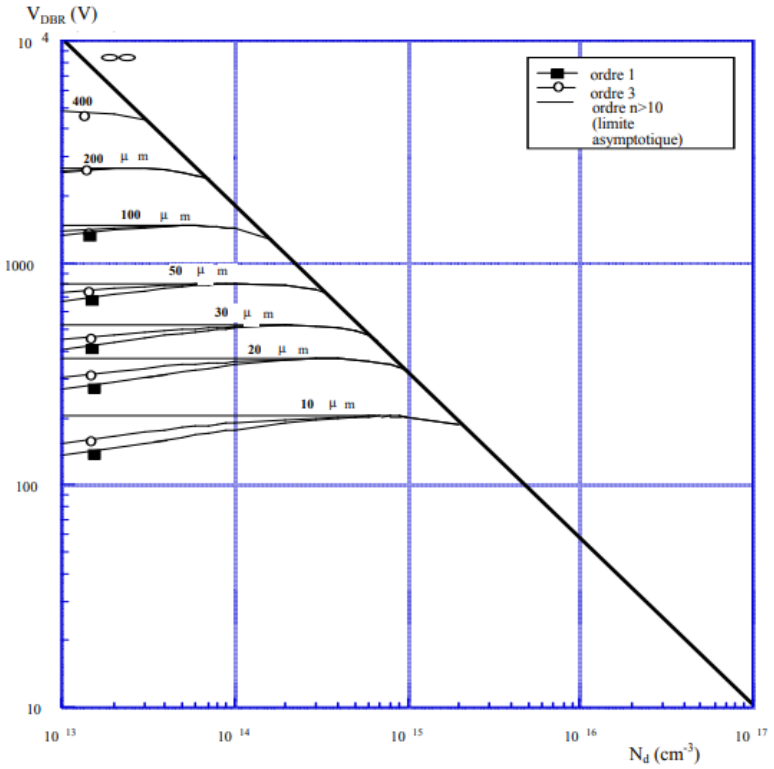

Figure I.10: Breakdown voltage of the PN-N + junction "Punch Through" limitation [8].

The thickness of the N-epitaxial zone in the case of the limiting structure (PT) will be smaller than that in the case of non-limitation (NPT). Therefore, the on-state resistance will be lower in the case of depletion region limitation than in the case of non-limitation. In the case of IGBTs, there are two PT and NPT structures on the market. PT IGBTs have reduced conduction losses while NPT structures are faster with low switching losses.

New IGBT structures have emerged in recent years to try to combine the advantages of both PT and NPT structures (LPT: Light PT for Mitsubishi and SPT: Soft PT for ABB for example).

I.3.2. On state resistance

The on-state resistance of the power MOS transistor is defined as the total resistance that occurs between the source and the drain as the transistor drives in a linear, low-drain-source voltage regime. Its value can be calculated by determining the ratio:

$$R_{on} = \left.\frac{V_{ds}}{I_{ds}}\right|_{V_{ds}\to 0} \tag{I.27}$$

In practice, its value is given for a grid voltage of 10 volts.

This resistance (figure I.1) is equivalent to the sum of several resistors in series: the resistance of the source N^+ diffusion, the resistance of the channel, the accumulated resistance in surface of the intercellular zone under the gate, the resistance JFET of the zone drifting between the adjacent source P diffusions, the drift resistance, the substrate resistance, the metallization resistors and the resistances of the electrical connection wires to the housing. For high-voltage VDMOS devices, the drift resistance represents more than 90% of the component's on-state resistance. On the other hand, in the case of low voltage VDMOS transistors, the substrate resistance is not negligible and the channel resistance and the access resistance (accumulated resistance + JFET resistance) become comparable to the drift resistance.

I.3.2.1. Channel Resistance

The resistance of the channel is calculated by determining the ratio:

$$R_{ch} = \left.\frac{V_{ch}}{I_{ds}}\right|_{V_{ch}\to 0} \tag{I.28}$$

where V_{ch} is the voltage between the drain and the source at the terminals of the inversion channel and Ids is the drain current [20].

In the hypothesis of uniform doping in the channel, the expression of the resistance of the channel can be given by:

$$R_{ch} = \left(\mu_0 . C_{ox} . \psi . \frac{Z}{L} \right)^{-1} . \frac{V_{gs}' + \psi - 2.\phi_F}{V_{gs} - V_T} \quad \text{(I.29)}$$

where μ_0 is the low electric field mobility, C_{ox} is the oxide capacity, ψ is the transverse reduction potential of the mobility, V_{gs} 'is the effective gate voltage ($V_{gs}' = V_{gs} + Q_{ss} / C_{ox}$-$\varphi_{ms}$), V_T is the threshold voltage of the transistor and Φ_F is the Fermi potential. Z is the perimeter of the channel and L is the length of the channel. According to this expression, we can see the advantage of increasing the perimeter of the channel in the case of MOS structures of low voltage where the resistance of the channel is not negligible.

I.3.2.2. Accumulation resistance

The access Ra of a power MOS transistor is the equivalent resistance of two resistors in series: the resistance of the layer accumulated at the surface in the intercellular zone (R_{acc}) and the resistance JFET (R_{JFET}) between the diffusions P source adjacent.
Several authors have proposed formulas for calculating this resistance [8, 21, 22].

The expression of the access resistance can be written as [8]:

$$R_a = k \frac{L_a}{2.\mu_{0acc}.C_{ox}.A} . \frac{\left(V_{gs}' + \mathrm{A} - 2.\phi_F \right)}{\left(V_{gs} - V_T \right)} + \rho_D . \frac{h_2}{Z.\left(L_a - 2W_0 \right)} \quad \text{(I.30)}$$

where L_a is the length of the accumulated zone, h_2 is the depth of the source P diffusion and W_0 is the extension of the space charge area in the N-drift JFET zone. μ_{0acc} is the low field mobility in the accumulated layer,
Λ is the mobility reduction potential in the accumulated layer [22] and ρ_D is the resistivity of the N^- drift zone. K is a corrective factor that takes into account the two-dimensional nature of the passage of the channel current to the drift zone through the JFET pinch zone.
In the expression (I.30), the first term is equivalent to the resistance of the accumulated zone, while the second term corresponds to the resistance of the JFET region.
T.P. Pham [21] and J-L. Sanchez [22] proposed a calculation method based on a distributed diagram of the access zone in vertical and horizontal directions. In this case, the expression of the access resistance Ra can be given by:

$$R_a = \frac{2.h_2}{q.\mu_n.N_d.Z.L_a}.\lambda' \quad \text{(I.31)}$$

μ_n is the mobility in the volume of the drift zone N^- and λ 'is a parameter which depends on the gate-source voltage V_{gs}, the doping of the drift zone N^-, the depth of the source diffusions P and the mobility.

I.3.2.3. Drift resistance

It is the resistance of the layer that supports the voltage in the off state. As a first approximation, it can be considered that the current passes uniformly in this zone and the drift resistance is equivalent to an ideal drift resistance which can be calculated according to the conventional relation of a semiconductor bar:

$$R_d = \frac{H - h_2}{q.\mu_n.N_d.S}. \quad \text{(I.32)}$$

where S is the surface of the elementary cell

The two-dimensional nature of the defocusing phenomenon of the current lines in the volume of the material does not allow an analytical approach adapted to the study of all the cases of surface geometry and thickness of the epitaxial layer. Considering the defocusing of current lines under source P scattering at a 45 ° angle (Figure I.1), B. J. Baliga [8] proposed the following expression:

$$R_a = \frac{1}{q.\mu_n.N_d.Z}.\ln\left(\frac{(L_a - W_0) + (H - h_2)}{L_a - W_0}\right) \quad \text{(I.33)}$$

There are other analytic expressions for calculating this resistance according to several elementary cell geometries. In our case, we will use the formula (I.33) which gives a good approximation of the drift resistance of the FLIMOS transistor. The current in the drift zone passes largely in the region under the grid (figure I.1) thus creating an unused zone under the source P scattering [23]. Thanks to the technological progress of densification of the elementary cells of the MOS transistor, this unused area has been greatly reduced and, consequently, the specific pass resistance of the power MOS device has been improved [23]. More recently, innovative structures, based on the concept of super junction and the concept of floating islands, have allowed a significant improvement in drift resistance. The drift resistance depends mainly on the doping and

the thickness of the drift zone which fixes the breakdown voltage of the component. It is therefore also possible to reduce this resistance by introducing broad bandgap semiconductor materials with high ionization energy. The higher this energy, the lower the drift resistance. This is one of the reasons why new materials with high ionization energy are being studied to develop MOS transistors of low resistance power in the on state and which can operate in addition to high temperature through their wide bandgap.

I.3.2.4. Other resistances

The other resistors of the VDMOS structure are: N^+ source scattering resistance, substrate resistance and contact resistances. The resistance of the N^+ source scattering is negligible in the face of other resistances because of high N^+ doping. On the other hand, the resistance of the substrate is not negligible in the case of low voltage transistors because the substrate must be sufficiently thick to allow the robustness of the wafer during the manufacturing steps of the component. The resistance of the substrate can be calculated using the formula for calculating the resistance of a Nsub semiconductor doping bar and thickness E_{sub}:

$$R_{sub} = \frac{E_{sub}}{q.\mu_{nsub}.N_{sub}.S} \tag{I.34}$$

In the case of small power MOS transistors intended for portable applications (breakdown voltage of the order of 30 volts), the connection resistances are no longer negligible in the face of the silicon resistors thanks to the new high power density MOS structures. integration such as trench MOS transistors for example. It is for this reason that several power device manufacturers have changed how to connect their chips, in the case of small power devices, in order to solve the various problems due to the standard housings used: connection resistance, parasitic inductance and thermal resistance.

I.3.3. Silicon limit of vertical DMOS transistors

In theory, it can be assumed that the on-state resistance of the power MOS transistor depends on the number of cells elementary elements in parallel constituting this component. This implies that by increasing the number of cells in parallel, the on-state

resistance of the power MOS transistor can be reduced. But this reduction will be accompanied by a chip surface too important. It is therefore the product ($R_{on.S}$) of the resistance in the active state by the active surface, called specific resistance-resistance or "specific on-resistance", which is the parameter the most important for power MOS devices. Considering that the on-state resistance is equivalent to the ideal drift resistance, ie neglecting the other resistances, the ideal specific pass resistance can be given by:

$$R_{on}.S = \frac{H - h_2}{q.\mu_n.N_d}. \qquad \text{(I.3)5}$$

The relation linking the mobility to the breakdown voltage can be given by [24]:

$$\mu_n\left(cm^2.V^{-1}.S^{-1}\right) = 7{,}1.10^2.V_{DBR}^{0,1} \qquad \text{(I.36)}$$

In the case of the limitation of the ECA, Gharbi [7] considered that the electrical breakdown field at the main junction remains equal to that of the non-limiting junction and expressed the "thickness-doping" torque of the drift zone according to the following relationships:

$$\left(H - h_2\right)(cm) = 1{,}87.10^{-6}.V_{DBR}^{\frac{7}{6}} \qquad \text{(I.37)}$$

$$N_d\left(cm^{-3}\right) = 1{,}85.10^{18}.V_{DBR}^{-\frac{4}{3}} \qquad \text{(I.38)}$$

We considered the case of the limitation which gives the smallest thickness of the epitaxial zone and thus the lowest resistance in the on state.

Using equations (I.35), (I.36), (I.37) and (I.38), we find:

$$R_{on}.S\left(\Omega.cm^2\right) = 8{,}9.10^{-9}.V_{DBR}^{2,4} \qquad \text{(I.39)}$$

This equation expresses for a vertical MOS component, or more generally for vertical unipolar power devices, the minimum resistance that cannot be exceeded for a given breakdown voltage.

B.J. Baliga gave [8] a formula different from equation (I.39), with a calculation based on non-uniform drift doping, in which the breakdown voltage is at power 2.5:

$$R_{on}.S\left(\Omega.cm^2\right) = 8{,}3.10^{-9}.V_{DBR}^{2,5} \qquad \text{(I.40)}$$

However, the values of the specific pass resistance calculated by formulas (I.39) and (I.40) are very close. As a result, we will use equation (I.39).

By protecting the main junction of the vertical DMOS structure, new structures have significantly reduced the drift resistance and, consequently, the specific pass resistance of the unipolar power devices. However, equation (I.39) is a very difficult limit to overcome or "break" in the case of VDMOS transistors of low voltage power because the drift resistance represents, in this case, only 30 to 40% of the total resistance of these conventional structures. On the other hand, this limit can be exceeded by new structures in the case of high voltage MOS devices because the drift resistance represents, in this case, more than 90% of the total resistance in the on state. Several research projects, on new silicon structures or new silicon substitution materials, have been conducted in recent years to try to approach or "break" this so-called silicon limit. Thus, new power MOS structures have been introduced; for example, superjunction structures [25] and floating-island structures [26, 27, 28, 29].

I.3.4. Silicon limit in DMOS transistors

The conventional LDMOS structure is intrinsically limited to breakdown voltages not exceeding 250 volts. To exceed this limit, the LDMOS Resurf structure is used in general. We will therefore retain this last structure to define the so-called silicon limit in the case of lateral DMOS structures. Fujihira [25] proposed an estimation of the silicon relation for conventional Resurf structures:

$$R_{on}.S\left(\Omega.cm^2\right) = 2{,}04.10^{-6}.W_{epi}^{\frac{5}{12}}.V_{DBR}^2 \qquad \text{(I.41)}$$

W_{epi} is the thickness of the epitaxial zone (Figure I.4). This thickness depends on the doping of the epitaxial zone to avoid a premature breakdown of the structure [25].

I.4. Wide band gap semiconductor materials for power electronics

I.4.1. Introduction

The need for new applications of power electronics, for example in hybrid vehicles, requires reliable, fast electronics, low conduction and switching losses and can operate at very high temperatures. Silicon, currently the most used microelectronic material, can not meet these requirements because of these physical and thermal characteristics that limit its use in many power applications and in particular in automotive electronics. It is therefore to new semiconductor materials with a wide bandgap that research has focused in recent years to meet the requirements mentioned above. Indeed, several research projects are currently being conducted to promote broad bandgap semiconductor materials that can improve the static and dynamic performance of power devices. It is well known that, due to the thermal agitation in the crystal lattice of a semiconductor material, the height of the band gap decreases as the temperature increases and, therefore, this material can become conductive at high temperature. The choice of wide bandgap semiconductor materials is therefore the solution to have an electronics capable of continuing to operate at high temperature. In addition, the critical field of breakdown of the semiconductor material is related to the height of the forbidden band. The higher the height of the band gap, the greater the critical field of breakdown. Therefore, these large bandgap semiconductor materials will be very interesting for power electronics applications because to maintain high voltages in the off state, the operation of the drift zone will be greatly improved and the thickness of this zone will be very thin. In this case, the drift resistance will no longer be a handicap for high voltage (> 250 Volts) MOS devices in wide bandgap semiconductor materials. It can also be noted that the resistance of the connection wires and the resistance of the channel will no longer be negligible for breakdown voltages below 1 kV because of the sharp reduction in drift resistance.

Among the promising silicon substitution materials in high temperature power applications are silicon carbide (SiC), gallium nitride (GaN) and diamond. In the case of silicon carbide power MOS devices, for example [6], [30], the low mobility in the inversion layer remains one of the major problems to be solved for high voltage MOS

devices. It has been shown [30] that the channel resistance can represent 44% of the on-state resistance whereas the drift resistance only represents 17% of this resistance for a silicon carbide power MOS transistor 660 volts. This experiment shows the need for a new definition of the material limit in the case of unipolar devices made from wide bandgap semiconductors because the drift resistance no longer represents the important device up to the voltages of the order of 10 kV.

In practice, Schottky diodes made of silicon carbide are marketed for breakdown voltages exceeding 500 volts with a high current in the on state. For example, the company Infineon offers Schottky diodes 600 volts silicon carbide with a maximum current in the passing state of 100 amps (characteristics of this diode can be found on the website of the company: device under reference IDT02S60C).The electron saturation velocity of wide-bandgap semiconductor materials is much greater than that of silicon and, therefore, it is possible that the devices made from these materials are capable of operating at high frequencies. In addition, the stored load and the recovery time will be considerably reduced thanks to the small thickness of the drift zone.

A last important parameter for these silicon substitution materials is the thermal conductivity. The higher the thermal conductivity, the lower the thermal resistance and, therefore, the material can easily transmit heat to the outside. This allows a slow increase in temperature in the power device. Table I.1 gives the main physical characteristics of broad bandgap semiconductor materials. There are two types of silicon carbide substrates: 4HSiC and 6H-SiC. Prior to the introduction of 4H-SiC in 1994, the only available silicon carbide substrate was 6H-SiC. These two materials have similar properties except the mobility of electrons which is in the case of isotropic 4H-SiC and greater than the anisotropic mobility of electrons in the case of 6H-SiC.

According to Table I.1, diamond is the reference semiconductor material due to its high critical breakdown field, higher electron mobility than other materials and the highest thermal conductivity. Gallium Nitride has the lowest thermal conductivity, compared to other semiconductor materials, including silicon, but it can be very interesting for optoelectronic power applications thanks to its direct gap and its critical field of breakdown 6 times higher than critical field of silicon.

Table I.1: Key characteristics of SiC vs. other semiconductor materials [8].

	Si	*GaAs*	*4H-SiC*	*GaN*	*Diamond*
$E_{g@300K}$ (ev)	1.1	1.4	3.2	3.4	5.45
E_C (MV/cm)	0.3	0.4	2.2	2	10
V_{sat} (×10^7 cm/s)	1.0	2.0	2	2.5	2.7
$\mu_{n@N=10^{16}\,cm^{-3}}$ (cm^2/VS)	1500	8500	720	1000	2200
$\mu_{p@N=10^{16}\,cm^{-3}}$ (cm^2/VS)	480	400	120	30	850
ε_r	11.9	13.1	9.7	8.9	5.5
λ (W/cm K)	1.5	0.5	5	1.3	22

I.4.2. Compromise "specific On resistance / breakdown voltage"

For a PN-junction, the breakdown voltage depends on the critical field of breakdown of the semiconductor material used:

$$V_{DBR}(Volts) = \frac{\varepsilon_0.\varepsilon_r.E_c^2}{2.q.N_d} \tag{I.42}$$

where ε_0 (F/cm) and ε_r represent the permittivity of the vacuum and the semiconductor material used respectively, q the elementary charge of the Coulomb electron, N_d the doping of the N-zone in cm^{-3} and E_c the critical field of breakdown in V/cm.

The ideal specific passing resistance of drift in the on state can be given by the following relation [25]:

$$R_{on}.S(\Omega.cm^2) = \frac{27.V_{DBR}^2}{8.\varepsilon_0.\varepsilon_r.E_c^3.\mu_n} \tag{I.43}$$

μ_n being the mobility of the electrons of the material used in $cm^2V^{-1}.s^{-1}$.

Figure I.11 shows the specific pass resistance, calculated from Equation (I.43), of the main broad bandgap semiconductor materials as a function of breakdown voltage.

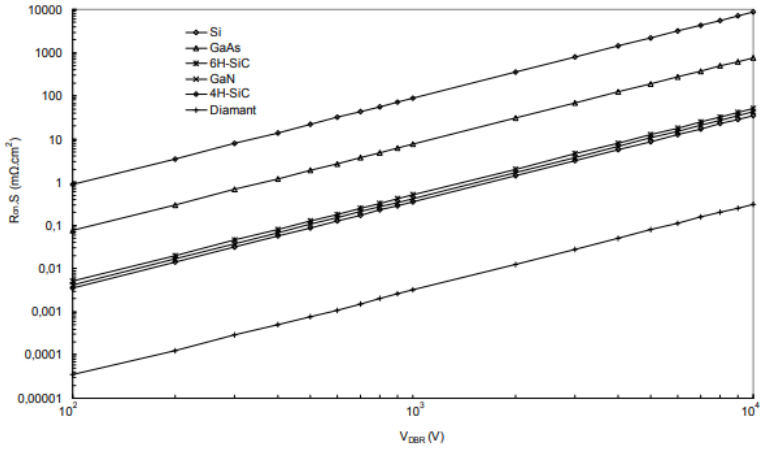

Figure I.11: Limits of silicon, 4H-SiC and broad bandgap materials [3].

In conclusion, here are some advantages and disadvantages of the 4H-SiC broadband semiconductor material:

Silicon carbide: thanks to a more advanced technology compared to other broad bandgap semiconductor materials, silicon carbide devices are currently marketed. Most recently, Cree Research Foundation, the leading supplier of silicon carbide wafers, offers 1200 volt silicon carbide Schottky diodes with a current of 50 amperes (www.cree.com). Other studies are under way toto reduce micro-defects in silicon carbide substrates and to improve reverse layer mobility in the case of power MOS transistors made from this material.

I.4.3. SiC MOSFETs

The development of Vertical Power MOSFETs in SiC has been, and still is, a crucial element in the development strategy of the various players in the sector. Indeed, the silicon carbide Mosfets have the triple advantage of being normally blocked (in English Normally-off), easy to control and perfectly adapted to the power ranges required for consumer electronics, robotics or transport. It is thus naturally towards these structures of transistors that the efforts of the industrialists are mainly carried, which made it possible to appear from 2011 the first Mosfets Sic commercial.

I.4.3.1. The different structures

The development of these devices has been marked by numerous changes in the geometry of these structures. We will try, here, to quickly recall the milestones of this story but also to describe what could be the future of these commercial devices.

The first silicon carbide power MOSFETs appeared in 1994 [31]. At that time, the developed devices had Vertical Trench Grid (UMOSFET) structures, as shown in Figure 1.12. The most obvious interest of this structure is that it allows the formation of the source and base zones by epitaxial and not by ion implantation, which makes it possible to overcome the annealing associated with high temperature which can degrade certain states of area.

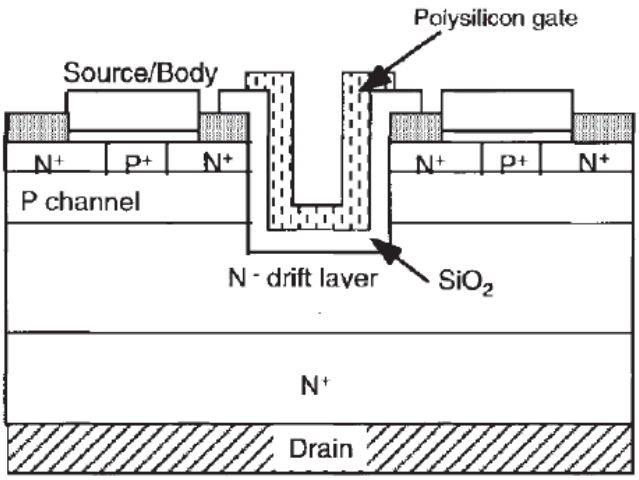

FIGURE I.12 - Schematic sectional view of a vertical SiC MOSFET structure with a trench gate [3].

However, the first developments of trench gate structure have shown a strong limitation of the voltage withstand of these devices. Indeed, the presence of a large electric field at the corners of the trench is likely to cause localized breakdown of the gate oxide. Therefore, the first generations of UMOSFET developed in the early 1990s were limited to a voltage withstand of 260 V [32].

A simpler solution to overcome the phenomenon of breakdown of the oxide at the corners of the trench has been to remove the trench gate structure itself. It is for this reason that appear, as early as 1996, the first MOSFETs of so-called planar grid power. Figure 1.13 shows a schematic sectional view of a planar-gate SiC MOSFET or DMOSFET. This structure takes its name from the double ion implantation necessary for the creation of the p and n + doped channel and source zones. This new MOSFET structure has significantly increased the voltage resistance in the off state. At the time, the calibres in voltage could thus be multiplied by a factor of about three passing from the UMOSFET structure to the DMOSFET structure and reach 760 V [33].

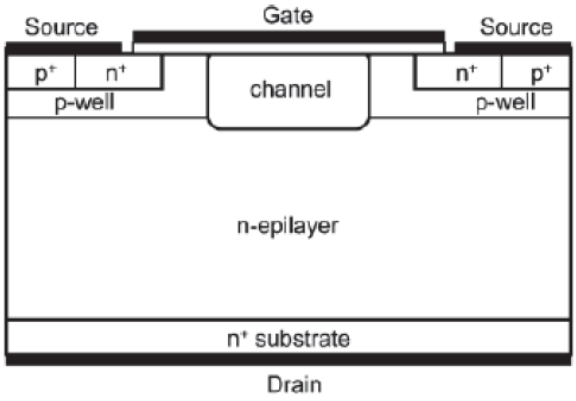

FIGURE I.13 - Schematic sectional view of a double planar "planar" MOSFET structure [33].

For silicon carbide, the use of the diffusion technique is impossible. It is therefore necessary to form the source region by ion implantation followed by activation annealing at a temperature between 1600 and 1700°C.

The implementation of this doping technique has consequences on the surface state of the semiconductor and therefore on the quality of the conduction channel. The weakness of carrier mobility in the SiC DMOSFET channel has led to many studies aimed at understanding the causes [34, 35] and solving this problem [36,37].Between the end of the 90s and the beginning of the 2000s, work was also carried out, by various groups, to improve the voltage resistance [38-40]. Structures able to support up to 10 kV have been proposed [41, 42]. All these efforts allowed the arrival on the market in 2011 of SiC MOSFET in the range of 600 / 1200V able to conduct a current up to 60A [43].

At the same time, any hope of developing UMOSFET devices capable of blocking high voltage levels has not been abandoned. Indeed, as early as 1998, Purdue University [44]

proposed a trench gate structure associated with an ion-implanted p-doped area under the bottom of the trench as shown in Figure 1.14. This structure, known as the Bottom p-tell (BPW), is grounded and thus protects the oxide from a too strong electric field in the off state. This trench MOSFET gate oxide protection technique continues to be the focus of research by Mitsubishi Electric Corporation [45, 46].

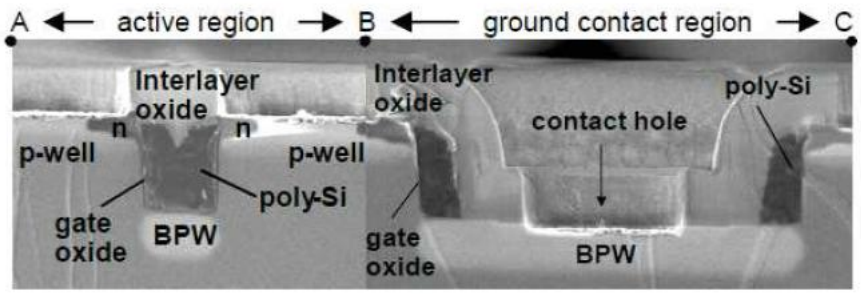

FIGURE I.14 - Scanning Electron Microscopy Image (SEM) of a 4H-SiC UMOSFET with a "BPW" zone reduced to the size [46]

This desire to develop this type of device is justified by the possibility of obtaining a higher density of elementary cells than for a DMOSFET structure. In addition, contrary to the planar MOSFET, the trenched devices do not have a JFET zone, which therefore makes it possible to obtain specific resistances (R (on, sp)) lower than for the DMOSFETs. Finally, the UMOSFET devices differ from the DMOSFETs by a better mobility of the carriers in the channel. Indeed, the channel of UMOSFET structures is formed on the side of the trench. The MOS interface is therefore carried out in the <1100> or <1120> planes of the crystal and not on the <0001> face as for the flat-plate structures. However, a certain number of studies tend to show a better mobility of the carriers in the plane <1120> [47].

More recently, the company ROHM presented a solution that consists in developing a so-called double-trench structure, in which the grid and the source zone are made by trench structures as presented in Figure 1.15. The simulation results presented below show a reduction of the electric field under the oxide and the appearance of a higher electric field under the trench source zones [47, 48]. This new structure is presented by the company ROHM being the basis of the 3rd generation of silicon carbide power MOSFET, available on the market in 2015.

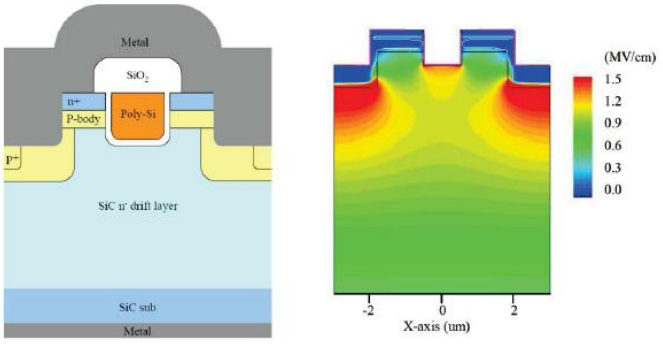

FIGURE I.15 - (a) Schematic sectional view of a double-trenched 4H-SiC MOSFET (b) electric field in the structure for VDS = 600 V and VGS = 0 V [48].

I.4.3.2. Gate-Source capacitance C_{gs}

Figure I.16 shows a schematic section of a cell of the FLIMOS structure with the location of the different capacities of this structure. The gate-source capacity C_{gs} is composed of three parallel capacities: I) the capacitance C_{gs1} for covering the gate oxide on the source N^+ diffusion, II) the capacitance C_{gsb} between the gate polysilicon and the channel area, III) the capacitance C_{gs2} between the source metallization and the gate polysilicon. As a first approximation, one can consider these capacities constant. Thus, the calculation of these different abilities can be performed using the general formula of the ability of a plane capacitor $C = (\varepsilon.S) / e$ and taking into account the geometrical shape of the cell elementary of the structure.

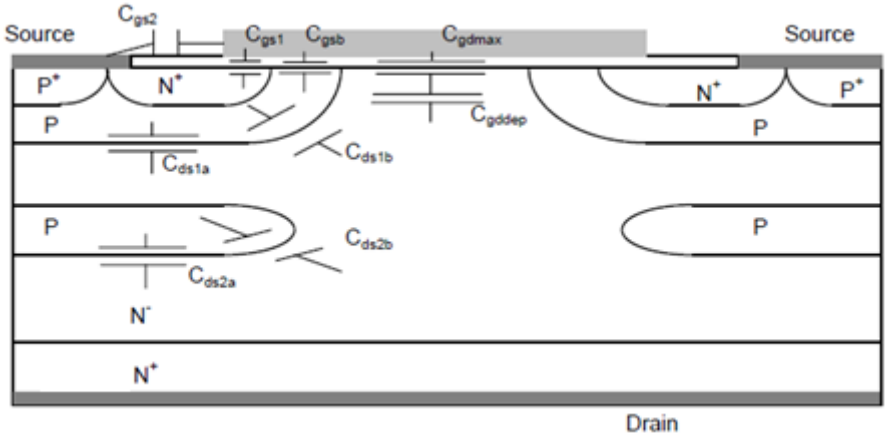

Figure I.16: Schematic section of a vertical FLIMOS cell and location of different inter-electrode capabilities of this structure [47].

I.4.3.3. Drain-source capacitance C_{ds}

The drain-source capacity consists of two capacities: the drain-source capacity of the main junction and the capacity of the "P-island / N-drift" junction. This last capacity intervenes only for drain voltages greater than the island's piercing voltage floating. Indeed, if the space charge area of the main junction does not break the island floating (Vds <Vper), the island's potential is not involved in the modulation of the ECA. The island piercing voltage depends on the distance d between the main junction and the floating island and the doping level of the drift zone; its value can be calculated using the relation(II.4).

For drain voltages below the island's piercing voltage, drain-source capacity is therefore equivalent to the capacity of the main junction. This ability is similar to the drain-source capacity of the conventional VDMOS structure. Its value can be calculated in the recital equals the sum of two capacities (parallel capacities): the capacity of the plane junction (Cds1a) and the capacity of the cylindrical junction (C_{ds1b}) (Figure II.16): $C_{ds1} = C_{ds1a} + C_{ds1b}$.The capacity of the C_{ds1a} plane junction can be calculated using the expression of the capacitance transition of a plane junction:

$$C_{dsla} = S_p . \sqrt{\frac{q.N_d.\varepsilon_0.\varepsilon_{si}}{2.V_{ds}}} \tag{I.44}$$

where S_p is the surface of the main drain-source plane junction. Concerning the cylindrical capacity Cds1b of the drain-source junction, Sze and Lee [14] have proposed a numerical calculation based on the use of charts to determine the value of this ability. Based on the values provided by these two authors, G. Tardivo [15]proposed, with an approximation of less than 10%, two analytical expressions for calculate this capacity:

$$C_{dsla} = \pi.\varepsilon_0.\varepsilon_{si}.Z.\left(\frac{V_{ac}}{V_{ds}}\right)^{0.426} \quad si \cdots V_{ds} \leq V_{ac} \tag{I.45}$$

$$C_{dsla} = \pi.\varepsilon_0.\varepsilon_{si}.Z.\left(\frac{V_{ac}}{V_{ds}}\right)^{0.306} \quad si \cdots V_{ds} \succ V_{ac} \tag{I.46}$$

$$V_{ac} = \frac{q.N_d.r_j^2}{4.\varepsilon_0.\varepsilon_{si}}$$

where r_j is the radius of curvature of the junction

For drain voltages greater than the floating voltage of the floating island (V_{ds}> V_{per}), the space charge area pierces the island and sets its potential. In this case, the drain-source capacity becomes equal to the depletion capacity of the main junction in series with the ability to depletion of the ''P-island/N-drift'' C_{ds2} junction:

$$C_{ds} = \frac{C_{ds1}.C_{ds2}}{C_{ds1} + C_{ds2}} \tag{I.47}$$

$$C_{ds2} = C_{ds2a} + C_{ds2b} \tag{I.48}$$

The capacities of plane and cylindrical "P-island / N-drift" junctions can be calculated in using relations (II.11), (II.12) and (II.13).

I.4.3.4. Gate-drain capacitance C_{gd}

The gate-drain capacitance C_{gd} is an important parameter of the power MOS transistors because it is the element of counter-reaction between the input and the output of these devices. She is too called Miller ability because it increases the dynamic capacity at the input of the device and thus reduces its switching speed. Indeed, the transition frequency of a transistor MOS power is limited primarily by the value of this ability. Indeed, the grid-drain capacity consists of two serial capabilities:

I) a C_{gdmax} oxide capacity of constant value, it is the equivalent capacity of Cgd when the voltage V_{ds} is lower than the voltage V_{gs}, that is to say when one is in regime accumulation.

II) a depletion capacity C_{gddep} on the surface of the intercellular zone under the grid and which intervenes when the voltage V_{ds} becomes greater than V_{gs}. The main difference lies in the doping of the drift zone of the structure FLIMOS which is superior to that of the equivalent VDMOS structure. Therefore, the depletion capacity of the structure FLIMOS increases because of the level increase doping the area under the gate oxide. To calculate this capacity, Sze [16] proposed the following formula:

$$C_{gd} = \frac{C_{j0}}{\sqrt{1 + \frac{2.{C_{ox}}^2.V_{dg}}{q.N_d.\varepsilon_0.\varepsilon_{SI}}}} \tag{I.49}$$

où C_{j0} est égale à $C_{gd\max}$.

I.5. Conclusion

In this chapter, we reviewed some power MOS transistor structures by recalling their mode of operation, the advantages and disadvantages of each structure. First, we presented the conventional structures of discrete and integrated power MOS transistors. Then, we gave the expression of the silicon boundary, which expresses the relationship between the specific pass resistance and the breakdown voltage in the case of vertical and lateral unipolar power MOS transistors. By this relation, we have demonstrated that the silicon limit is related to the structure of the unipolar device and the ionization energy of the material used. The arrival on the market of silicon carbide power MOSFETs is an essential element to go further in the concept of more electric devices. Indeed this type of component, which can be found in power converters as well as in electronic circuit breakers, has physical properties allowing it to operate at high temperature, high frequency, while drastically reducing conduction losses. and switching. SiC MOSFETs initially have electrical and thermal performance higher than their silicon equivalent. However, the question of the long-term stability of these performances and the reliability of the devices is worth asking. Indeed, as we have presented, the Metal-Oxide-Semiconductor structure of the SiC MOSFETs is the seat of wear mechanisms such as the gate oxide breakdown or the instability of the threshold voltage which are susceptible to alter the performance of the devices over time and lead to failure.

Our contribution is part of an investigation and modeling of the 4H-SiC MOSFET power transistor. In the second chapter, we will expose the analytical and numerical models that serve to optimize the performance of low power 4H-SiC MOSFET.

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CHAPTER 2:

Modeling of the Electrical Behavior of 4H-SiC MOSFET

Chapter 2

Modeling of the Electrical Behavior of 4H-SiC MOSFET

II.1. Introduction

Due to a rigorous formalism, the proposed model shows a good ability to support a large number of physical models, such as carrier mobility, incomplete ionization of doping atoms, and lifetime profiles. In this chapter, after a brief introduction to the principal structure of Silicon Carbide MOSFET, the attention is focused on the physical and electrical parameters useful for analyzing the behavior of power MOSFETs realized with this semiconductor, especially with the polytype of interest, the 4H-SiC.

II.2. 4H-SiC MOSFET structure

The schematic cross-section view of the n-channel 4H-SiC DMOSFET single-cell considered in this work is shown in figure II.1.

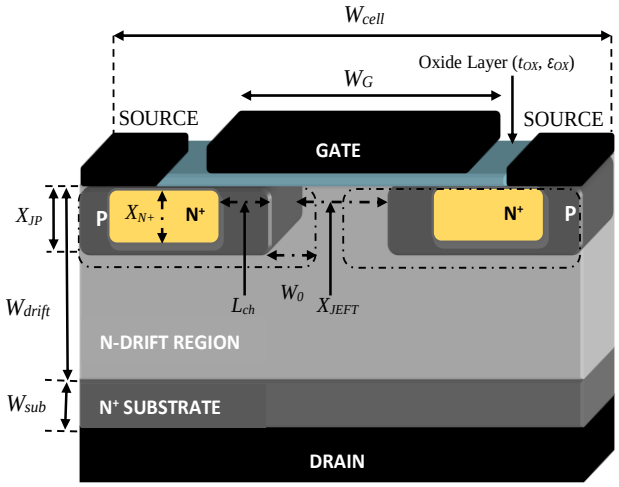


Figure II.1: Cross-section view of the n-channel 4H-SiC DMOSFET single-cell. The drawing is not in scale.

Here, the adopted notation concerning the geometry of the different device regions is also reported. In particular, W_{cell} is the cell width, L_{ch} is the device channel length, X_{JFET} is the distance between the base regions, W_{drift} is the thickness of the n-drift region, and X_{JP} and X_{N+} are the p-base and n+-source depths, respectively. The source contact shorts the source and the base regions to prevent the switch-on of the parasitic substrate(n^+)-epilayer(n)-base(p)–source(n^+) bipolar junction transistor. A silicon oxide layer is used to insulate the actual MOS structure.

II.3. Physical models

The DMOSFET numerical simulation study was developed by using a commercial TCAD-2D physical simulator that provides the solution of Poisson's equation and carrier continuity equation [1]. The fundamental physical models taken into account during the simulations and their reference parameters at T = 300 K are summarized in table II.I. They include

II.3.1. Transport Properties

The transport properties of 4H-SiC polytype are listed in Table II.1, along with other wide bandgap semiconductors, like Gallium Nitride and Diamond, and the most commonly used semiconductor materials (Si and GaAs). By a direct comparison, the advantages of SiC over Si are the tenfold increase in breakdown fields, twofold increase in saturation velocity, and more than doubling of thermal conductivity. Although the carrier mobility in Silicon Carbide is somewhat lower than in Silicon, in general the transport parameters give Silicon Carbide devices better performances than comparable Silicon devices. Investigating the basic electrical and physical parameters for electronic devices, such as bandgap (*Eg*), mobility (μ), saturation velocity (*vsat*), breakdown electric field (*Ecrit*), and thermal conductivity (λ), it instantly evident that wide bandgap semiconductors are very promising materials for using in high performance electronic devices.

II.3.1.1.The carrier mobility ($\mu_{n,p}$)

The mobility describes the mean velocity of electrons and holes when an electric field is applied. At low electric fields, the velocity increases proportional to the field, since the carrier mobility is fundamentally due to the Coulomb and phonon scattering; for higher fields, the proportionality is lost and the velocity saturates at v_{sat}. The carrier mobility ($\mu_{n,p}$) by means of both low-field and high-field models is given as follows:[2]-[4].

$$\mu_{n,p} = \mu_{0n,p}^{\min} + \frac{\mu_{0n,p}^{\max} - \mu_{0n,p}^{\min}}{1 + \left(\frac{N}{N_{n,p}^{crit}} \right)^{\delta_{n,p}}}, \tag{II.1}$$

$$\mu_{n,p}(E) = \frac{\mu_{n,p}}{\left[1 + \left(E \frac{\mu_{n,p}}{v_{sat}} \right)^{\kappa_{n,p}} \right]^{\frac{1}{\kappa_{n,p}}}} \tag{II.2}$$

where $\mu_{0n}^{\min}$ =40 cm²/V·s, $\mu_{0p}^{\min}$ = 15.9 cm²/V·s , $\mu_{0n}^{\max}$ = 950 cm²/V·s, $\mu_{0p}^{\max}$ = 125 cm²/V·s

N_n^{crit} = 2×10¹⁷ cm⁻³, N_p^{crit} = 1.76×10¹⁹ cm⁻³, δ_n = 0.76, δ_p = 0.34, k_n = 2, k_p = 1, v_{sat} = 2×10⁷ cm/s

II.3.1.2. The incomplete ionization of impurities ($N_A^-, {}_D^+$)

The incomplete ionization of impurity atoms affects the free carrier concentration of several wide-bandgap (WBG) semiconductor materials even at room temperature, thus modifying the electrical properties of power devices [5]-[7].

$$N_A^-, {}_D^+ = N_{A,D} \left(\frac{-1 + \sqrt{1 + 4 g_{v,c} \frac{N_{A,D}}{N_{V,C}(T)} e^{\frac{\Delta E_{A,D}}{kT}}}}{2 g_{v,c} \frac{N_{A,D}}{N_{V,C}(T)} e^{\frac{\Delta E_{A,D}}{kT}}} \right) \tag{II.3}$$

N_V = 3.29×10¹⁹ cm⁻³; N_C = 1.66×10¹⁹ cm⁻³; g_v = 4, g_c = 2

ΔE_A = 190 meV; ΔE_D = 70 meV

II.3.1.3. The carrier impact ionization rates ($\alpha_{n,p}$)

$$\alpha_{n,p} = a_{0n,p} \exp\left(-\frac{b_{0n,p}}{E}\right) \tag{II.4}$$

a_{0n} = 2.5 × 10^5 cm^{-1}; a_{0p} = 3.25 × 10^6 cm^{-1}; b_{0n} = 1.84 × 10^7 V/cm; b_{0p} = 1.71 × 10^7 V/cm

Recall that the impact ionization phenomenon is the origin of the avalanche breakdown. For the sake of more physical representation, the anisotropy model is taken into consideration and symbolized by anisotropic impact ionization for arbitrary electric field direction [8,9].

$$\alpha\left(E_x E_y\right) = ae^{\left(-c\sqrt{1-A^2c^2\left(\frac{E_x Ey}{b_x b_y}\right)^2}\right)} \tag{II.5}$$

where $A = \ln\left(a_y / a_x\right)$; $c = \frac{b}{E} = \left(\frac{E_x^2}{b_x^2} + \frac{E_y^2}{b_y^2}\right)^{-1/2}$; $a = a_x^{\frac{c^2E_x^2}{b_x^2}} a_y^{\frac{c^2E_y^2}{b_y^2}}$

E_x and E_y denote, respectively, the magnitude of the electric filed according to the *x* and *y* directions. The parameters a_x, a_y, b_x and b_y are depending on the plane orientation.

Table II.1: Anisotropic impact ionization parameters values [10], [11].

Symbol	c axis ||	a axis ⊥	Unit
a_e	1.76 × 10^8	2.1 × 10^7	cm^{-1}
b_e	3.3 × 10^7	1.7 × 10^7	V/cm
a_h	3.41 × 10^8	2.96 × 10^7	cm^{-1}
b_h	2.5 × 10^7	1.6 × 10^7	V/cm

Considering a high electric field, the carrier velocity saturation is modeled using the Canali model as follows [12]:

$$\mu_{\perp}^{high} = \frac{\mu_{\perp}^{low}}{\left[1+\left(\frac{\mu_{\perp}^{low}{}_{F}}{v_{\perp}^{sat}}\right)^{\delta}\right]^{\frac{1}{\delta}}} \quad \text{(II.6)}$$

with $v_{\perp}^{sat} = v_{0,\perp}^{sat}.\left(\frac{T}{300}\right)^{\zeta}$; $\delta = \delta_0\left(\frac{T}{300}\right)^{\eta}$

where $\mu_{\perp}^{high}$, $\mu_{\perp}^{low}$, and $v_{\perp}^{sat}$ denote, respectively, the high-field mobility, the low field mobility, and the saturation velocity. The following table contains the values of carrier saturation velocity parameters under high electric field [13, 14].

Table II.2: Saturation velocities parameters values

$v_{0,\perp}^{sat}$ [cm/s]	δ_0	δ	η
2.2×10^7	1.2	-0.46	0.88

II.3.2. Carrier recombination lifetime

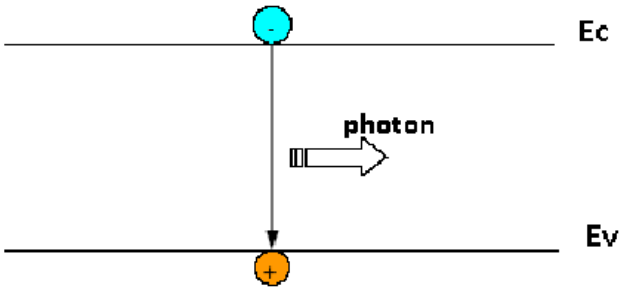
In semiconductor materials the generation of electrons and holes in excess is due to thermal activity, electrical and/or light excitation; opposite to this phenomenon, there is the recombination of such carriers, whose rate can be defined by the following expression:

$$U = \frac{\Delta c}{\tau} \quad \text{(II.7)}$$

with Δc the excess carrier density, and τ the recombination lifetime of such carriers. This latter parameter is strongly related to the crystal quality and defects and, since its value quantifies the effect of different processes which conjointly participate to the recombination phenomenon, it is important to use a complete model that includes all the involved recombination mechanisms in order to get an accurate estimation of the effective lifetime. As shown in the following sections, there are fundamentally three recombination mechanisms which occur in semiconductors, with different intensities: radiative recombination, Auger recombination and recombination through defects in the bandgap [15]. Respect to the latter, the first two are band to band, or direct, recombination processes and they depend only on the concentration of free carriers present in the bulk semiconductor. The free carrier concentrations (electrons and holes) are defined as:

$$n = n_0 + \Delta n \approx N_D + \Delta n \quad \text{for n - type material}$$
$$p = p_0 + \Delta p \approx N_A + \Delta p \quad \text{for p - type material} \tag{II.8}$$

where n_0, p_0 are the electron and hole concentrations at equilibrium, N_D, N_A the donor and acceptor doping density, and Δn , Δp the density of electrons and holes in excess per unit volume. (see illustrations below)



At equilibrium, both excess carrier concentrations must be equal, because the generation process involves the creation of electron-hole pairs, i.e.$\Delta n = \Delta p$. Therefore, at given doping density and illumination level mechanisms, the direct recombination processes are exclusively inherent to the material properties: in this case, the only way to reduce the total recombination rate is through the minimization of the number of defect during the manufacture process.

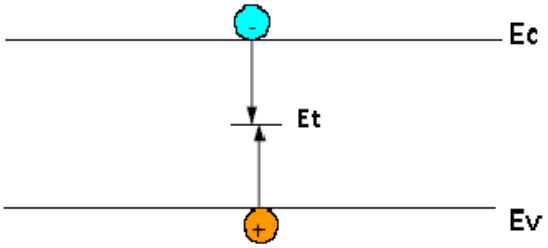
II.3.2.1. The Shockley-Read-Hall recombination (R_{SRH})

The recombination through defects in the bandgap is a process which is the dominant recombination mechanism in semiconductors with indirect forbidden bandgap, such as Silicon and Silicon Carbide. It results explicitly dependent on the number of imperfections in the crystal, caused by impurities or by crystallographic defects, such as vacancies and dislocations. These imperfections originate intermediate states (see illustration) within the bandgap that act as recombination centers, or traps, for the free carriers. The theory for recombination through these localized traps was for the first

time analyzed by Shockley and Read [16,17] and then by Hall. Their analytical model which describes the recombination rate (SRH-rate) is given by:

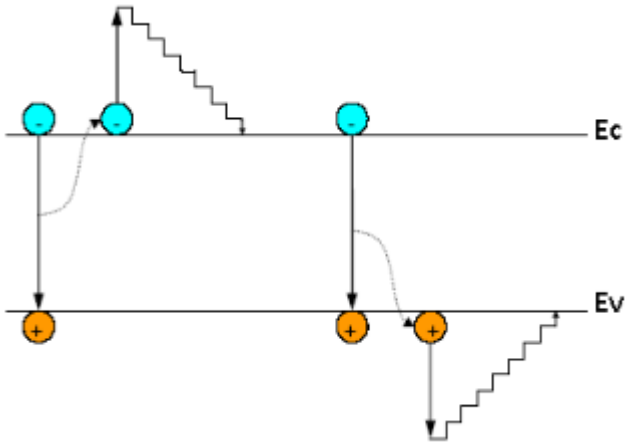
$$R_{SRH} = \frac{pn - n_i^2}{\tau_p\left(n + n_i \exp\left(\frac{E_{trap}}{kT}\right)\right) + \tau_n\left(p + n_i \exp\left(-\frac{E_{trap}}{kT}\right)\right)} \qquad \text{(II.9)}$$

where n_i = 6.7×10-11 cm-3. Here, E_T and E_i are, respectively, the recombination center and the intrinsic Fermi energy levels; N_t is the recombination center density; v_{th} is the electron thermal velocity, and σ_n ,(σ_p) is the capture cross section, that is an estimation of how much the electron (hole) must be near to the trap to be captured.



II.3.2.2 The Auger recombination (R_{Auger})

Auger recombination, that can be considered as the inverse of the impact ionization process, involves three particles (one electron and two holes, or vice versa). It occurs when the energy released by the recombination of an electron-hole pair is transferred to a third free carrier [18,19], as shown in the illustration. In this process, at low injection level, the expression of the recombination rate is related to the excess carrier concentration and to doping density [20]:



$$R_{Auger} = \left(C_{Ap}\, p + C_{An} n\right)\left(np - n_i^2\right) \tag{II.10}$$

with C_{An} and C_{Ap} the Auger coefficients for electrons and holes

C_{An} = 5×10^{-31} cm^6/s

C_{Ap} = 2×10^{-31} cm^6/s

II.3.2.3. The doping dependent carrier lifetime ($\tau_{n,p}$)

Due to the fragmentary knowledge that actually is available for the Silicon Carbide, the carrier lifetime is still a crucial parameter, especially for monitoring the semiconductor properties and the device operation conditions. So, it must not amaze the intensive effort made by a lots of scientific works to provide accurate measurement methods (one of which is discussed in Chapter 4) for evaluating the carrier lifetime, not only for conventional materials but also for innovative semiconductors, like SiC. the expression of the carrier lifetime related to doping density :[21, 22],

$$\tau_{n,p} = \frac{\tau_{0n,p}}{1 + \left(\frac{N}{N_{n,p}^{SRH}}\right)} \tag{II.11}$$

where τ_{0n} = 500 ns, τ_{0p} = 100 ns, $N_{n,p}^{SRH}$ $N_{n,p}^{SRH}$= 1×10^{30} cm^{-3}

II.3.3. The apparent bandgap narrowing ($\Delta E_{gp,n}$)

In devices containing adjacent layers or regions with different doping concentrations, doping-induced band edge displacements may greatly influence device behaviour. This is due to the resultant potential barrier which influences carrier transport across the junctions. Apparent bandgap narrowing models for calculating the shifts in band edges for 4H-, 6H- and 3C-SiC have been published in the 1998 by Lindefelt [23,24]. Relatively to 4H-SiC, he quantifies the band edge displacements as a function of the activated doping according to the following expressions:

$$\Delta E_{gp,n} = A_{p,n}\left(\frac{N_{A,D}^{-,+}}{10^{18}}\right)^{\frac{1}{2}} + B_{p,n}\left(\frac{N_{A,D}^{-,+}}{10^{18}}\right)^{\frac{1}{3}} + C_{p,n}\left(\frac{N_{A,D}^{-,+}}{10^{18}}\right)^{\frac{1}{4}} \tag{II.12}$$

$A_p = 1.54\times10^{-3}$; $B_p = 1.3\times10^{-2}$; $C_p = 1.57\times10^{-2}$; $A_n = 1.17\times10^{-2}$; $B_n = 1.5\times10^{-2}$; $C_n = 1.9\times10^{-2}$

As displayed in figure II.2, where a direct comparison is done respect to the Si, a larger ΔEg is expected in n-type material for 4H-SiC, whereas approximately the same isplacements are obtained in p-type material for both materials. The resultant bandgap narrowing effect and its influence on the intrinsic carrier concentration are shown in figure II.3.

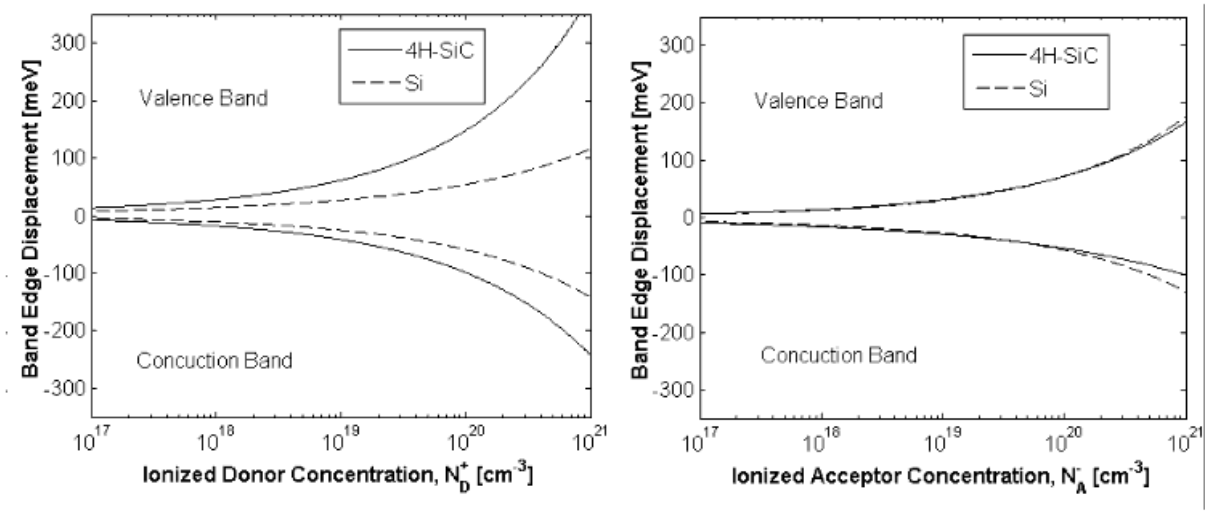


Figure II.2: Conduction and valence band displacements for 4H–SiC vs ionized doping concentration in purely *n*-type (left) and *p*-type (right) material. For comparison, the band edge displacements for Si are also shown [24]

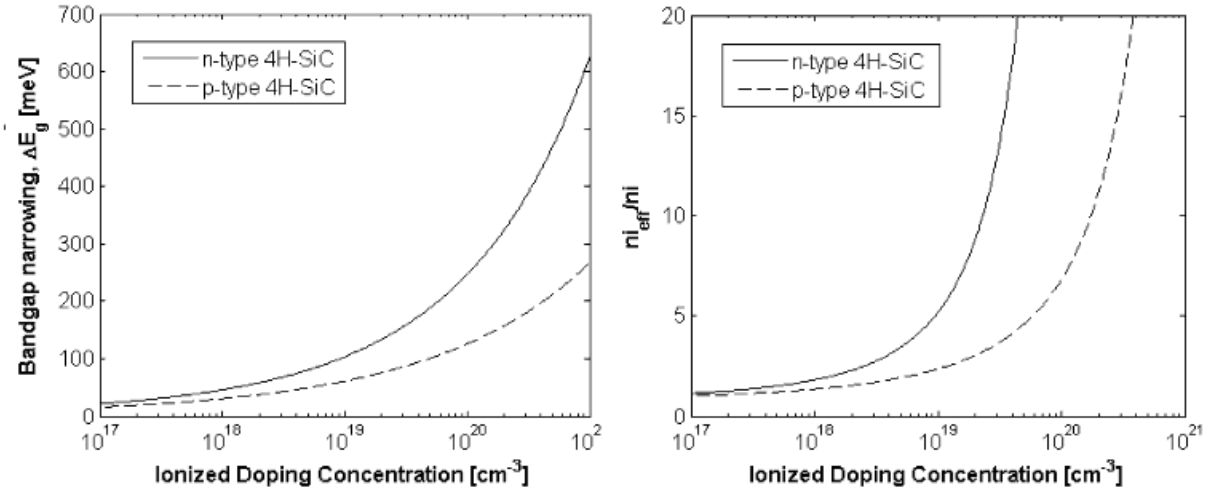


Figure II.3: Bandgap narrowing in 4H-SiC (left) and corresponding influence on the effective intrinsic carrier density (right) [24].

II.3.4.4H-SiC/SiO2 interface

In addition, all the simulations are carried out taking Fermi-Dirac statistics and multidimensional dependent anisotropic effects (Aniso) into consideration. A full description of the models used can be found in reference [25]. Also in order to take into account the scattering mechanisms such as phonon scattering, surface roughness scattering, impurity scattering and coulomb scattering that degrade the channel mobility. Lombardi model is considered for mobility degradation in this work. This model has been chosen and verified for SiC MOSFET simulations [26].

The above mentioned simulation setup and the relative parameters details arereported in recent authors manuscripts addressed to the study of 4H-SiC-based devices [27-29]. Moreover, the models prediction capabilities are supported by experimental results that was obtained on both implanted p-i-n and Schottky diodes in a wide range of currents and temperatures [30-34].

In order to take into account the defect and trap effects at the SiO_2/4H-SiC interface, we solve the Poisson's equation in the channel region in the form of

$$\nabla \cdot \left(\varepsilon \nabla \Psi \right) = q\left(n - p - N_D^+ + N_A^- \right) - Q_T \tag{II.13}$$

where an overall trapped charge contribution Q_T is considered in addition to the ionized donor (N_D^+) and acceptor (N_A^-) impurity concentrations to describe the variation of the electrostatic potential ψ with the local (total) charge density.

According to [35], the incomplete ionization of impurities is given by

$$N_{A,D}^{-,+} = N_{A,D}\left(\frac{-1+\sqrt{1+4g_{v,c}\dfrac{N_{A,D}}{N_{V,C}(T)}e^{\frac{\Delta E_{A,D}}{kT}}}}{2g_{v,c}\dfrac{N_{A,D}}{N_{V,C}(T)}e^{\frac{\Delta E_{A,D}}{kT}}} \right) \tag{II.14}$$

where N_D and N_A are the substitutional n-type and p-type doping concentrations, $N_C$and N_V are the electron and hole density of states varying with temperature, g_c = 2 and g_v = 4 are the degeneracy factors of the conduction and valence band, and ΔE_D and ΔE_A are the donor and acceptor energy levels, respectively.

The interface density of states (DoS) in the 4H-SiC inversion layer is modelled by the following expression [36,37]

$$D_{it}(E) = D_{it,T} + D_{it,M} \tag{II.15}$$

where $D_{it,M}$ is a Gaussian distribution of deep states in the mid-gap and $D_{it,T}$ is the sum of two exponentially decaying band tail states close to the conduction and valence band-edges, respectively. More in detail, we can write

$$D_{it,T} = D^0_{t,TC} \exp^{[(E-E_C)/U_C]} + D^0_{t,TV} \exp^{[(E_V-E)/U_V]} \tag{II.16}$$

$$D_{it,M} = D^0_{t,M} \exp^{[(E-E_M)/W_M]^2} \tag{II.17}$$

where E_C and E_V are the conduction and valence band energies, U_C and U_V are characteristic energy decays, $D^0_{t,TC}$ and $D^0_{t,TV}$ are the band edge intercept densities, W_M takes into accounts the spectral width of the mid-gap Gaussian distribution, and E_M is the energy value of the defect density peak $D^0_{t,M}$.

In Equation (3) each term acts either as donor-like or acceptor-like level for free carriers [25]. In other words, a donor-like center is positively charged (ionized) when empty and neutral when filled (with an electron), while an acceptor-like center is negatively charged (ionized) when filled and becomes neutral when empty.

The total charge Q_t is therefore expressed by

$$Q_t = q(D^+_{it,D} - D^-_{it,A}) \tag{II.18}$$

where, referring to the terms $D_{it,M}$ and $D_{it,T}$ introduced above, $D^+_{it,D}$ and $D^+_{it,A}$ are the ionized densities for donor-like and acceptor-like traps, respectively. In particular, each ionized density depends upon the trap density and the relative probability of ionization, which is in the form of

$$F_{t,D} = \frac{v_{th}\sigma_n + e_p}{v_n(\sigma_p + \sigma_n) + (e_n + e_p)} \tag{II.19}$$

$$F_{t,A} = \frac{v_{th}\sigma_p + e_n}{v_p(\sigma_p + \sigma_n) + (e_n + e_p)} \tag{II.20}$$

Here,v_n and v_p are the carrier thermal velocities, and σ_n and σ_p are the trap capture cross sections for electrons and holes, respectively. Finally, e_n and e_p are the trap emission rates given by

$$e_n = v_n \sigma_n n_i \exp\left(\frac{E - E_i}{kT}\right) \tag{II.21}$$

$$e_p = v_p \sigma_p n_i \exp\left(\frac{E_i - E}{kT}\right) \tag{II.22}$$

Where E_i is the intrinsic Fermi level and n_i is the intrinsic carrier concentration.
The fundamental DoS parameters used during the simulations are summarized in Table II.2 [25,37,38]. In particular, the trap density reference values are assumed as in [37].

II.4. 4H-SiC MOSFET Figure of merits

II.4.1. Breakdown *voltage*

The breakdown or blocking voltage (BV_{DS}) characteristics of a DMOSFET can be calculated when the device is in a firm off-state, *i.e.* V_G = 0 V and grounded source. The BV_{DS} value, in fact, is related to the onset of a breakdown within the base-drain p-i-n structure for an increasing bias voltage V_{DS}. By assuming the drift-region in a punch-through condition, namely totally depleted before the breakdown occurs. A first level prediction of BV_{DS} is given by [39]

$$BV_{DS} = E_{pn}^{crit} W_{drift} - \frac{qN_{drift}W_{drift}^2}{2\varepsilon_{sc}} \tag{II.23}$$

where E_{pn}^{crit} is the critical electric field that appears somewhere along the border of the p-base/n-drift junction, ε_{sc} is the material permittivity, and N_{drift} is the doping concentration in the drift region. This expression is validated for $W_{drift} \leq \varepsilon_{sc} E_{pn}^{crit} q^{-1} N_{drift}^{-1}$. For example, considering typical values of the 4H-SiC permittivity and a critical electric field of 2 MV/cm, the width of the n-type drift region has to be in the limit of 10 µm for

N_{drift} = 1 × 10^{16} cm^{-3} [39]. This result was also calculated in [38] for a similar p-i-n structure.

The electric field dependence on N_{drift} is in the form of [40]

$$E_{pn} = 2.49\times10^{6}\left(5-0.25\log N_{drift}\right). \tag{II.24}$$

II.4.2. On-state resistance

The total on-state resistance in the device current path is the sum of various contributions as follows

$$R_{ON} = R_{N+} + R_{ch} + R_{acc} + R_{JFET} + R_{drift} + R_{sub} \tag{II.25}$$

where R_{N+} is the source resistance, R_{ch} is the channel region resistance, R_{acc} is the accumulation region resistance relative to the distance X_{JFET} next to the channel (see figure II.1), R_{JFET} refers to the JFET channel portion, R_{drift} is the resistance of the drift region, and R_{sub} is the substrate contribute. In accordance with figure II.1, the appropriate expressions of these terms can be written as [39]

$$R_{ch} = \frac{L_{ch}W_{cell}}{2\mu_{ch}C_{OX}\left(V_{GS}-V_{TH}\right)}, \tag{II.26}$$

$$R_{acc} = \frac{X_{JFET}W_{cell}}{4\mu_{acc}C_{OX}\left(V_{GS}-V_{TH}\right)}, \tag{II.27}$$

$$R_{JFET} = \frac{\rho_{JFET}X_{JP}W_{cell}}{W_G-2X_{JP}-2W_0}, \tag{II.28}$$

$$R_{drift} = \frac{\rho_{drift}W_{drift}W_{cell}}{W_{cell}-W_G+2X_{JP}+2W_0}\ln\left(\frac{W_{cell}}{W_G-2X_{JP}-2W_0}\right) \tag{II.29}$$

Here, in particular, C_{OX} is the gate oxide capacitance, μ_{ch} and μ_{acc} are, respectively, the doping-dependent mobilities of the inversion and accumulation layers, ρ_{JFET} is the resistivity of the JFET region, and W_0 is the zero-bias depletion width in the JFET region computed by using

$$W_0 = \sqrt{\frac{2\varepsilon_{SC} N_A V_{bi}}{qN_{JFET}(N_A + N_{JFET})}} \tag{II.30}$$

where N_A and N_{JFET} are the doping concentrations in the p-base and JFET region, respectively, and the built-in potential V_{bi} is in the form of

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_{JFET}}{n_i^{\,2}}\right) \tag{II.31}$$

Note that, for the sake of simplicity, in our calculations, the resistance contributions R_{N+} and R_{sub} are considered negligible because they are relative to heavily doped regions.

II.4.3. Threshold *voltage and drain current*

The DMOSFET threshold voltage (V_{TH}) is defined as the gate bias voltage that assures the strong inversion regime in the channel region. Its value depends on the doping concentration in the p-base and increases linearly with the gate oxide thickness. A typical expression of V_{TH} is given by [39]

$$V_{TH} = \frac{t_{OX}}{\varepsilon_{OX}}\sqrt{4\varepsilon_{SC} kTN_A \ln\left(\frac{N_A}{n_i}\right)} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{II.32}$$

By neglecting the subthreshold current (*i.e.*, $I_D = 0$ for $V_{GS} < V_{TH}$) and assuming the DMOSFET operating point in the triode region (*i.e.*, $V_{DS} \le V_{GS} - V_{TH}$), the drain current was calculated considering [41]:

$$I_D = \mu_{ni} C_{OX} \frac{W_{cell}}{L_{ch}}\left[2(V_{GS} - V_{TH})(V_{DS} - I_D R_{ON}) - (V_{DS} - I_D R_{ON})^2\right] \tag{II.33}$$

where the $(V_{DS} - I_D R_{ON})$ term is the drain internal voltage that differs from the terminal one for the ohmic contribution.

Finally, for $V_{DS} > V_{GS} - V_{TH}$ we use:

$$I_D = \mu_{ni} C_{OX} \frac{W_{cell}}{2L_{ch}}(V_{GS} - V_{TH})^2\left[1 + \lambda(V_{DS} - I_D R_{ON})\right] \tag{II.34}$$

where λ is an appropriate channel modulation coefficient.

II.5. Conclusion

In this chapter the important set for 4H-SiC device simulation has been compiled from literature data. The associated parameters of the most important models in unipolar devices simulation are described in this chapter. The numerical simulation analysis was performed using the Atlas-Silvaco TCAD physical simulator. The device structure was fine meshed wherever appropriate and in particular around the p–n junctions and the surface channel region under the SiO2/ 4H-SiC interface. The total number of mesh points was about 32,000 and the mesh spacing was scaled down to 0.5 nm at the interfaces. The key physical models taken into account include the material bandgap temperature dependence, apparent bandgap narrowing effect, Auger and Shockley–Read–Hall recombination phenomena, incomplete doping activation, impact ionization, and carrier lifetime and carrier mobility expressions depending on temperature and doping concentration. Moreover, Fermi–Dirac statistics and multidimensional dependent anisotropic effects as well as scattering mechanisms that degrade the channel mobility were considered during the simulations. In addition a combined model of defect energy levels inside the 4H-SiC bandgap (tail and deep-level traps) and oxide-fixed traps has been considered. The trap densities have been assumed referring to literature data.

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CHAPTER 3:

Physical and Geometrical parameters effect

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III.1. Introduction

The vertical power metal–oxide–semiconductor field effect transistor (MOSFET) structure was developed in the mid-1970s to obtain improved performance when compared with the existing power bipolar transistors. One of the major issues with the power bipolar transistor structure was its low-current gain when designed to support high voltages [1]-[5]. In addition, power bipolar transistors could not be operated at high frequencies due to the large storage time related to the injected charge in their drift regions and were prone to destructive failure during hard switching in applications with inductive loads. The replacement of these current-controlled devices with a voltage-controlled device was attractive from an application's viewpoint. The high input impedance of the metal–oxide–semiconductor (MOS)- gate structure simplified the drive circuit requirements when compared with bipolar transistors being used at that time [6-7]. In addition, their superior switching speed opened new applications operating in the 10–50 kHz frequency domain. Today, 4H-SiC power MOSFETs are the most commonly used power switches in applications where the operating voltages are below 200 V [8-11]. In order to meet the specific constraints related to modern power electronics, the design of 4H-SiC MOSFETs needs the deployment of intensive efforts based on numerical, analytical, and empirical calculations, which carefully take into account the different geometrical and physical parameters that affect the device performance [12]-[15].

Since the temperature affects considerably the device figure of merits (FOMs) [16, 17], it is relevant to investigate the device performance in wide range of temperature. In addition, it is worth to note that the 4H-SiC hexagonal crystal structure presents an anisotropy that depends on the wafer orientation [18, 19]. Hence, it is mandatory to examine the device under different crystallographic plane mobility models.

In this work, we investigate the electrical characteristics of a 4H-SiC DMOSFET designed for low voltage ratings (150 V) over a wide range of temperatures [300K-500K]. It is worth to note that smart maximum power point trackers (SMPPT) converters for photovoltaics are characterized by R_{ON} in the limit of few hundreds kΩ/μm^2 for a blocking voltage of 150 V or less [20]-[23]. For the sake of physical reality, both isotropic and anisotropic mobility models are considered in this study to investigate their effects on the forward characteristics. The interweaving effects of 4H-SiC DMOSFET parameters related to different regions yields to a crucial problem of compromise. In order to achieve high electrical performances, we investigate the effect of different design parameters on the performance of 4H-SiC DMOSFET. Despite the fact that several studies deal with the tradeoff between the FOMs of a 4H-SiC DMOSFET [24]-[26], to the best of our knowledge, no investigations have been made about a global performance optimization based on evolutionary algorithms. With this intent, MOGA-based optimization approach [27] is used to improve the 4H-SiC DMOSFET FOMs in terms of breakdown voltage, drain current and on-state resistance. The obtained results are compared with those reported in [28].

III.2. Simulation analysis

In this section, the impacts of temperature and fundamental design parameters on the main figure of merits of the DMOSFET are investigated by using the geometrical parameters and doping concentrations listed in table III.1 as initial entry data for modeling. In addition, both anisotropic and isotropic mobility models are investigated and compared.

Table III.1: 4H-SiC DMOSFET reference parameters.

Silicon oxide thickness, t_{ox} (μm)	0.08
Source thickness, X_{N+} (μm)	0.5
Channel length, L_{ch} (μm)	1
Base junction depth, X_{JP} (μm)	1.5
Base-to-base distance, XJFET (μm)	7
Epilayer thickness, W_{drift} (μm)	10
Substrate thickness, W_{sub} (μm)	100
Gate width, W_G (μm)	9.4
Cell width, W_{cell} (μm)	15
Device footprint area (μm^2)	15
N$^+$-source doping, N_D (cm^{-3})	1×10^{18}
P-base doping, N_A (cm^{-3})	1.5×10^{17}
N-drift doping, N_{drift} (cm^{-3})	1×10^{16}
N$^+$-substrate doping, N_{sub} (cm^{-3})	1×10^{19}

III.2.1. Analysis of temperature effect

Figures. III.1 and III.2 depict the curves of the drain current as function of the drain-source and gate-source voltages, respectively, for a wide range of temperature.

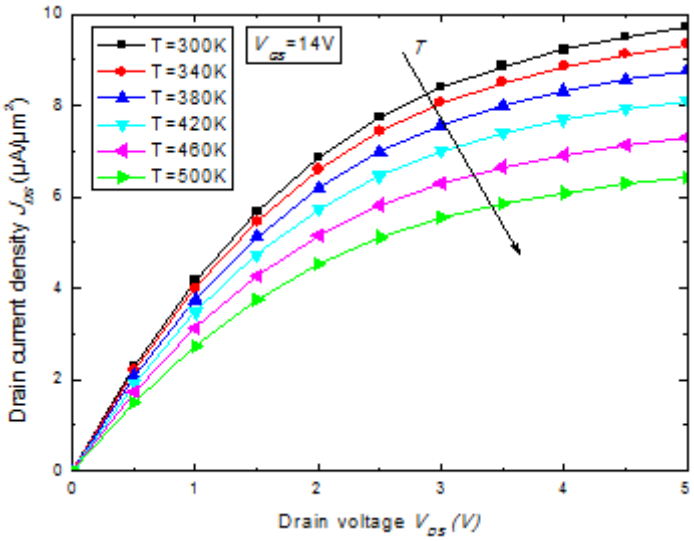


Figure III.1: Drain-source voltage versus the forward drain current for [300 K- 500 K].

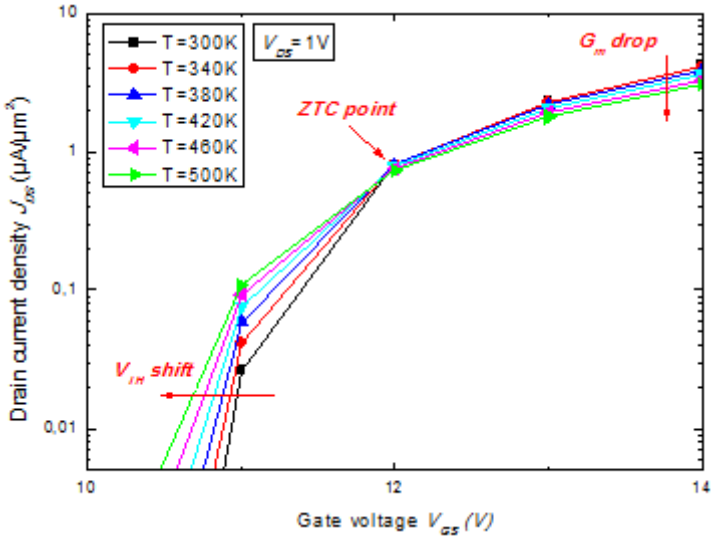


Figure III.2: Gate-source voltage versus the forward drain current for [300 K- 500 K]

As shown in Figure III.1, the drain current decreases severely when increasing temperature. This fact is due essentially to the close connection between the temperature and the carrier mobility at the level of the inversion layer. Besides, since the resistance is dependent upon the collisions that occur between the charge carriers and atoms, the overall resistance is expected to increase. As for the drain current versus

the gate voltage curve (Figure III.2), when the temperature increases, the threshold voltage lessens leading to a zero temperature coefficient (ZTC) point at 12 ± 0.05V; this fact may be linked to the augmentation of the 4H-SiC intrinsic carrier concentration.

The drain current density and the on-state resistance curves as function of the temperature are depicted in figure III. 3. It is clear that the more the temperature increases, the more the on-state resistance rises. This fact is caused by the diminution of the carrier mobility at the level of both inversion layer and the drift region [7].

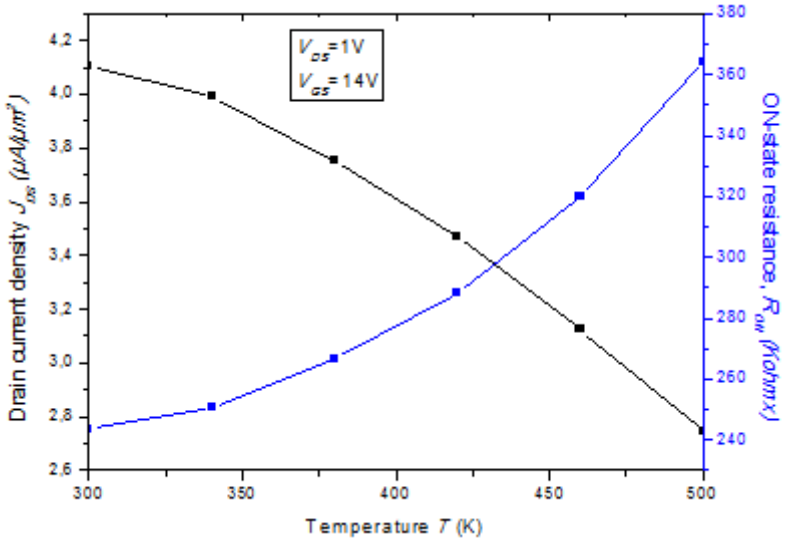


Figure III.3: On-state resistance and drain current density as function of the temperature (V_{GS}=14V, V_{DS}=1V, N_{drift}=1×10^{16} cm^{-3}, N_A=1.5×10^{17}cm^{-3}).

III.2.2. Isotropic and anisotropic mobilities study

In the following, the isotropic and anisotropic models are examined. Two isotropic mobility models, namely <1100> and <1000> planes are considered. As for the anisotropic model, it is established in both <1100> and <1000> planes by introducing anisotropic impact ionization and high filed velocities saturation into the physical model.

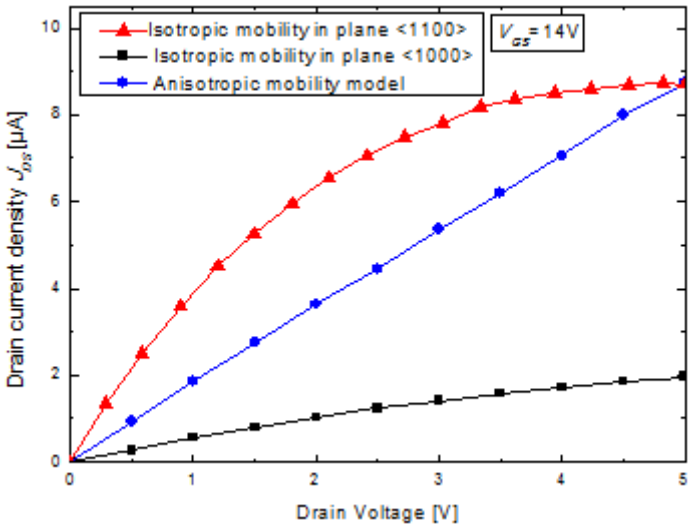


Figure III.4: I_D – V_{DS} curves for the device in Table III.1 at different mobility models

(V_{GS}=14V, L_{ch}=1μm, N_{drift}=1×10^{16} cm^{-3}, N_A=1.5×10^{17}cm^{-3}).

Figure III. 4 depicts the I_D – V_{DS} characteristics of the considered device for both isotropic and anisotropic models. It is worth to note that the drain current of the isotropic model for the <1100> plane surpasses those of the isotropic for the <0001> plane and the anisotropic one. This difference is mainly due to the fact that the isotropic model for the <1100> plane is representative of the current flow in the channel direction which is the high mobility plane. However, the pinch-off region in the channel controls the current saturation in the channel region.

In contrast, the isotropic model for the <0001> plane exhibits a less current value that is essentially due to the long path (almost twice longer than that of the channel length) that causes high rate of carriers recombination. Besides, this region offers a high resistance value thanks to a low-level doping concentration.

As for the anisotropic model, it considers the realistic situation. Firstly, it encompasses the majority of the physical effects that occurs in the channel represented

by the <1100> plane, namely high channel mobility, pinch-off and current saturation. Secondly, it takes into consideration the current degradation in the plane <0001> caused by the high drift region resistance and carriers recombination.

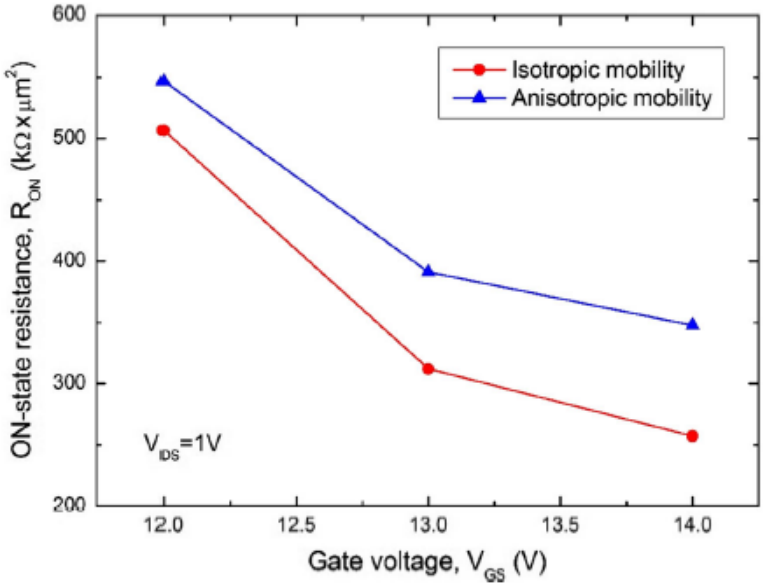


Figure III.5: R_{ON} as a function of V_{GS} for different mobility models (V_{DS}=1V, L_{ch}=1μm, N_{drift}=1×10^{16} cm^{-3}, N_A=1.5×10^{17}cm^{-3}).

Figure III.5 depicts the variation of the on-state resistance R_{ON} as function of the gate voltage V_{GS} for different mobility models. It is clear that anisotropic model exhibits a considerable resistance than that of the isotropic model for the <1100>. This is mainly due to the thickness and the doping concentration level of the drift region. More precisely, the drift region resistance constitutes the dominant part in the on-state resistance.

III.2.3. Physical and geometrical parameters effect

The BV_{DS} value is strictly dependent on the n-drift thickness, which determines the distance between the base junction and the substrate, *i.e.* the difference W_{drift} - X_{JP}.

In the numerical analysis, BV_{DS} was calculated considering the device in the off-state and raising gradually V_{DS} up to the occurrence of an electric field threshold of 1.9 MV/cm. The increase of V_{DS}, in fact, is responsible for the expansion of the depletion region to the low-doped side of the p-base/n-drift junction and the more the depletion region expands, the more the electric field increases. The drain leakage current density,

J_D, was kept below 10 mA/cm^2. For the considered device, we calculated a BV_{DS} of about 900 V. Then, W_{drift} was reduced up to 1.8 µm to meet the constraint of a BV_{DS} value close to 150 V. Different values of BV_{DS} as a function of W_{drift} are summarized in Table III.2.

The electric field and drain current behaviors are shown in figure. III.6 as a function of the drain voltage for two devices with different W_{drift} thicknesses, namely, W_{drift} = 5.0 µm and W_{drift} = 1.8 µm. In particular, W_{drift} = 1.8 – µm device was identified as the one meeting the specification of BVDS = 150 V for the P-base and N-epilayer doping levels reported in Table III.1.

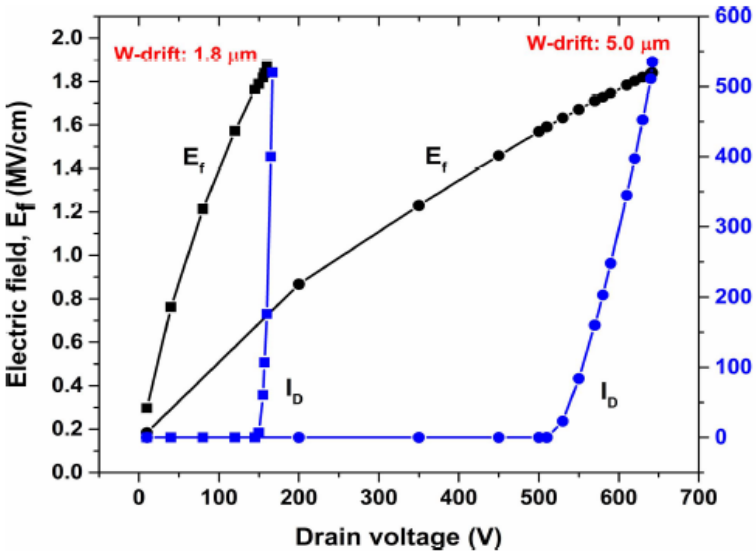


Figure III.6: Electric field (black curve) and drain current (blue curve) as a function of the drain bias for two devices with different W_{drift} [28].

However, it should be considered that the P-base/N-epilayer junction is weakly asymmetrical in this case (1.5 10^{17} cm^{-3} versus. 10^{16} cm^{-3} dopings), and therefore, the electric field in the OFF-state is in fact sustained by both sides of the junction, namely, the Nepilayer (W_{drift}) and the P-base (W_{P_base}), with consequent increase of BV_{DS}.

Table III.2: DMOSFET breakdown voltage versus n-drift thickness, assuming an electric field threshold of 1.9 MV/cm and N_{drift} = 1×10^{16} cm^{-3}

W_{drift} (µm)	BV_{DS} (V)
10	900
8	800
6	700
4	500
3	350
2	200
1.8	150

The influence of the n-drift doping concentration on BV_{DS} was also evaluated. In particular, decreasing the doping concentration from 1×10^{16} cm^{-3} to 1×10^{15} cm^{-3}, we calculated a decrease in the critical electric field with a maximum reduction of BV_{DS} on the order of 10% for the same drain leakage current level assumed previously. For example, for the investigated device, we simulated BV_{DS} = 850 V for N_{drift} = 3×10^{15} cm^{-3} as in [28]. However, as expected, in the investigated n-drift doping range, N_{drift} has only a limited effect on the device BV_{DS} characteristics considering the thinner values of W_{drift} (*i.e.*, W_{drift} ≤ 3 µm in Table III.2) [7].

The DMOSFET I_D - V_{DS} curves of a device which has W_{drift} = 1.8 µm and N_{drift} = 3×10^{15} cm^{-3} are shown in figure III.7 for V_{GS} from 10 to 14 V. From the simulations, it was pointed out that the device is in a really on-state for V_{GS} > 8V.

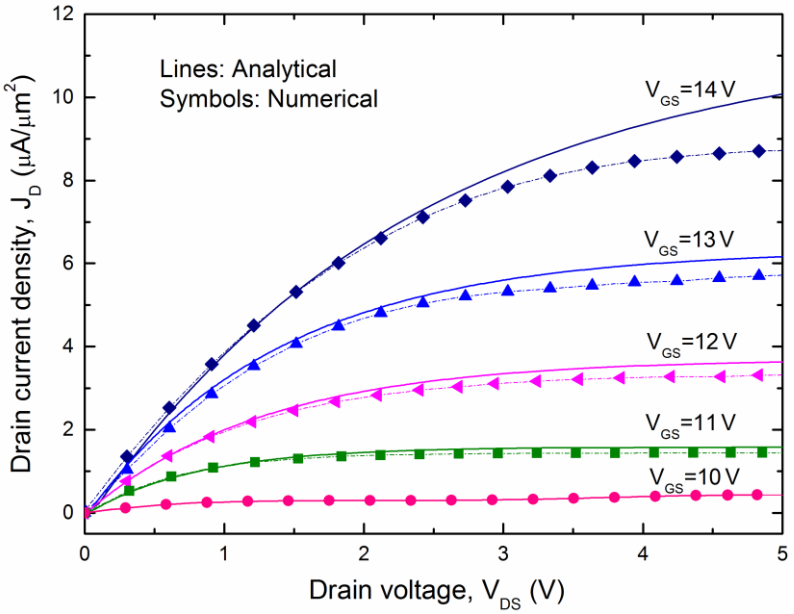


Figure III.7: DMOSFET forward I_D - V_{DS} characteristics. W_{drift} = 1.8 µm and N_{drift} = 1×10^{16} cm^{-3}. The other geometrical and electrical parameters are those listed in Table III.2.

As we can see, the numerical simulations and analytical model results are in good agreement especially by assuming the device operating in the deep triode region (V_{DS} -≤ -2-V).

For V_{DS} =1 V and V_{GS} = 14 V, the drain current is close to 3.9 µA/µm², corresponding to an on-state resistance R_{ON} of about 255 kΩ×µm². From figure III. 7, different values of R_{ON} calculated for different V_{DS} as a function of V_{GS} are plotted in figure III. 8.

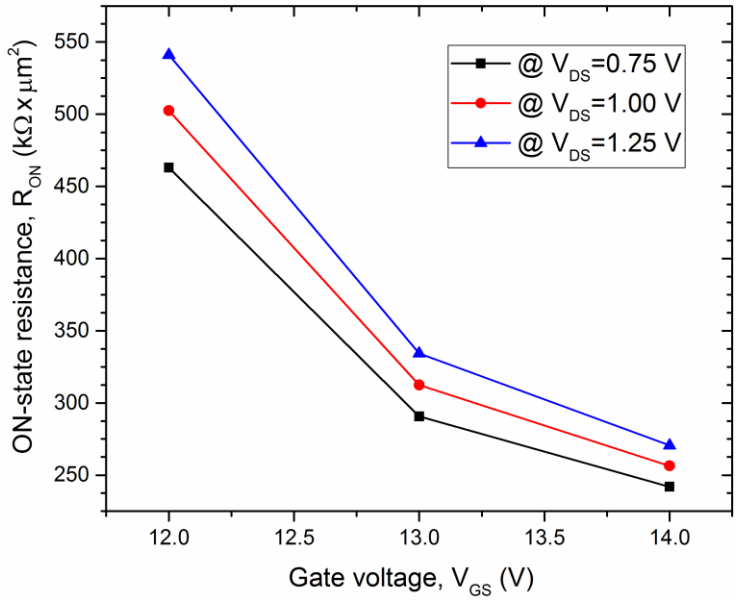
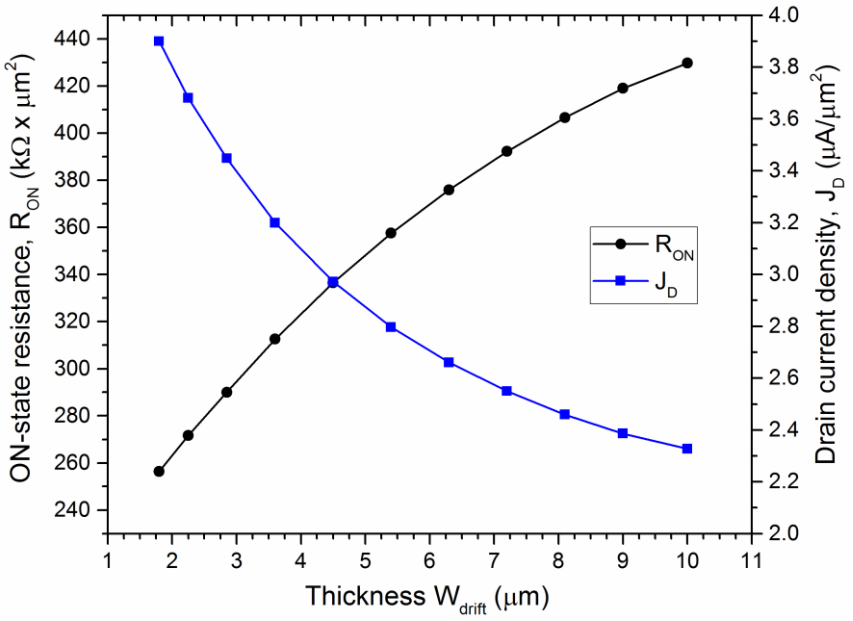


Figure III.8: R_{ON} as a function of V_{GS} for different V_{DS}.

Critical physical and geometrical parameters that determine the device on-state resistance are the drift region thickness W_{drift}, the n-drift doping concentration N_{drift}, and the channel length L_{ch}. The DMOSFET R_{ON} and J_D curves as a function of these fundamental parameters are shown in figure III. 9 for V_{GS} = 14 V and V_{DS} = 1 V.


ON-state resistance, R_{ON} (kΩ x μm^2)
Drain current density, J_D (μA/μm^2)
Thickness W_{drift} (μm)
R_{ON}
J_D
440
420
400
380
360
340
320
300
280
260
240
4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
2.4
2.2
2.0
1
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10
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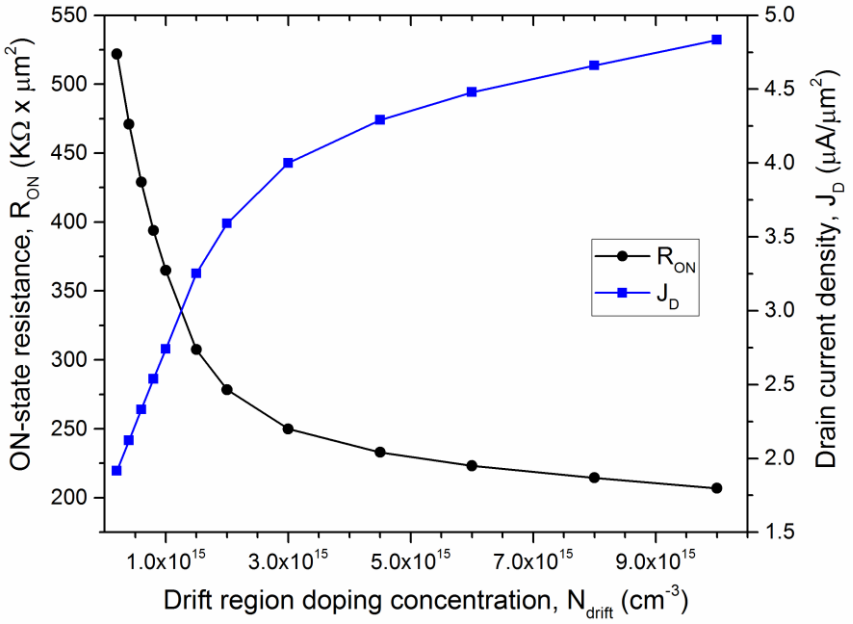
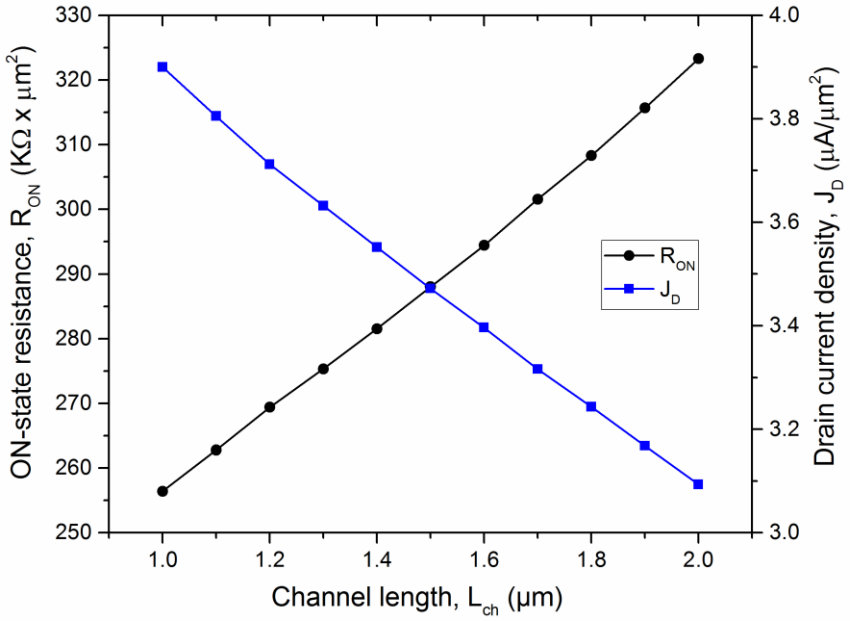
(a)


ON-state resistance, R_{ON} (KΩ x μm^2)
Drain current density, J_D (μA/μm^2)
Drift region doping concentration, N_{drift} (cm^{-3})
R_{ON}
J_D
550
500
450
400
350
300
250
200
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0x10^{15}
3.0x10^{15}
5.0x10^{15}
7.0x10^{15}
9.0x10^{15}

(b)



(c)

Figure III.9: R_{ON} and J_D behaviors as a function of W_{drift} (a), N_{drift} (b), and L_{ch} (c), for V_{GS} = 14 V and V_{DS} = 1 V.

As expected, from figure III. 9 (a) and (b) the drain current increases with decreasing W_{drift} and increasing N_{drift} as a result of the R_{ON} decreasing due to a reduction of its component R_{drift}. On the other hand, from figure III.9 (c) an increasing channel length tends to increase R_{ON} via the component R_{ch} rather in a linear manner.

Finally, keep fixed the base depth and the distance between the base regions, we simulated the R_{ON} behavior for different doping concentrations, N_{JFET}, in the JFET region under the gate oxide. In the simulated doping range of N_{JFET} (from 3×10^{15} cm^{-3} to 3×10^{16} cm^{-3}), results show that this parameter has only a limited impact on the R_{ON} value. This fact is mainly due to the weak dependence of the on-state current on the majority carrier concentration in the JFET region where the inversion layer is formed.

III.3. MOGA-based optimization approach

In recent years, MOGA-based technique has gained great popularity in the scientific community and encompassed many research areas. This technique focuses, in particular, on the optimal solution of multi-dimensional and nonlinear problems [29]-[32]. Distinctive characteristics of the MOGA approach are the universality and simple implementation. It is well known that the majority of optimization procedures provide a

single solution. In contrast, MOGA-based techniques permit to find a set of optimized solutions commonly called 'Pareto front'. This allows to select an appropriate combination of results according to the application field.

The background in this scenario is to establish many proper arguments, namely a set of objective functions, different constraints, and design parameters. Then, the multi-objective optimization provides different solutions achieving the best compromise between the considered functions. Moreover, the criteria can involve dilemma and/or complementary conditions. A simplified schematic flowchart for a multi-objective genetic algorithm is shown in figure III.10.

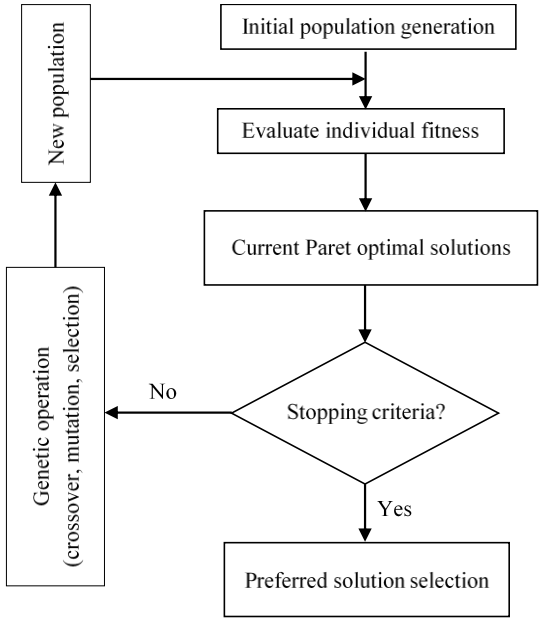


Figure III.10: Schematic flowchart for a multi-objective genetic algorithm.

In MOGA terminology, a population is a set of chromosomes generated randomly, where each chromosome is made of numbered units called genes. The genes correspond to the design parameters such as channel length, drift region thickness and doping etc... So, a chromosome is a combination of design parameters. MOGA is based on the application of crossover, mutation, and selection operators on a certain generation. Starting from two chromosomes, called parents, the operation of crossover consists in combining them to obtain a new chromosome called offspring which is expected to get good genes. This process is repeated for all the chromosomes to yield to the best offspring. The mutation occurs at the gene level. The mutation operator aims to

guarantee the exploration of all the state space. The process of selection concerns the obtained set of offspring from all their parents. It permits to choose the best offspring to create the next generation of population. Many techniques of selection are available such as tournament selection, ranking, and proportional selection. Starting from an initial population, these operations allow the algorithm to evolve through different generations up to a required criterion is reached. Otherwise, the constraint on the maximum number of iterations will determine its end.

III.3.1. 4H-SiC DMOSFET optimized design

In this section, the MOGA-based technique is used as an alternative to a simulation study (numerical and/or analytical) to find the optimized design of a 4H-SiC DMOSFET in terms of its breakdown voltage and on-state resistance for the proposed application. In other words, we deal with two objective functions that are considered in the form of $BV_{DS}(Y)$ and $R_{ON}(Y)$ where $Y = \{t_{ox}, W_G, L_{ch}, W_{drift}, X_{JP}, X_{N+}, X_{JFET}, N_A, N_D, N_{drift}\}$ is a vector of the fundamental geometrical and physical device parameters.

The design optimization of the considered device is established according to the following purpose: minimization of the on-state resistance and maximizing the breakdown voltage for a fixed drain-source voltage range. With respect to realistic physical and geometrical values, proper constraints that determine the excursion of the parameters in *Y* were defined. Tournament selection and scattered crossover techniques were employed to generate random vectors of *Y*. By biomimicry considerations, each combination of *Y* was binary coded. A full set of configuration parameters used in this study for the MOGA-based optimization is summarized in table III.3 [33, 34].

Table III.3: Configuration parameters used for the MOGA-based optimization.

Number of variables	10
Population size	1000
Maximum number of generations	100
Selection	Tournament
Crossover	Scattered
Mutation	Adaptive Feasible Migration
Crossover fraction	0.8
Migration fraction	0.2
Front Pareto population fraction	0.5

It is worth to note that a MOGA-based technique can use indifferently the analytical model or the numerical one as fitness function. However, the complexity of the DMOSFET design, which involves different interwoven parameters, suggests to evaluate the algorithm computational time performing a comparison between the procedures based either on numerical or analytical prerequisites. Moreover, it is important to note that, as shown previously, the output I_D-V_{DS} characteristics of both models are in good agreement within the device triode region. In order to deal with this computational time comparison, the weighted sum approach method was used to incorporate the two objective functions defined above in a single one expressed by

$$F(Y) = w_1(1/BV_{DS}) + w_2 R_{ON} \qquad \text{(III.1)}$$

where the optimal solution varies according to the values of the weighting factors w_1 and w_2. In particular, we considered three cases, namely w_1 = 0.25, w_2 = 0.75 (a), w_1 = w_2 = 0.5 (b), and w_1 = 0.75, w_2 = 0.25 (c). The *F(Y)* behaviors as a function of the evolving generations for different weighting factors are depicted in figure III. 11.

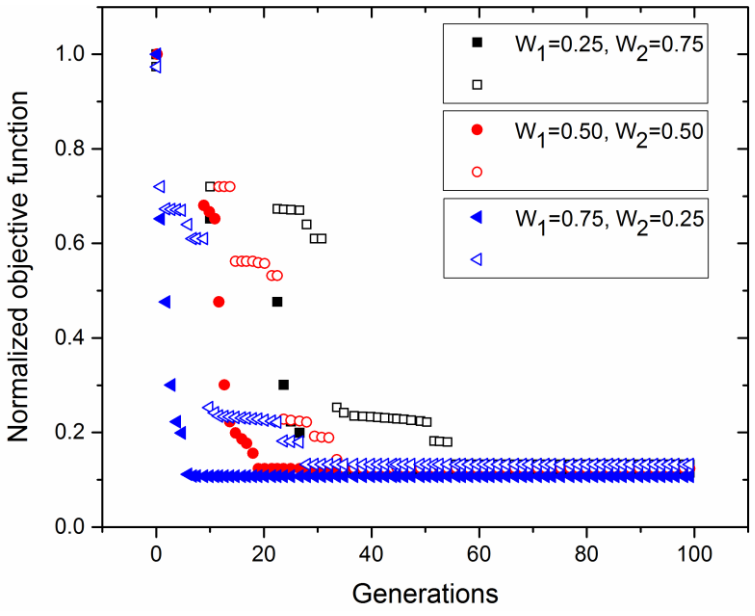


Figure III.11: *F(Y)* behaviors *vs.* generations for different weighting factors w_1 and w_2, both using the numerical (filled symbols) and the analytical (empty symbols) model as fitness functions.

As we can see, for a mono-objective function *F(Y)* based on a numerical fitness function the convergence occurs within 28 (a), 18 (b) and 5 (c) generations, respectively. In contrast, it occurs within 55 (a), 35 (b) and 28 (c) generations for *F(Y)* based on an analytical one. In addition, these latter optimization procedures required a much longer computational time (about twice), which is in the order of 10-15 minutes on an up-to-date PC. For the sake of rapidity, in what follows only the numerical model was considered.

The Pareto front with the assumed objective functions $R_{ON}(Y)$ and $BV_{DS}(Y)$ is depicted in figure III.12. Each pair of solutions (R_{ON}, BV_{DS}) corresponds to a specific combination of the vector *Y*.

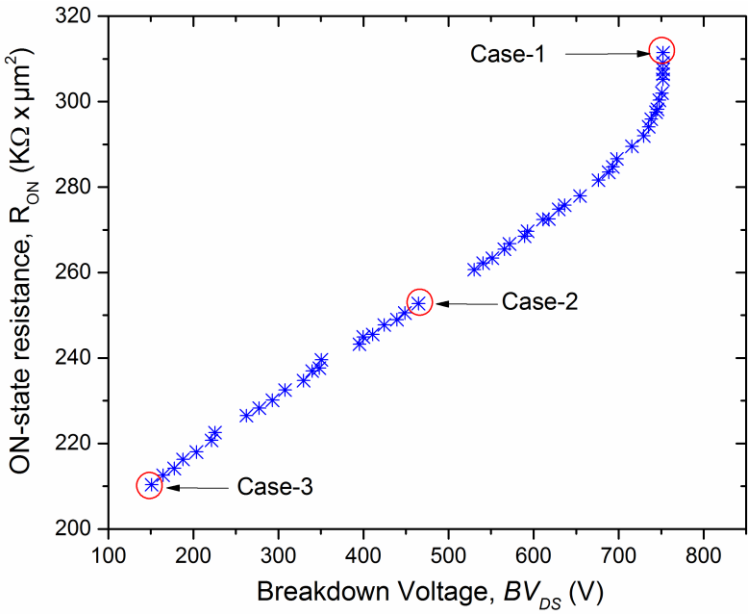


Figure III.12: Pareto-optimal solutions for the DMOSFET design.

As shown in figure III. 12, we chose three pairs of solutions to assess the accuracy of the proposed optimization in the design of a device rated for BV_{DS} of 150 V (case-1), 450 V (case-2), and 800 V (case-3), respectively. The relative geometrical and physical parameters are listed in table III.4. Here, the fundamental device parameters reported in [28], which refer to a 4H-SiC DMOSET with the same device footprint area of 15 μm² and dimensioned for BV_{DS} = 150 V, are also reported for comparison. The R_{ON} values are calculated for V_{GS} = 14 V and V_{DS} = 1 V.

Table III.4: MOGA-based optimization of the 4H-SiC DMOSFET design parameters.

Design parameters	**Case 1**	**Case 2**	**Case 3**	**Ref. [28]**
Silicon oxide thickness, t_{ox} (µm)	0.085	0.085	0.085	0.08
Source thickness, X_{N+} (µm)	0.5	0.5	0.5	0.5
Channel length, L_{ch} (µm)	1.06	1.14	1.0	1.0
Base junction depth, X_{JP} (µm)	2.0	2.0	1.65	1.5
Base-to-base distance, X_{JFET} (µm)	6.13	6.72	7.6	7.0
Epilayer thickness, W_{drift} (µm)	10	3.75	1.8	1.8
Gate width, W_G (µm)	8.65	9.4	10	9.4
N^+-source doping, N_D (cm^{-3})	1×10^{18}	1×10^{18}	1×10^{18}	1×10^{18}
P-base doping, N_A (cm^{-3})	1×10^{17}	1×10^{17}	1.25×10^{17}	1.5×10^{17}
N-drift doping, N_{drift} (cm^{-3})	2.88×10^{15}	2.89×10^{15}	2.89×10^{15}	3×10^{15}
Objective functions				
On-state resistance, R_{on} (kΩ×µm²)	315	250	210	260
Breakdown voltage, BV_{DS} (V)	800	450	150	150

In order to highlight more the efficiency of the proposed design strategy, a comparison with the R_{ON} results calculated in [28] for V_{GS} that spans from 11 V to 15 V and V_{DS} = 1 V is shown in figure III.13. It can be clearly seen that, for a device performing the same BV_{DS}, the presented MOGA-based optimization performs a better R_{ON} behavior in the whole investigated V_{GS} range. In fully on-state, in fact, R_{ON} decreases by a factor up to 20%.

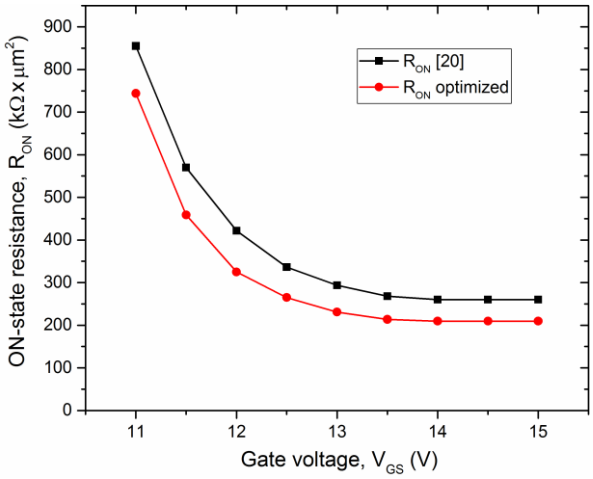


Figure III.13: R_{ON} comparison between the MOGA-based results and those reported in [28].

III.4. Conclusion

In this work, we have investigated via numerical simulation the effects of temperature, the isotropic and anisotropic mobility models and the physical and geometrical parameters on the 4H-SiC DMOSFET figure of merits. The more the temperature increases, the more the drain current decreases. This state of fact is due to the augmentation of the on-state resistance value which is caused by the diminution of the carrier mobility. In parallel, the threshold voltage shifts negatively due to the augmentation of the 4H-SiC intrinsic carrier concentration.

To be more representative of reality, both isotropic and anisotropic are studied and compared in terms of forward characteristics. It is clear that, due to many physical considerations, namely high resistance and carriers recombination in the drift region, the anisotropic mobility model leads to a certain current degradation.

A substantial part in this work has concerned the investigation on the effects of physical and geometrical parameters on the device figure of merits. Afterwards, the analytical and numerical models have been used as fitness functions for a MOGA-based design which aims to fix the optimal geometrical and physical parameters that minimize the on-state resistance value for devices with different breakdown voltage rates. In particular, without loss of generality, this study has been referred to a low-voltage DMOSFET dimensioned to show a breakdown voltage of 150 V. The proposed device performs an on-state resistance in the order of 210 $k\Omega \times \mu m^2$ which is decreased by a factor of 20%.

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CHAPTER 4:

Temperature and SiO2/4H-SiC interface trap effects on the electrical characteristics

Temperature and SiO_2/4H-SiC interface trap effects on the electrical characteristics

IV.1. Introduction

The main technological issue of a SiC-based MOSFET is the effective quality of the silicon oxide (SiO_2) interface that could made the device much less efficient [1-10]. Defects occurring in the SiO_2/4H-SiC interface, in fact, heavily affects the MOSFET current capabilities [11-14]. More in detail, through the enhanced scattering mechanisms of free carriers, interface trap effects tend to decrease the effective carrier mobility in the channel region, increase the device on-state resistance (R_{ON}), and increase the sensitivity of the threshold voltage (V_{th}) to the temperature.

In this contest, the aim of the work is to investigate, by means of a careful numerical simulation study, the electrical characteristics of a 4H-SiC MOSFET designed for low voltage ratings (150 V) over a wide range of temperatures. Without loss of generality with respect to different designs dimensioned for higher blocking voltages, explicit interface trap effects due to a detailed density of states in the inversion region and to a fixed trap density in the oxide are considered referring to literature data. Preliminary results at room temperature and neglecting defect and trap effects were presented in [5,6] in order to emphasize, as stated previously, the use of fast and rugged 100-V-class switches. The obtained results clarify the role of the interface traps in reducing the carrier mobility in the channel region. At the same time, the device threshold voltage decreases as a function of both the trap density and temperature. In particular, a high oxide-fixed trap density meaningfully influences the V_{th} value. Finally, this study indicates that deep level traps at the 4H-SiC interface have only a limited effect in determining the MOSFET R_{ON} once the tail traps contributions have been introduced. The R_{ON} is in the order of 200 kΩ×μm^2 for a defected device at V_{GS} = 10 V,V_{DS} = 1V and T = 300K. This result is compared to the state-of-the-art of a commercial Si-MOSFET with the same breakdown voltage supporting the opportunity to explore the use of 4H-SiC

also for lower voltage applications where efficiency, robustness, miniaturization, and temperature control are critical targets.

IV.2. MOSFET structure

The schematic cross-section of the considered vertical n-channel 4H-SiC MOSFET single-cell is shown in Fig. I.1.

The different geometrical parameters are labelled as follows: W_{cell} is the cell width, W_G is the gate contact width, L_{ch} is the device channel length, W_J is the distance between the base regions, X_{N+} is the n+-source junction depth, X_P is the p-base junction depth, W_{drift} is the n-drift region thickness, W'_{drift} is the base-to-substrate distance, and W_{sub} is the starting substrate thickness. The source contact shorts the source and base regions to prevent the switch-on of the parasitic substrate(n^+)-epilayer(n)-base(p)–source(n^+) bipolar junction transistor. The reference geometrical and doping parameters used during the simulations are summarized in Table IV.I.

Table IV.1: MOSFET reference parameters.

Silicon oxide thickness, t_{ox} (μm)	0.08
Source thickness, X_{N+}(μm)	0.5
Channel length, L_{ch} (μm)	1
Base junction depth, X_P(μm)	1.3
Base-to-base distance, W_J(μm)	7
Epilayer thickness, W_{drift} (μm)	1.8
Base-to-substrate distance, W'_{drift} (μm)	0.5
Substrate thickness, W_{sub}(μm)	100
Gate contact width, W_G (μm)	9.4
Cell width, W_{cell} (μm)	15
N^+-source doping, N_D (cm^{-3})	1×10^{18}
P-base doping, N_A (cm^{-3})	1×10^{16}
N-drift doping, N_{drift} (cm^{-3})	3×10^{15}
N^+-substrate doping, N_{sub} (cm^{-3})	1×10^{19}

From Table IV.1, the distance between the n^+-source region and the n-epilayer (X_P-X_{N+}) is 0.8 μm, which assures a device breakdown voltage close to 150 V.

Although simplified for simulation purposes, the proposed structure is in principle compatible with a manufacturing process based on doping by ion implantation [15-17].

IV.3. *I-V-T* characteristics in absence of trap effects

By considering the 4H-SiC MOSFET described in Table IV.1 as a structure free of interface defects and trap effects (fresh device), the current density curves I_D-V_{DS} and I_D-V_{GS} calculated for the half-cell in figure I.1 (A = 7.5μm^2) at different temperatures are shown in figure IV.2 and figure IV. 3, respectively.

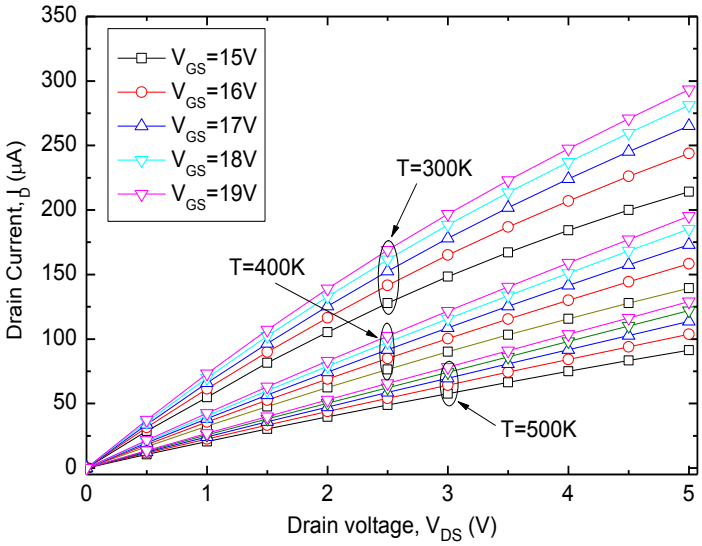

Figure IV.2: Forward I_D- V_{DS} characteristicsfor the device in Table IV.1 at T =300 K, T=400 K, and T=500 K. (N_{drift}=3×10^{15}cm^{-3}, N_a=10^{16}cm-3, L_{ch}=1μm, W_{drift}=1.8μm)

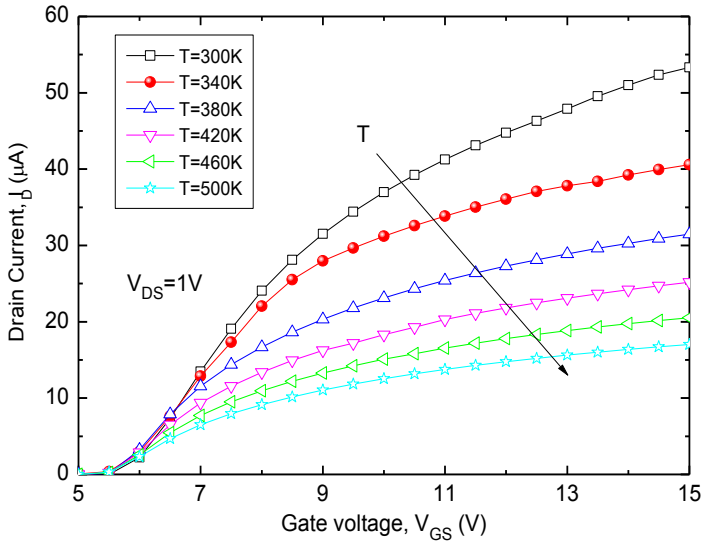

Figure IV.3: I_D – V_{GS} curves for the device in Table IV.1 at different temperatures.

(N_{drift}=3×10^{15}cm^{-3}, N_a=10^{16}cm-3, L_{ch}=1μm, W_{drift}=1.8μm)

As expected, the drain current decreases harshly when increasing temperature. This effect is determined by the temperature dependence of the carrier mobility in the inversion layer and the overall increase of the device on-state resistance.

By imposing a subthreshold current in the limit of 10 nA during the simulations, the temperature dependence of the device threshold voltage is shown in figure IV. 4. Here, the degradation of total carrier mobility behavior in the channel region is also reported. The plot is traced by taking a cut-line of the device structure for V_{GS} = 15 V and V_{DS} = 1 V.

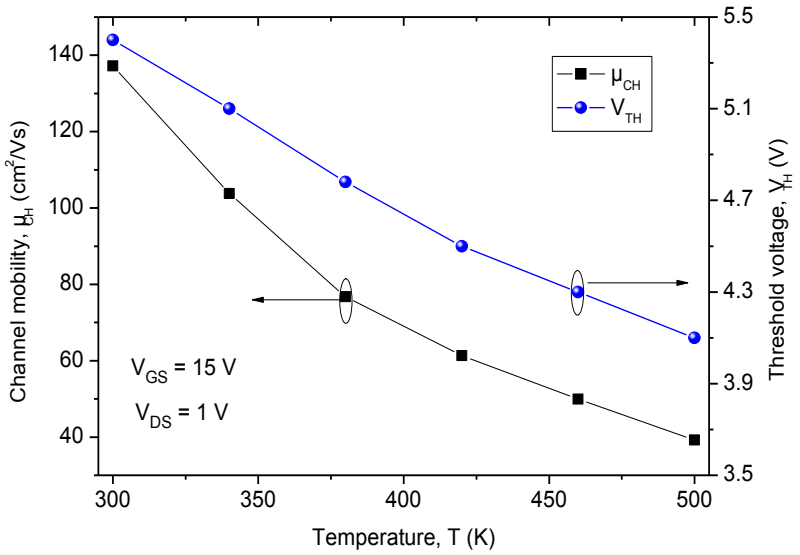

Figure IV.4: Channel mobility and device threshold voltage as a function of the temperature. (N_{drift}=3×10^{15}cm^{-3}, N_a=10^{16}cm-3, W_{drift}=1.8µm, V_{GS}=15V, V_{DS}=1V)

From figure IV.4 we observe that the threshold voltage and total channel mobility decrease with temperature is due to the increase of the 4H-SiC intrinsic carrier concentration. These V_{TH} and μ_{ch} variations determine different values of the device transconductance which results in the order of 25 S at T=300 K and decreases to about 10 S at T=500 K in the considered range of gate to source voltage V_{GS}.

From figure IV. 3, the drain current density for V_{GS} = 15 V and V_{DS} = 1 V at T = 300K is 7.11 µA/µm^2(I_D= 53.32 µA, A = 7.5 µm^2). The corresponding MOSFET on-state resistance R_{ON} is therefore calculated as close to 140 kΩ×µm^2.

The R_{ON} behavior as a function of the temperature is shown in figure IV. 5. Here, the R_{ON} increase with temperature is mainly due to the decrease of the carrier mobility in the inversion layer as well as in the drift region [30]. In other words, the increased temperature limits the current components which origin in these two regions.

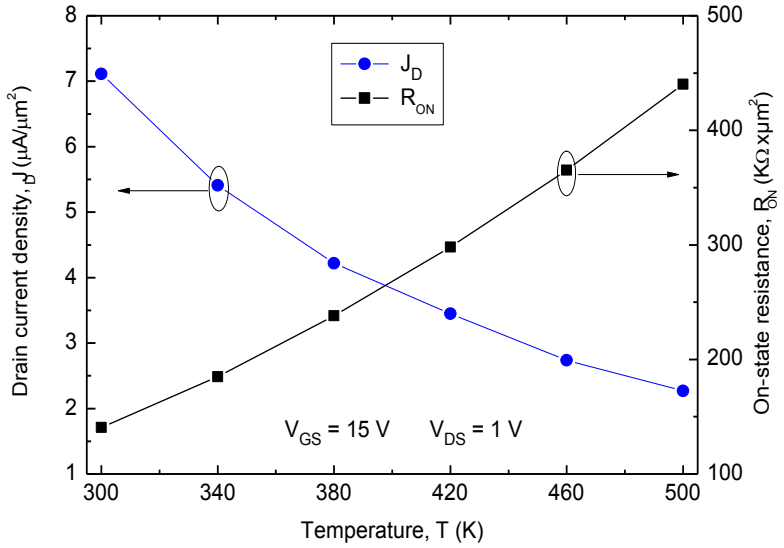

Figure IV.5: On-state resistance and drain current density as a function of the temperature. (N_{drift}=3×10^{15}cm^{-3}, N_a=10^{16}cm-3, W_{drift}=1.8µm, μ_{ch}=*1µm,* V_{GS}=15V, V_{DS}=1V)

IV.4. Analysis of trap effects at the SiO2/4H-SiC interface

IV.4. 1. Tail traps

Introducing in the model a constant value of the deep traps in the mid-gap of 2.3×10^{11} cm^{-2} eV^{-1} [28], figure IV.6 depicts the device I_D-V_{GS} characteristics in semi-logarithmic scale calculated at T=300K, T=400K, and T=500K for a different band tail trap density. In particular, in (4) we have considered the band edge intercept density in the range 10^{12}-10^{14} cm^{-2} eV^{-1} [28,31].In addition, it is important to note that, from the simulations, the traps with energetic states close the valence band can be neglected once the contribution $D_{t,TC}^{0}\exp^{[(E-E_C)/U_C]}$ has been introduced. In this study, in fact, when the device is forward biased, even in weak inversion condition, the Fermi level more and more moves in the upper half of the bandgap.

From figure IV. 6, similarly to the fresh device, the device threshold voltage tends to decrease as the temperature increases. For V_{GS}>V_{th}, the saturated value of I_D is almost the same up to a tail trap density in the limit of 10^{13} $cm^{-2}eV^{-1}$. Then, for example for $D_{t,TC}^{0}$ = 10^{14} $cm^{-2}eV^{-1}$, the device current capabilities are meaningfully penalized at any V_{DS} bias level.

When a positive V_{GS} is applied, the acceptor defect states are able to trap a great number of electrons from the inversion layer, thus making them immobile and excluding them from carrier transport mechanisms. In addition, at each temperature, these filled traps origins Coulomb scattering phenomena of mobile charges by causing in turn a reduced drain current and a positive shift of the threshold voltage. On the other hand, the more the temperature increases, the more the number of filled traps decreases; hence, the threshold voltage decreases as stated above.

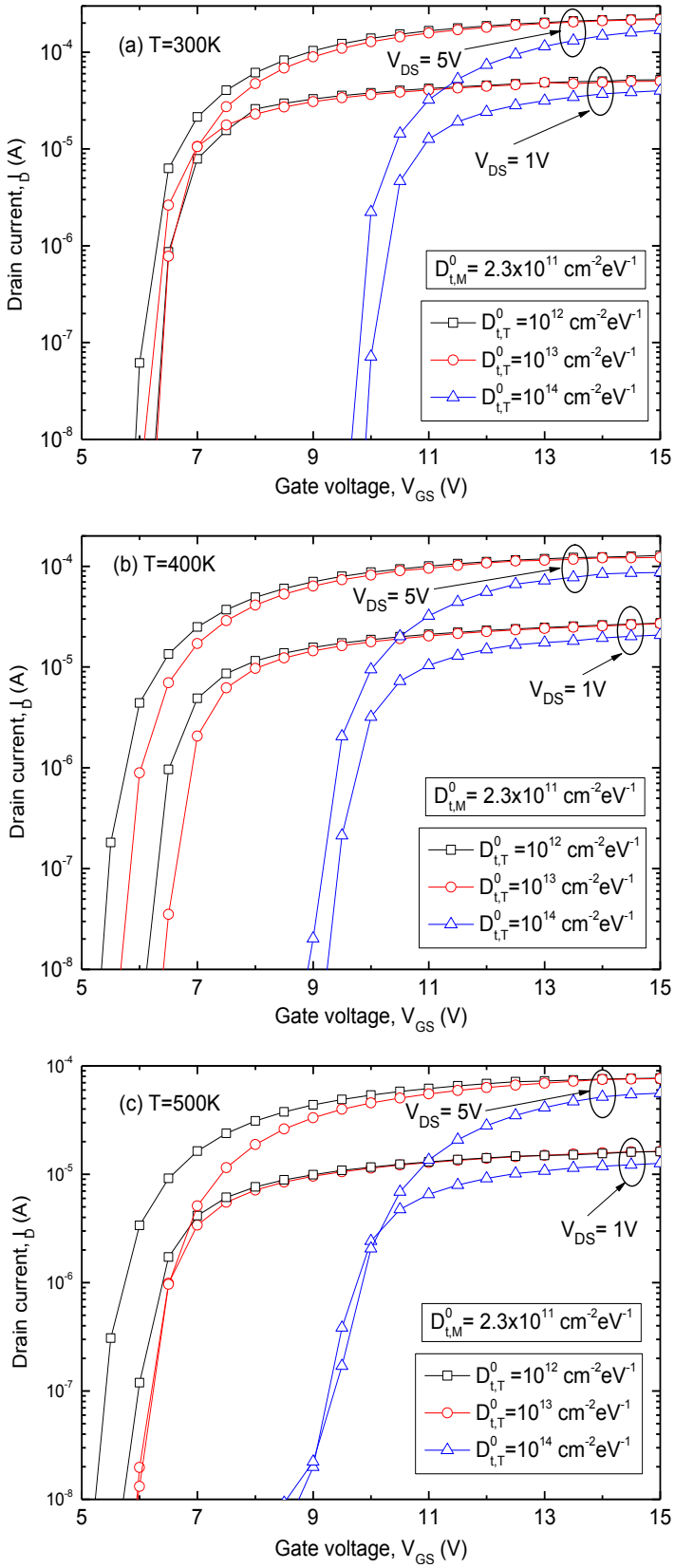

Figure IV.6: $I_D - V_{GS}$ characteristics as a function of the tail trap density at (a) T = 300K, (b) T = 400K, and (c) T=500K. (N_{drift}=3×10^{15}cm^{-3}, N_a=10^{16}cm-3, W_{drift}=1.8µm, μ_{ch}=1μm)

The MOSFET R_{ON} behaviors as a function of V_{GS} both for a fresh and a defected device are shown in figure IV.7. From the simulations, the R_{ON} of a heavily-defected device dramatically increases for increasing temperature in particular at low biases ($V_{GS} \leq 12$ V) as a consequence of the mobility degradation induced by traps [32]. For V_{GS}> 12 V, however, the increase of mobile carriers leads to an increased screening of traps which supports the MOSFET output current limiting the R_{ON} increase especially at low temperatures.

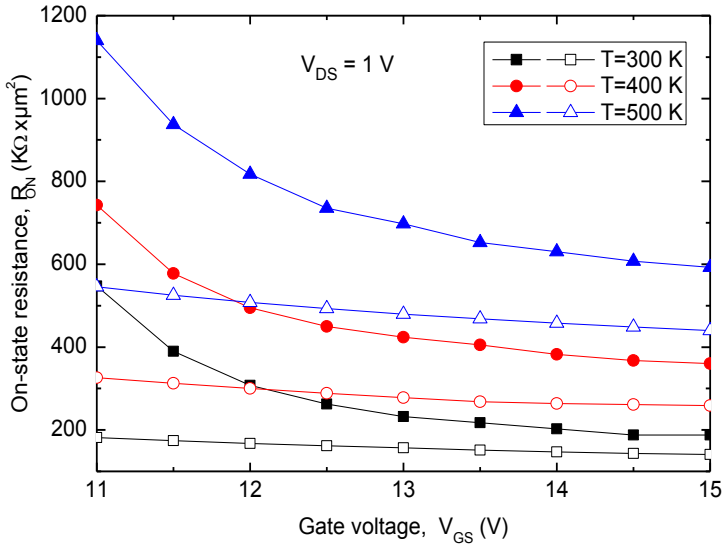

Figure IV.7: R_{ON} as a function of V_{GS} at different temperatures for fresh (open symbols) and defected (solid symbols)device. $D^0_{t,T}$ =10^{14} cm^{-2} eV^{-1}, $D^0_{t,M}$ =2.3×10^{11} cm^{-2} eV^{-1}.

IV.4.2. Deep level traps

By assuming a fixed band edge intercept density $D^0_{t,T}$ =10^{13}cm^{-2} eV^{-1}, figure IV.8 depicts the MOSFETI_D-V_{GS} characteristics in semi-logarithmic scale for two different deep level traps in the mid-gap not exceeding a peak value of 10^{12} cm^{-2} eV^{-1} [31].

In this case, the trap effect mostly occurs at the beginning of the I_D curves determining, once again, an increase in the device threshold voltage.

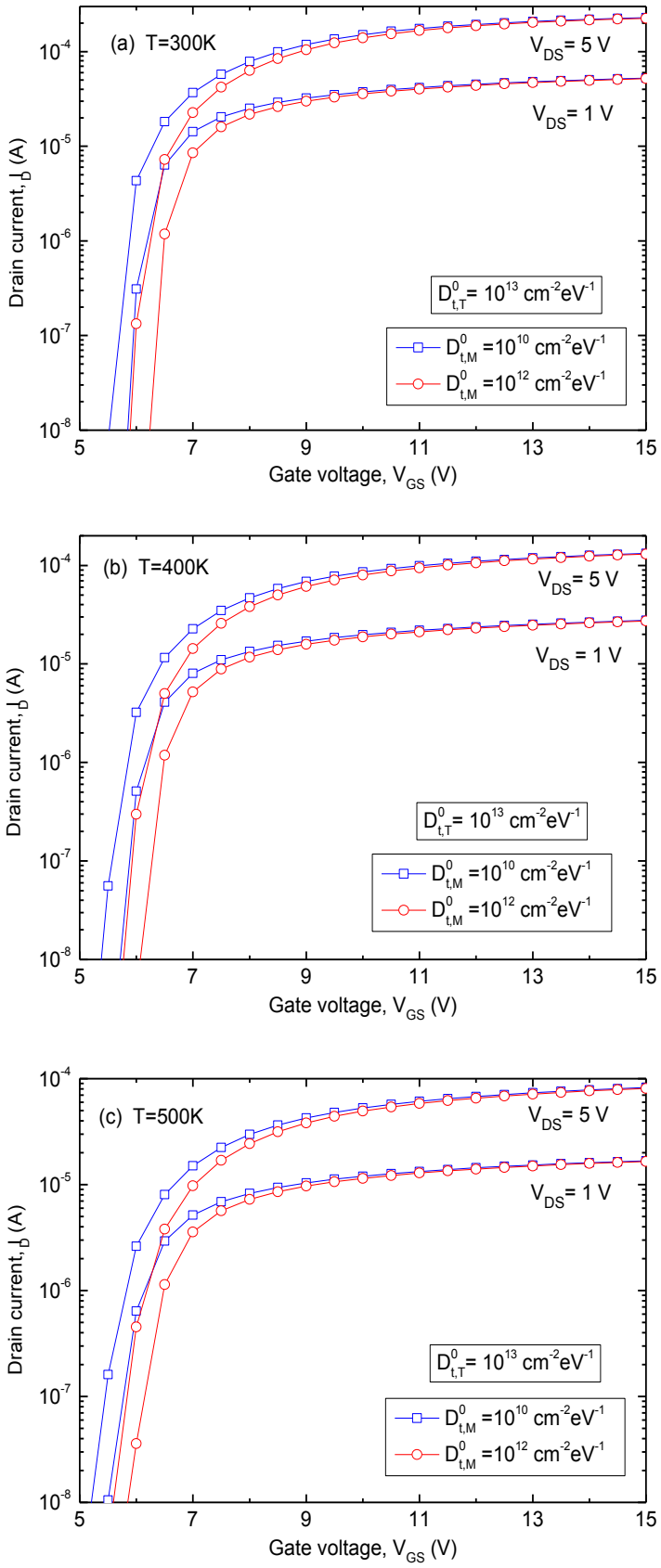

Figure IV.8: $I_D - V_{GS}$ characteristics as a function of the deep-level trap density at (a) T=300K, (b) T=400K, and (c) T=500K.

In other words, since the tail traps contribution has been introduced, the effect of the trapped charge in the deep level traps on the slope of the I_D curves in figure IV.8 is negligible and, in fact, for V_{GS}> 10 V the drain current appears not affected at any temperature. This result is shown in more detail in figure IV.9 by plotting the R_{ON} behaviors as a function of V_{GS} for 11≤ V_{GS}≤ 15 V.

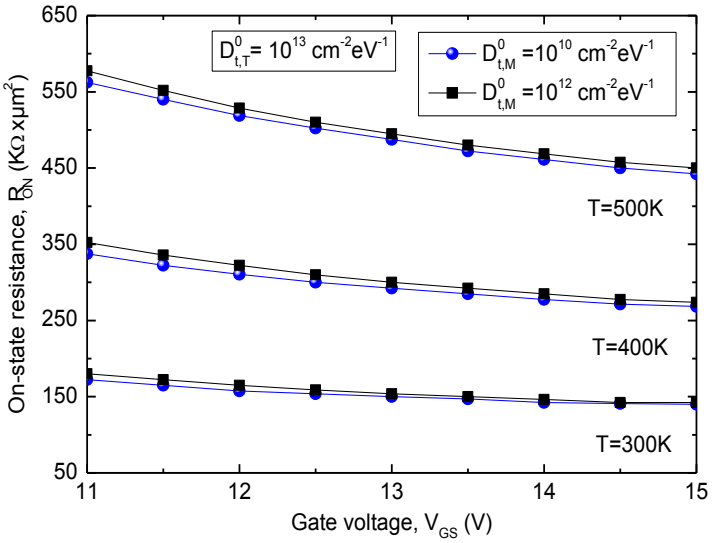

Figure IV.9: R_{ON} as a function of V_{GS} for different deep-level trap densities in the 300-500 K temperature range.V_{DS}=1V. (N_{drift}=3×10^{15}cm^{-3}, N_a=10^{16}cm-3, W_{drift}=1.8μm, μ_{ch}=$1\mu m$)

IV.4.3.Oxide-fixed traps

Moving from the developed analysis on the interface-trapped charges which are related to the defect energy levels inside the 4H-SiC bandgap, in order to determine the effective MOSFET current capabilities, in this section we have involved in the model an oxide-fixed trap effect as shown in Fig. 10.In particular, we have considered a thin film of fixed traps located in the oxide next to theSiO_2/4H-SiC interface with a charge density N_{fix}= 1.3×10^{12} cm^{-2} [28].

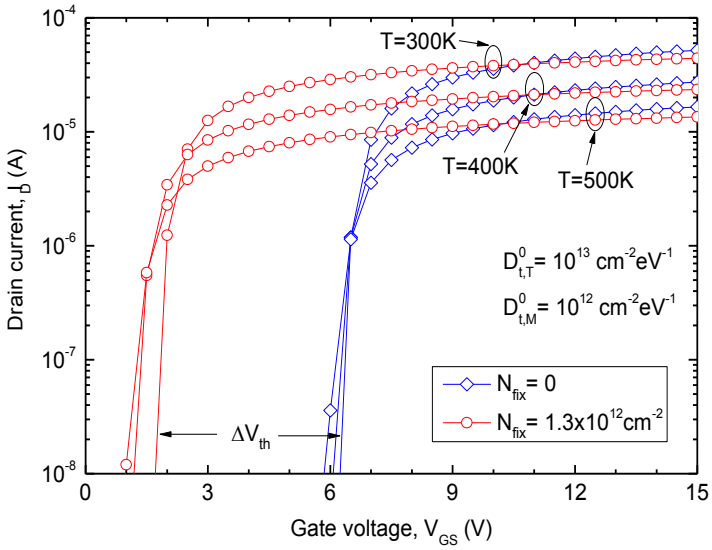

Figure IV.10: $I_D - V_{GS}$ characteristics for an oxide-fixed trap density at different temperatures.V_{DS} = 1 V. (N_{drift}=3×10^{15}cm^{-3}, N_a=10^{16}cm-3, W_{drift}=1.8µm, μ_{ch}=1μm)

In figure IV.10 the oxide-fixed traps, which have a density strictly depends on the 4H-SiC surface oxidation process, became scattering centers that influence the device threshold voltage as shown in figure IV.11 Here, the carrier mobility degradation in the inversion layer is also reported.

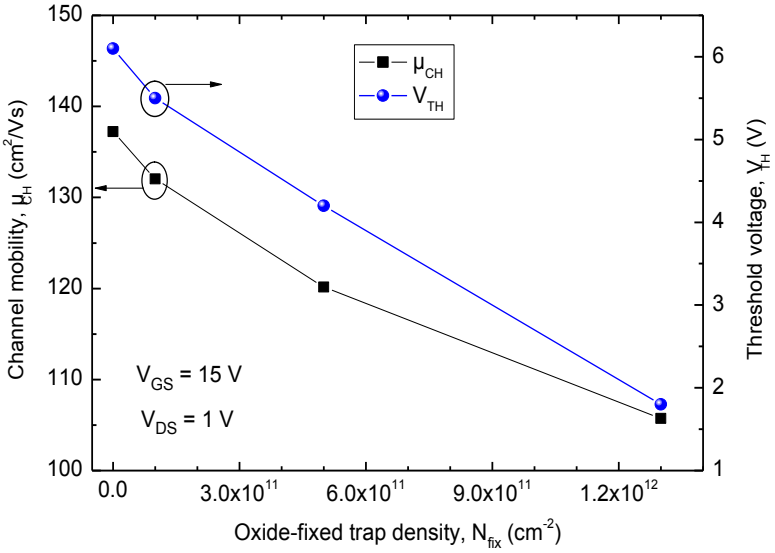

Figure IV.11: Channel mobility and device threshold voltage as a function of the oxide-fixed trap density at room temperature. (N_{drift}=3×10^{15}cm^{-3}, N_a=10^{16}cm-3, W_{drift}=1.8µm)

From figure IV.11, it is clear that the MOSFET threshold voltage significantly decreases in presence of an explicit oxide fixed trap density. These centers, in fact, by acting as positive charges produce a band bending at the semiconductor interface even without the application of a positive bias voltage at the gate contact. In other words, the band bending for a p-type MOSFET tends to induce a depletion region (channel region) before the V_{GS} bias is applied. This effect obviously reduces the device threshold voltage at any operation temperature. In addition, due to the Coulombic scattering phenomena [33], the effective carrier mobility in the inversion layer is degraded as well.

Finally, the comparison of the defected device in figure IV.10 ($D_{t,T}^{0}$ =10^{13} cm^{-2} eV^{-1}, $D_{t,M}^{0}$ =10^{12} cm^{-2} eV^{-1}, and N_{fix} = 1.3×10^{12} cm^{-2})and the fresh one in figure IV.3 in terms of R_{ON} at different temperatures is shown in figure IV.12.

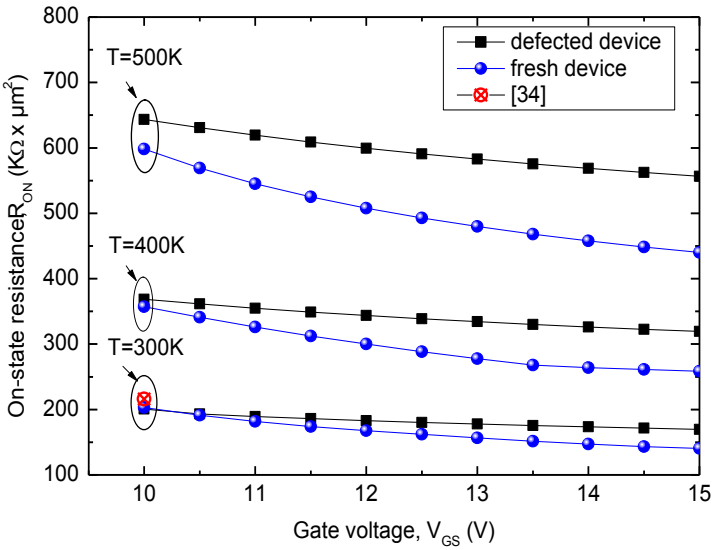

Figure IV.12: R_{ON} behaviors as a function of V_{GS} at different temperatures.
(N_{drift}=3×$10^{15}$$cm^{-3}$, N_a=10^{16}cm-3, W_{drift}=1.8μm, μ_{ch}=$1\mu m$, V_{DS}=1V)

Here, the datasheet value R_{ON}= 216 kΩ×μm² for a Si-based commercial MOSFET rated for 150 V at V_{GS} = 10 V and T = 300 K is also reported [34].This value is slightly higher than that calculated for the proposed device at the same bias level, i.e. R_{ON} = 200.6 kΩ×μm². In presence of an oxide-fixed trap effect, the R_{ON} behavior tends to increase in the whole explored V_{GS} range, in particular at the higher temperatures that more and more contribute to limit the drain current.

IV.4. Conclusion

In this work, the temperature and carrier-trapping effects on the electrical characteristics of a 4H-SiC MOSFET have been predicted by numerical simulations. A combined model of both defect energy levels inside the 4H-SiC bandgap (tail and deep level traps) and oxide-fixed traps has been considered. The trap density reference values have been assumed referring to literature data. The device features an epilayer thickness of 1.8 μm and it performs a breakdown voltage of 150 V.

Starting from a fresh structure (defect-free) we have calculated an on-state resistance close to 140 kΩ×μm^2(V_{GS} = 10 V, V_{DS} = 1 V, and T = 300 K), which increases up to 200 kΩ×μm^2 for a defected device resulting comparable to that of a commercial Si-based MOSFET rated for the same voltage range. The device threshold voltage and carrier mobility in the channel region decrease as a function of both the temperature and trap density. In particular, the oxide-fixed traps have a severe impact on the V_{th} value.

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CHAPTER 5:

Effect of Non uniform doped P base region and High-k Dielectrics

Chapter5

Effect of Nonuniform doped P base region and High-k Dielectrics

V.1. Introduction

The use of 4H-SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) in photovoltaic module-level applications was investigated [1]–[9] and, in order to respond to the specific design constraints, several physical and geometrical parameters need to be carefully evaluated [10]-[14]. Among these, the p-base region doping profile plays a key role [15]. As a design rule, the more the p-base doping level increases the more the p-base depth can be decreased preserving the safe operation conditions. Nevertheless, a high doping concentration causes a high channel resistance and penalizes the current flow with a negative shifting of the threshold voltage. In the standard manufacturing process, the p-base doping profile is usually ensured by ion implantation techniques [16]-[17]. The end of transistor scaling is imminent as the transistor size approaches tens of nanometers. The physical thickness of the gate oxide has become thinner than the limit for electron tunneling (~2 nm), causing the gate leakage current density, *J*g, to become unacceptably high. Consequently, it is necessary to replace the conventional gate insulator, SiO2, with a high-*k* material for low power consumption.

Besides the scaling of equivalent oxide thickness (EOT) aspect, other technological capability evaluation is preferred to choose between competitive high k materials. [18] Similar to silicon case, by thermal oxidization of the SiC we yield a stoichiometric SiO2, this feature place the SiC material at the summit of wide bandgap semiconductors and makes the SiO2 as preferred gate dielectric. SiO2/SiC MOSFETs performance has been enhanced via diverse nitridation process. However, low channel mobility caused by the high interface state density rest an obstacle in front of their commercialization.[19] further, knowing that an interface electric field is inversely proportional with the

material dielectric constant, SiO2 with dielectric constant of 3.9 compared to a 10 of 4H-SiC cause a 2.5 times high electric field than SiC. This problem necessitates that the device works at an electric field distant underneath the SiC breakdown field to evade the oxide breakdown.[20]. This leads to the non-use of the high breakdown field of SiC _3.0 MV/cm, and lose one of the most important material's features for high-power applications. In addition, as we know, the power MOSFET breakdown voltage scales with the square of the electric field, this fact severely decrease the device's breakdown voltage ability for certain on state resistance. Since the SiO2 proved its limitations, it became necessary to research for a high-k gate oxide with low oxide field that allows MOSFET functioning in close proximity to the SiC breakdown field. Recent researches pay an impressive attention to high-k gate dielectric materials and stacks on SiC including Al2O3,[21] oxidized Ta2Si,[22] SiO2 /TiO2,[23] Gd2O3,[24] SiO2 /HfO2,[25] and AlN.[26], However, high-k/4H-SiC interface Reliability and stability against temperature, interfacial traps and fixed charge defects is one of the greatest issues that must be studied in detail.

The contribution of this work is threefold. First, we provide an investigation of a non-uniform p-base doping concentration in determining the fundamental 4H-SiC MOSFET figure of merits, both in blocking and forward current regime (i.e. blocking voltage, threshold voltage, drain current, and on-state resistance) by means of a detailed numerical simulation study. A comparison with previous results taken from literature is also highlighted. Second, we investigate via numerical simulation the effect of the gate oxide dielectric type on the operation of a 4H-SiC MOSFET designed for low voltage ratings (BVDS = 150 V) . The gate dieliectrics compared are SiO_2, Si_3N_4, AlN, Al_2O_3, Y_2O_3 and HfO_2. The parameters evaluated in this study are: Channel mobility (µch), ON state resistance (R_{ON}), leakage gate current, oxide electric field, threshold voltage (V_{th}), subthreshold swing (SS), transconductance (g_m) and threshold shift (ΔV_{th}). Third, to the best of our knowledge, this is the first attempt to investigate the reliability behavior of low breakdown 4H-SiC MOSFET using various gate oxide dielectric type, Si_3N_4, AlN, Al_2O_3, Y_2O_3 and HfO_2, under high temperature and carrier-trapping conditions. As the HfO2 is the promising material view these performances, we investigate the effect of oxide thickness and the fixed traps effect on the electrical characteristics of the MOSFET, in addition, by benefit of high ΔEC of Al_2O_3 we propose this oxide as an interfacial thin layer to reduce the gate leakage current, interfacial Al_2O_3 with ε_{OX}=9.3 keep almost the same on

state performance rather than SiO_2. The numerical simulations are performed using SILVACO-ATLAS simulator [27].

V.2. MOSFET structure

The schematic cross-section of the considered vertical n-channel 4H-SiC MOSFET single-cell is shown in figure V.1 The different geometrical parameters are labeled as follows: W_{cell} is the cell width, W_G is the gate contact width, L_{ch} is the device channel length, WJ is the distance between the base regions, X_{N+} is the n^+-source junction depth, X_P is the p-base junction depth, W_{drift} is the n-drift region thickness, W'_{drift} is the base-to-substrate distance, and W_{sub} is the starting substrate thickness. The source contact shorts the source and base regions to prevent the switch-on of the parasitic substrate(n+)–epilayer(n)– base(p)–source(n+) bipolar junction transistor. The reference geometrical and doping parameters used during the simulations are summarized in Table V.1.

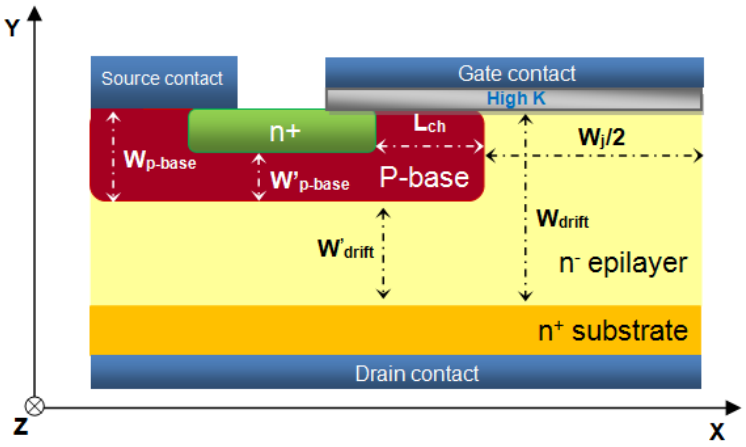

Figure V.1: Cross-sectional view of the 4H-SiC MOSFET. (The drawing is not to scale)

From Table V.1, the distance between the n+- source region and the n-epilayer (i.e., X_P–X_{N+}) is 0.8 µm. The epilayer thickness ensures a BV_{DS} value close to 150 V. Although simplified for simulation purposes, the proposed structure is in principle compatible with a manufacturing process based on doping by ion implantation [28-30]. The physical parameters values of various dielectric layer materials used are summarized in Table V.2.

Table V.1: MOSFET reference parameters

Design parameters	**Values**
oxide thickness, T_{OX} (μm)	0.02
Source thickness, X_{N+} (μm)	0.5
Channel length, L_{ch} (μm)	1
Base junction depth, X_P (μm)	1.3
Base-to-base distance, W_J (μm)	7
Epilayer thickness, W_{drift} (μm)	1.8
Base-to-substrate distance, W_{drift} (μm)	0.5
Substrate thickness, W_{sub} (μm)	100
Gate contact width, W_G (μm)	9.4
Cell width, W_{cell} (μm)	15
N+-source doping, N_D (cm^{-3})	1×10^{18}
P-base doping, N_A (cm^{-3})	1×10^{17}
N-$_{drift}$ doping, N_{drift} (cm^{-3})	1×10^{15}
N^+-substrate doping, N_{sub} (cm^{-3})	1×10^{19}

Table V.2: physical properties of various dielectric layer materials.

Layer	Parameter	Designation	Value	References
SiO_2	Eg (eV)	Band gap	9	[31]
	ε_{OX}	Relative permittivity	3.9	[31]
	ΔE_C (eV)	conduction band offset	2.7	[31]
Si_3N_4	Eg (eV)	Band gap	5.3	[31]
	ε_{OX}	Relative permittivity	7.5	[31]
	ΔE_C (eV)	conduction band offset	/	[31]
AlN	Eg (eV)	Band gap	6.23	[32]
	ε_{OX}	Relative permittivity	8.5	[32]
	ΔE_C (eV)	conduction band offset	1.7	[32]
Al_2O_3	Eg (eV)	Band gap	8.8	[33]
	ε_{OX}	Relative permittivity	9.3	[33]
	ΔE_C (eV)	conduction band offset	1.7	[33]
Y_2O_3	Eg (eV)	Band gap	5.6	[34]
	ε_{OX}	Relative permittivity	15	[34]
	ΔE_C (eV)	conduction band offset	/	[34]
HfO_2	Eg (eV)	Band gap	5.9	[35]
	ε_{OX}	Relative permittivity	22	[35]
	ΔE_C (eV)	conduction band offset	0.9	[35]
electrode contact (Al)	d (µm)	Thickness	0.3	[36]
	Φ_{Al} (eV)	Work function	4.26	[36]
Gate Aluminum	d (µm)	Thickness	0.3	[36]
	Φ_{Al} (eV)	Work function	4.26	[36]

V.3. Results and discussion

V.3.1. Test of simulations setup

The described simulation setup permits a reliable prediction of the device behavior; this credibility is examined by comparison with experimental data. By considering the same topology of figure V.1, we simulate via TCAD atlas SILVACO a commercial 900-V SiC MOSFET with and without interfacial traps [37] In order to circumvent the lack of information about geometry and doping levels, similar to ,[38]. By taking a drift-region entirely depleted before the breakdown occurs (punch-through condition), the BV_{DS} prediction expression is as follows [39]:

$$BV_{DS} = E_{pn}^{crit} W_{drift} - \frac{qN_{drift} W_{drift}^2}{2\varepsilon_{sc}} \; ; \; W_{drift} \leq \varepsilon_{sc} E_{pn}^{crit} q^{-1} N_{drift}^{-1} \qquad (1)$$

where E_{pn}^{crit} represent the critical electric field alongside the p-base/n-drift junction, ε_{sc} and q denote, respectively, the semiconductor permittivity and the electric charge, and N_{drift} refers to drift region doping concentration. By taking a 4H-SiC mosfet with N_{drift} =3×10^{15} and W_{drift}=10 μm, the breakdown voltage B_{VDS} reach a value of 900V [37]. figure V.2 depicts the On state resistance as function of drain voltage for the investigated MOSFET compared to experimental results. From figure V.2 the measurement and numerical simulations of the defected device ($D_{it,TA}$=10^{13}cm^{-2}, $D_{iT\ mA}$=2.310^{11}cm^{-2}) illustrate a good agreement

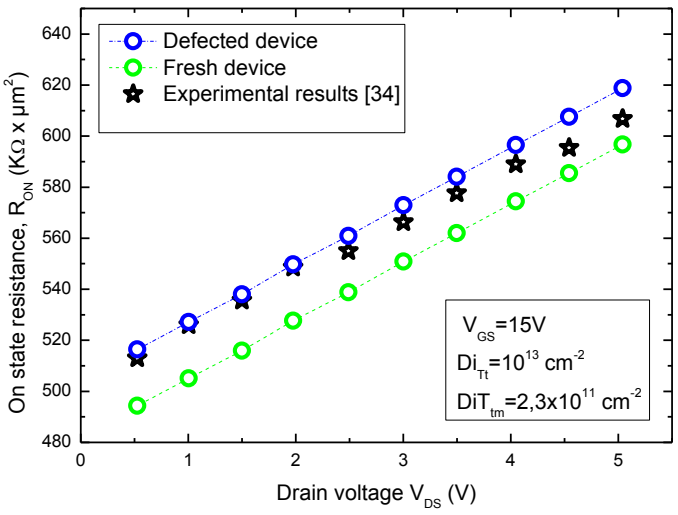

Figure V.2: R_{ON} as function of drain voltage for a commercial device and numerical simulations. (N_{drift}=1×10^{15}cm^{-3}, N_a=10^{17}cm-3, W_{drift}=1.8µm, μ_{ch}=1μm, V_{DS}=1V)

V.3.2. Impact of a non-uniform p-base doping concentration

The drain current-voltage (I_{DS}-V_{DS}) curve of the proposed device with a non-uniform doping concentration in the base region is shown in figure V.3. Here, the I_{DS}-V_{DS} characteristics calculated at the same gate bias voltage (V_{GS} = 15 V) for a conventional design with different values of N_a are also reported for comparison.

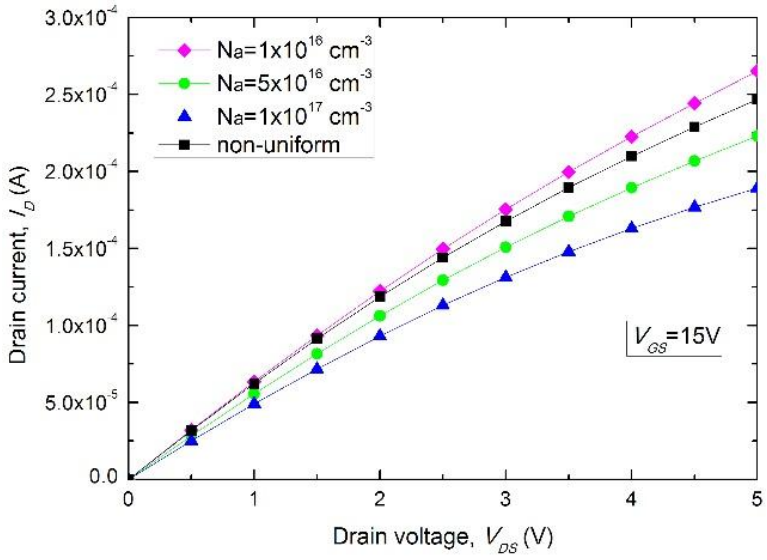

Figure V.3: $I_D - V_{DS}$ characteristics for different designs in terms of the base doping at T = 300K.

As we can see from this figure, the proposed device with non uniform doping profile in the base region shows a drain current behavior close to that achieved for a MOSFET where a uniform concentration of $N_a = 1\times10^{16}$ cm^{-3} is assumed in the base region, especially for low V_{DS} values in the limit of 3V. This result is mainly due to the low doping concentration in the channel region which allows an effective inversion regime. In fact, the more N_a increases the more the forward current I_D tends to be penalized.

The MOSFET $I_D - V_{GS}$ curves plotted in figure V.4 for V_{DS} = 1 V show the variation of the device threshold voltage fixing a reference value of I_D equal to 10 nA.

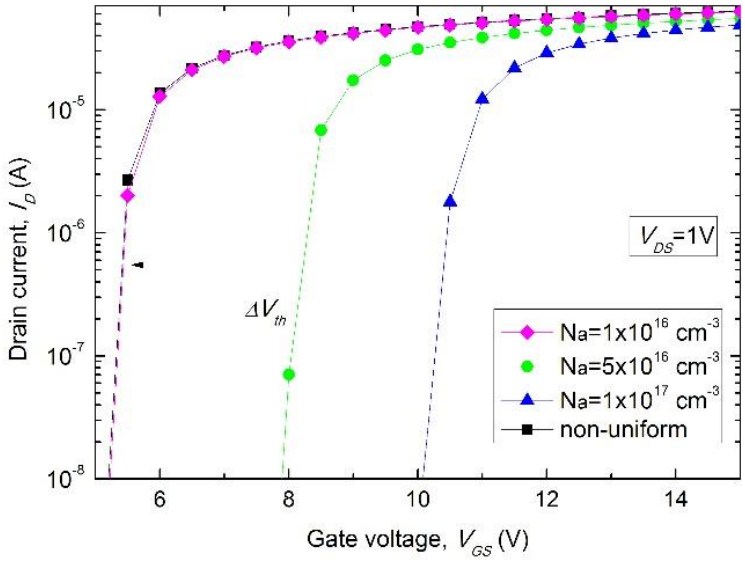

Figure V.4: $I_D - V_{GS}$ curves for different designs in terms of the base doping for V_{DS} = 1 V.

It is remarkable that the proposed device exhibits a low threshold voltage close to 5.5 V which tends to increase as the uniform p-base doping concentration increases.

By assuming in figure V.1 a cell width of 15 µm and therefore a device active area of 15 µm^2, the calculated on-state resistance behaviors are shown in figure V.5.

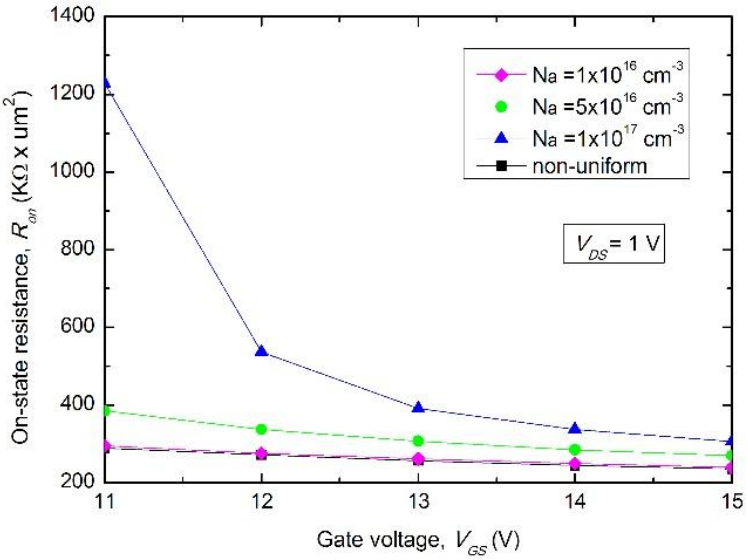

Figure V.5: On-state resistance as a function of VGS.

As expected, the effective device R_{on} tends to increase with the p-base doping concentration, especially for low values of V_{GS}. For example, for VGS = 11 V, we calculate Ron close to 300 kΩ×µm^2 using the non-uniform p-doping profile while R_{on} is about 1 MΩ×µm^2 for Na = 1×1017 cm^{-3}. In addition, a comparison between the obtained results in terms of R_{on} and those taken from literature in [10] for a similar device structure, which

presents $N_a = 1\times10^{17}$ cm^{-3}, allows to highlight a performance improvement on the order of 20%.

Finally, it is important to note that the non-uniform p-base doping profile considered in this work has only a limited impact in determining the MOSFET blocking voltage characteristics as shown in figure V.6. In fact, the device always withstands a drain voltage around 150 V before the breakdown of the p-base/n-drift junction occurs. This result is also confirmed in [10].

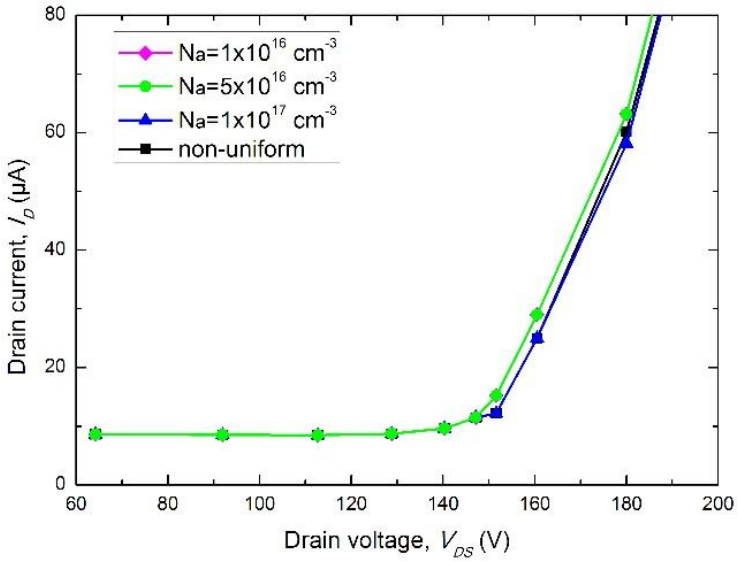

Figure V.6: MOSFET blocking voltage behavior.

The blocking voltage behaviors have been calculated with the MOSFET in the firm off-state and grounded source.

V.3.3. High k/4H-SiC MOSFET analysis

Among physical parameters that manage the threshold voltage value (V_{th}), thickness and Type of the oxide, interface charge density and the fixed charge in the oxide are some of the key parameters. For a fixed oxide physical thickness the threshold voltage decreases with increasing the oxide permittivity [37]. It is worthy to note, that for a decreased SiO_2 thickness with high-k dielectric *EOT*, we get a slight threshold voltage variation and a analogous *I-V* characteristics.

figure V.7 depicts the depict the $I_{DS} - V_{GS}$ curves of SiO_2 (20 nm) comparing with various high-k material with a fixed gate dielectric thickness for 300k and 423k. The threshold voltages values for 300k were 4.5; 4.35, 4.25, 4.2, 4.1 and 3.9 V for SiO_2, Si_3N_4, AlN, Al_2O_3, Y_2O_3 and HfO_2, from figure V.7, the more the oxide dielectric constant increase the threshold voltage decrease, this is due to the improved inversion charge density.

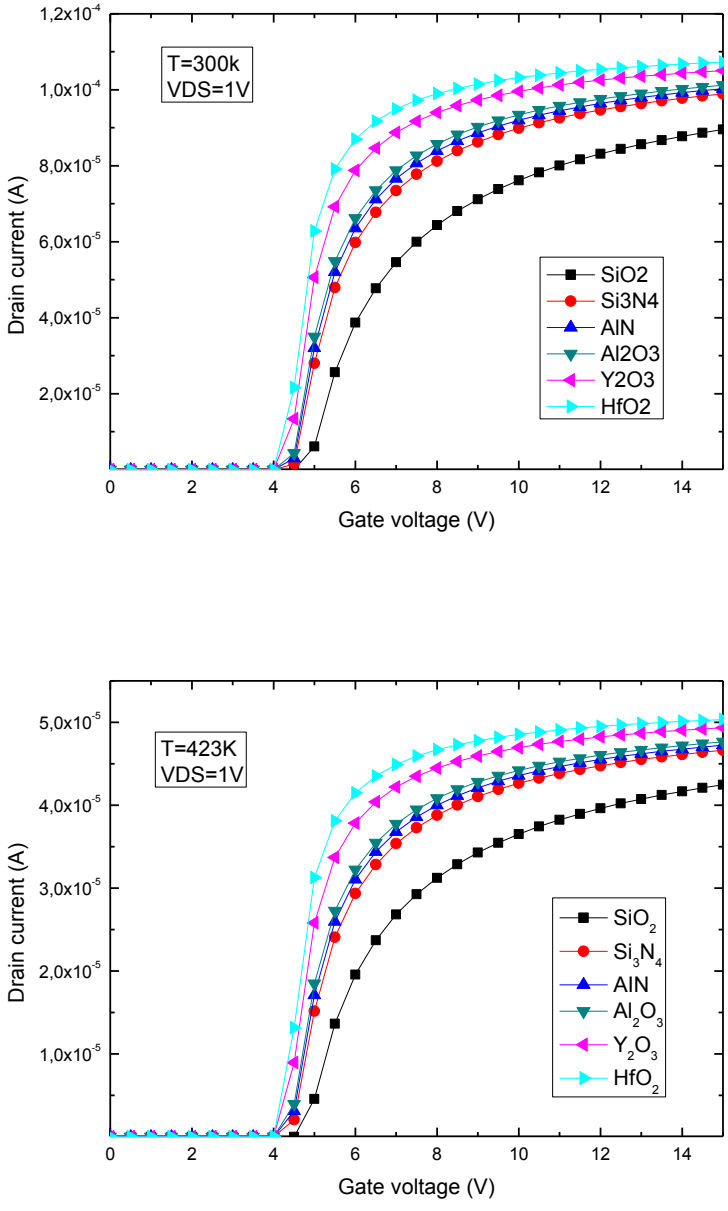

Figure V.7: $I_D - V_{GS}$ curves for the device in Table V.1 at T = 300 K, T = 423 K.

Besides, As estimated, when increasing temperature the drain current diminish severely. This is due mainly to the inversion layer carrier mobility dependence on temperature, along with the overall on-state resistance raise. The more the temperature increase the more the Phonon scattering mobility decreases, this fact is due to the rise of phonon numbers with temperature. Higher temperatures cause a screening of filled traps which improve the mobility affected by coulombic scattering mechanism. The Surface roughness is independent of T [37,40].

A further significant parameter is the Transconductance. figure V.8 depicts the transconductance versus sub threshold swing for various gate dielectric materials at temperatures sweep from 300 to 500 K.

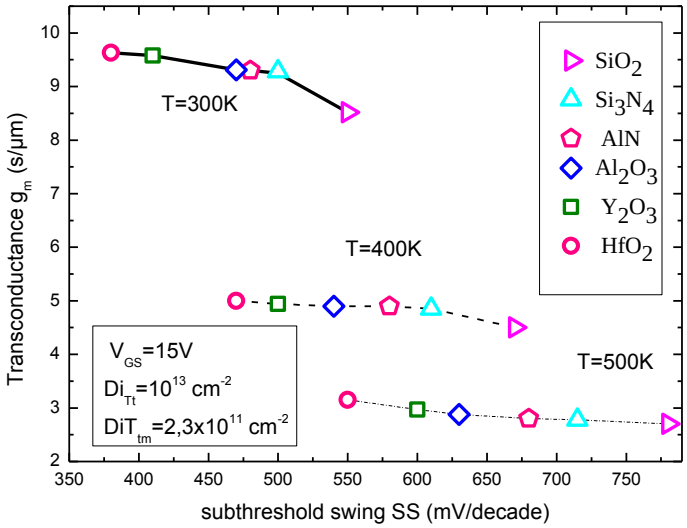

Figure V.8: Transconductance in function of sub threshold swing at temperatures from 300 K to 500 K.

the high-k dielectric transconductance is obviously increased when compared with SiO_2. From figure V.8 the transconductance decrease severely when increasing temperature this is due to influence on carrier lifetime, the intrinsic carrier concentration (n_i) and the mobility (μ). In general, variation in device temperature affects transconductance, V_{th}, sub threshold swing and $R_{on,sp}$ which in turn affects the switching behavior of the device. High transconductance and low sub threshold swing is considered for HfO_2 at any given

temperature. In contrast, SiO_2 reveal lower transconductance and higher sub threshold swing compared to other oxide materials.

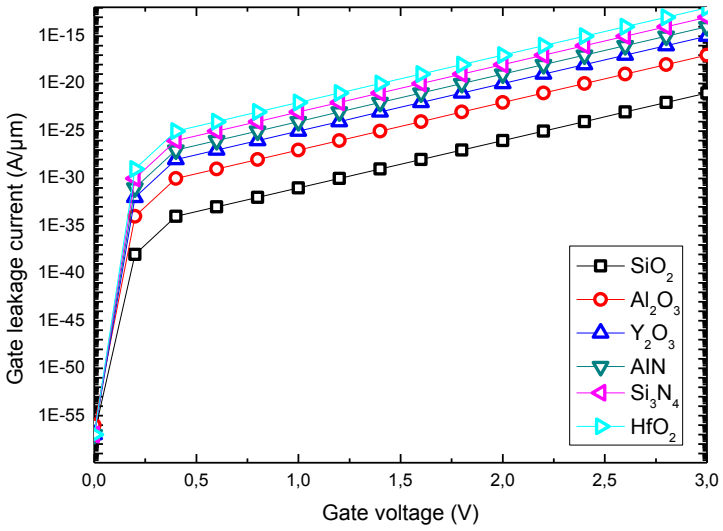

Figure V.9: Gate leakage current versus gate voltage in subthreshold region.

High gate leakage current is an inappropriate MOSFET operation feature that leads to MOSFET premature breakdown. Fowler-Nordheim tunneling mechanism, non local tunneling at dielectric-dielectric interface and dielectric- SiC interface are used to describe the current through the gate Assuming high temperature and electric fields. figure V.9 depicts the off state leakage current as function of V_{GS} values low than V_{th}. HfO_2 (ΔE_C=0.9 eV ALCVD) shows noticeably higher leakage current, SiO_2 (ΔE_C= 2.2 eV Thermal oxidation *)* and Al_2O_3 (ΔE_C= 1.7 eV ALCVD*)* show a decreased leakage current when compared to other dielectrics. The improved SiO_2 and Al_2O_3 leakage currents are due mainly to the conduction band offset difference. Take advantage of the less discontinuity variation in conduction band between SiO_2, Al_2O_3 oxides and 4H-SiC, an augment in oxide thickness diminish more the leakage current. Nevertheless, this fact, cause a high fixed charge density that affect transconductance and V_{th}, Even though HfO_2 has exhibited superior characteristics, a partial compromise on transconductance and sub threshold swing is required by inserting an interfacial layer with large band offset in order to address the high leakage currents that come with high-k dielectrics.

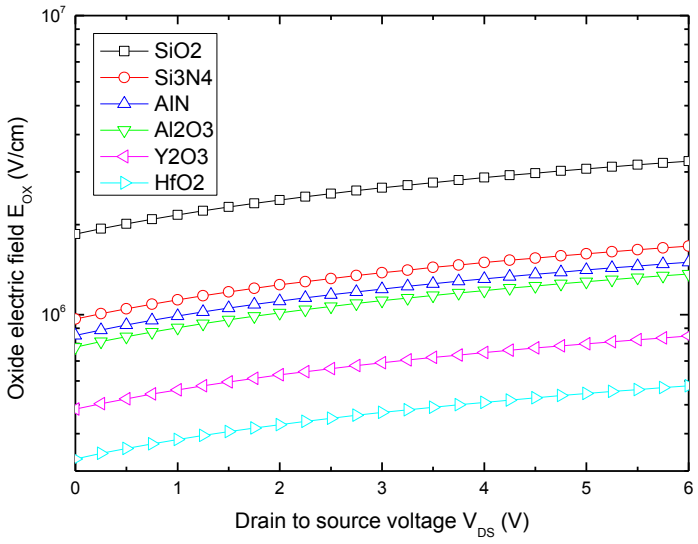

Figure V.10: Comparison of electric fields in the dielectric materials

figure V.10 depicts the oxide electric field variation as function of drain voltage for various gate dielectrics (SiO_2, Si_3N_4, AlN, Al_2O_3, Y_2O_3 and HfO_2). It is obvious from figure V.10 that SiO_2 has a much higher electric field when compared with other dielectrics. HfO_2 has the lowest electric field at any drain voltage. This could be due to the effective permittivity of the dielectric being much higher as compared to other dielectrics. Low electric field decreases the electric field stress via minimizing the defect density accumulation over time. However, the reduction in the electric field by increasing the permittivity value is consistent with high leakage currents observed in figure V.9.

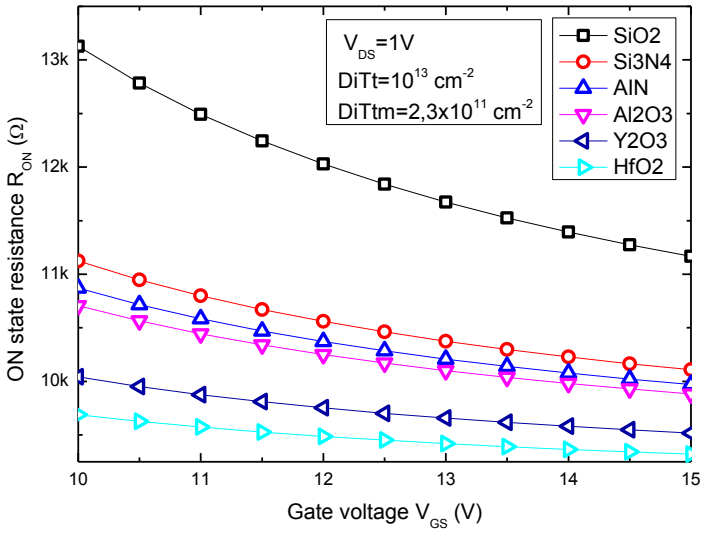

Figure V.11: On state resistance of various gate oxide dielectrics as function of gate voltage

The R_{ON} behaviors as a function of V_{GS} for a various gate dielectric material are shown in figure V.11. The R_{ON} in the case of SiO_2 is a V_{GS} dependent and exhibits a high value of (13KΩ) at (V_{GS}=10V), as a consequence of the mobility degradation induced by interfacial traps [37]. Dielectrics with high permittivity show a weak dependence of V_{GS}, and a decreased R_{ON} value, this is due to the increase of the inversion charge caused by the high permittivity value which enhances the conductivity in the channel region. The decrease of R_{ON} with increase of V_{GS} is due to the increased screening of traps caused by the increase of mobile carriers, this fact leads to improve the MOSFET output current and limit the R_{ON} rise.

V.3.4. Oxide/4H-SiC interfacial traps Effect

The focal point in this section is the oxide-4H-SiC interface with an emphasis on the channel mobility degradation and threshold voltage instability. Several investigations carried out of the interface traps density effect on channel mobility [37]. Among techniques that improve the mobility, Post-oxidation treatment is one of the effective ways that decrease the interface traps [41].

A. Tail interface traps effect

In this section, we investigate the tail traps concentration influence on the device threshold voltage, channel mobility, and R_{ON} for different gate oxide dielectrics.

The Fermi level progressively shifts in the bandgap upper half for a forward biasing. Figure 12-a depicts the channel mobility variation for device with various gate dielectrics as function of tail interface trap density.

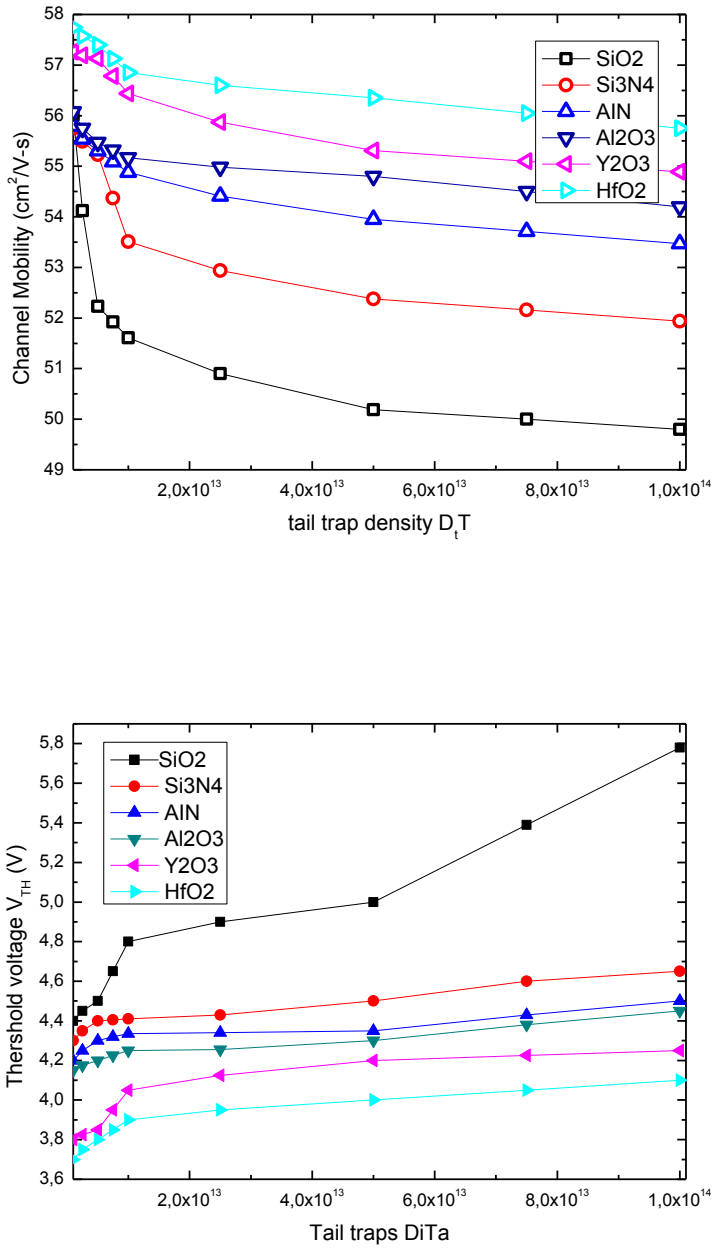

Figure V.12: tail traps $D_{iT,TA}$ effect on a)μ_{ch} and b)V_{th}

Earlier studies report that channel mobility value is about 30-40 cm^2/V^{-s}. Even if a values up to 165 cm^2/Vs has been stated. [48].

Earlier studies report that the inversion layer mobility is affected further at the first 5 nm below the interface. In this study the extracted mobility covert 100 nm in the channel region underneath the interface [49]. The extracted mobility value is approximately 49.8 cm^2/V^{-s} for SiO_2/SiC interface compared to 51.94, 53.47, 54.75, 54.89, and 55.75 cm^2/V^{-s} for Si_3N_4, AiN, Al_2O_3, Y_2O_3 and HfO_2 respectively, for $Dit_{,TA}$=$10^{14}cm^{-2}$ and a similar channel doping (1×10^{17} cm^{-3}) At any given trap concentration the extracted mobility for diverse distances below the interface (2 nm, 10 nm, and 50 nm) for the SiO_2-SiC interface show a decreased value compared to other dielectrics. This fact is due to the ability of acceptor defect states to trap a high number of electrons from the inversion layer when positive V_{GS} bais is applied, this fact weak the transport mechanisms. In the other side, the immunity of high k materials against the trapping effect is due to the high permittivity which assures a high charge concentration in the inversion layer make the effect of acceptor traps not clear. HfO_2 interface consistently shows at least 1.2 times better mobility than SiO_2 at $Dit_{,TA}$=$10^{14}cm^{-2}$.

figure V.12 depicts the variation of threshold voltage as function of tail traps concentration density for a various gate dielectric, From figure V.6, V_{th} of SiO_2 tends to increase harshly as the tail traps increases with a positive shift of ΔV_{th}=1.38V. this is due mainly to the Coulomb scattering phenomena of mobile charges occurred when increasing tail traps density, which shift positively the threshold voltage. MOSFET used a gate dielectric with high permittivity show a good immunity against the interfacial traps effect, the threshold voltage shift is about 0.35, 0.3, 0.3, 0.45 and 0.4 V for Si_3N_4, AlN, Al_2O_3, Y_2O_3 and HfO_2, respectively, this fact is due to the improved inversion charge caused by the elevated permittivity value of such materials.

B. Deep level traps

figure V.14 depicts threshold voltage variation as function of deep-level traps (not exceeding a peak value of 10^{12} cm^{-2} eV^{-1} [50] for MOSFET with various gate dielectric materials. During simulations we assume a band edge intercept with fixed density ($D_{0\ t,T}$ = 10^{13} cm^{-2} eV^{-1}). Due to the position of the deep-level traps situated in the midgap, this traps affect the device just at the start of the I_{DS} curves which shift positively the threshold voltage by trapping electron from inversion layer. In other words, by introducing the tail traps contribution in the model, the influence of the deep-level traps on the slope of the I_{DS} curves will be vanished and in turn, there is no effect on drain current. As expected the 4H-SiC MOSFET with high k material exhibit a good immunity against the deep level traps effect and show a low threshold voltage positive shift of ΔV_{th}= 0.2,0 .3, 0.23, 0.4, 0.3 V for Si_3N_4, AlN, Al_2O_3,Y_2O_3, HfO_2, respectively, when compared with SiO_2 gate oxide ΔV_{th}=0.35V.

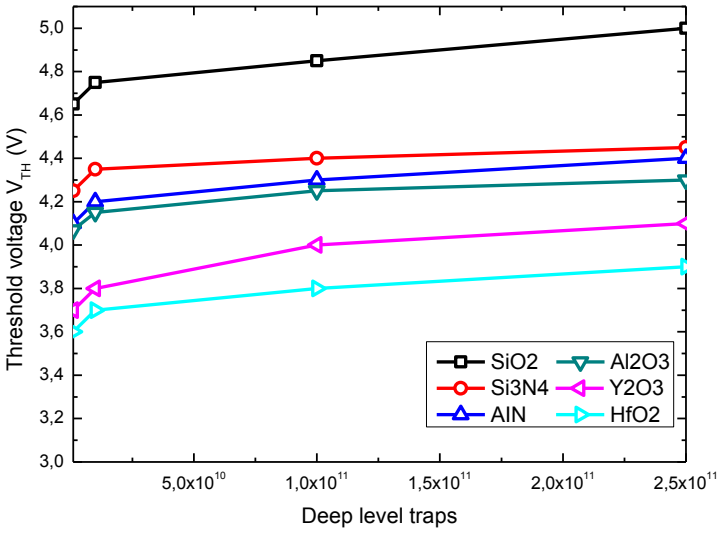

Figure V.14: Threshold voltage as function of deep level traps

V.3.5. Temperature effect

The effect of temperature on the channel mobility of 4H-SiC MOSFET with various gate dielectric materials is shown in figure V.15 From this figure the channel mobility diminish when temperature rise, This effect is due to the occurrence of Phonon scattering mechanism whose mobility decreases as the temperature is raised, because the phonon numbers increase with T, in high k material the augmentation of inversion charge caused by the high value of permittivity help in screening the traps and reduce the Coulombic scattering mechanism mobility at low temperatures [51].

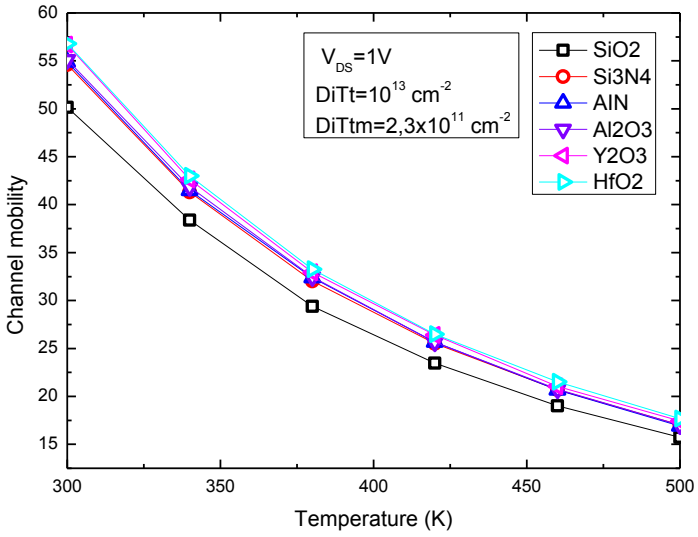

Figure V.15: Channel mobility curve versus temperature.

The effect of temperature on the device on state resistance is depicted in figure V.16. The increased temperature limits the current components which originate in the inversion layer and drift layer, wich dramatically increase the R_{ON}, and this is linked to the Phonon scattering mechanism. And Coulomb scattering phenomena, that due to the filled traps of mobile charges [52]. The gate dielectric with high k show R_{ON} value of 10.11K, 9.7K, 9.9K, 9.5K, and 9.3K for Si_3N_4, AlN, Al_2O_3,Y_2O_3, HfO_2, respectively, when compared with SiO_2 (11.17K),this fact, is due to the role of high permittivity that reduce the columbic scattering via screening the traps. [51].

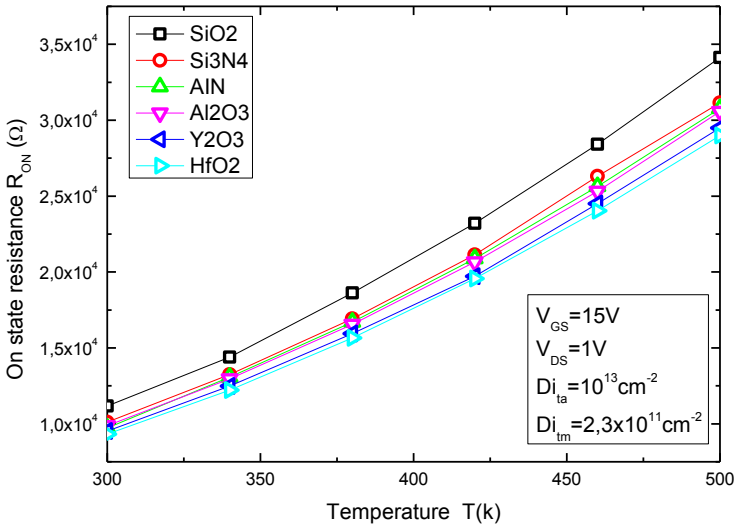

Figure V.16: R_{ON} versus temperature.

Besides, The more the temperature increases, the more the number of filled traps decreases hence the Coulomb scattering decrease and the only mechanism that reduce the mobility and increase the R_{ON} at high temperature is the phonon scattering [52].

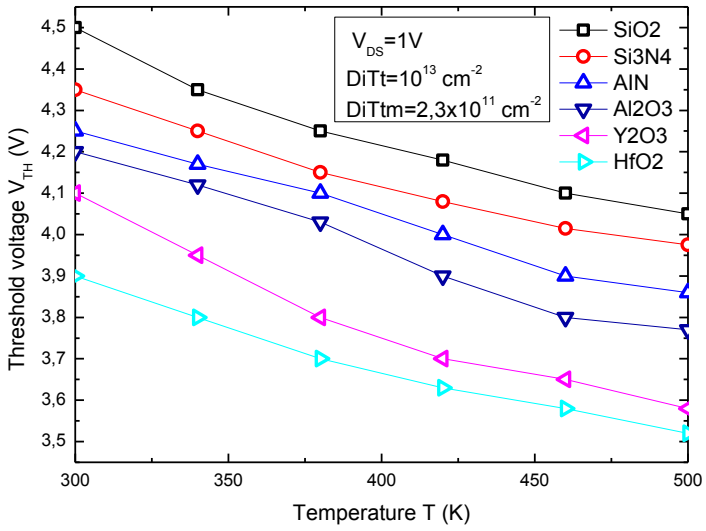

Figure V.17: V_{th} in function of temperature.

figure V.17 depicts the threshold voltage of the DMOSFET with various gate dielectric , V_{th} tends to decrease with increasing temperature, at room temperature , the filled traps

cause Coulomb scattering phenomena of mobile charges that determine in turn a reduced drain current and a positive shift of the threshold voltage, however the more the temperature increases, the more the number of filled traps decreases; hence V_{th} decreases. The high k gate dielectric show a reduced V_{th} of 4.35, 4.25, 4.2, 4.1, and 3.9V ,respectively, for (Si_3N_4, AlN, Al_2O_3,Y_2O_3, HfO_2) respectively at 300k when compared to SiO_2 (4,5V). The high permittivity play a crucial role in reducing the V_{th}, throw improving the inversion charge.

V.3.6. Effect of fixed charge and thickness in HfO_2

HfO_2 shows good performance compared with other insulators in this work. HfO_2 have the highest k which makes it ideal for 4H-SiC application. An improved oxide/4H-SiC interface must exhibits slight interfacial trap sites, low defect density and band engineering possibility. Moving from the developed analysis on the interface-trapped charges which are related to the defect energy levels inside the 4H-SiC bandgap, in order to determine the effective MOSFET current capability, in this section we have involved in the model an oxide-fixed trap effect. In particular, we have considered a thin film of negative and positive fixed traps located in the oxide next to the SiO_2/ 4H-SiC interface with a charge density varied from -3×10^{12} to 3×10^{12} cm^{-2} . figure V.18 depicts the I_{DS}-V_{GS} transfer characteristics variation for different charge density concentration.

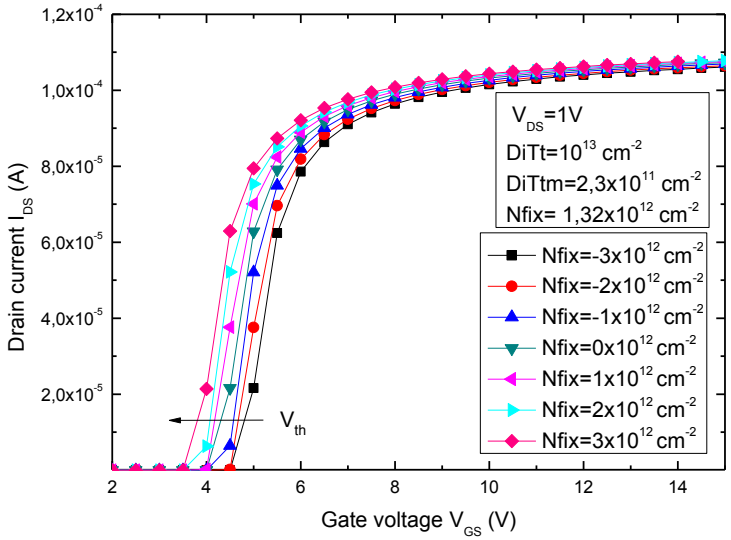

Figure V.18: $I_D - V_{GS}$ curves for HfO_2/4H-SiC MOSFET varying N_{fix} from 3×10^{12} cm^{-2} to $3\times10^{12}cm^{-2}$

The transfer characteristics curve moves toward positive for negative fixed charge, while the opposite trend is observed for a positive fixed charge. The oxide-fixed traps, which have a density strictly dependent on the 4H-SiC surface oxidation process, became scattering centers that influence the device threshold voltage V_{th} changes from 3.75 to 4.3 V for a negative fixed charge changing from 0 to -3×10^{12}. The positive charge leads to a negative *V*th shift. When the density of the fixed charge is positive and changes from 1×10^{12} to 3×10^{12} , V_{th} changes from 3.7 to 3.35 V [52]. The negative charge in the oxide reduces the electron density that accumulates at the interface between 4H-SiC and HfO_2. This makes the MOSFET requiring a more positive voltage to turn on, while the positive charge in the oxide acting as positive charges produce a band bending at the semiconductor interface even without the application of a positive bias voltage at the gate contact [53,54]. In other words, the band bending for a p-type MOSFET tends to induce a depletion region (channel region) before *V*GS is applied. This effect obviously reduces V_{th} at any operation temperature. These centers, in fact, by In addition, due to the Coulombic scattering [55], the effective carrier mobility in the inversion layer is degraded as well this fact not affect the current because of the improved inversion charge.

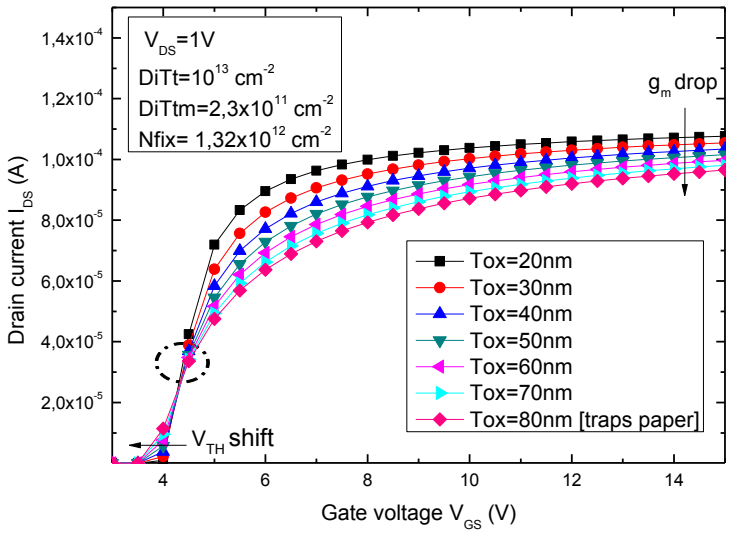

Figure V.19: $I_D - V_{GS}$ curves for HfO_2/4H-SiC MOSFET varying T_{OX} from 20nm to 80nm.

figure V.19 depicts the transfer characteristics variation as function of HfO_2 thickness, by varying T_{OX} from 20 to 80 nm V_{th} decreases slightly from 3.75 to 3.4 V, which is a negative shift. The transconductance decreases when increasing the thickness this is mainly due to the decrease in mobility affected by the high fixed traps density in the oxide. On the other hand, sub threshold swing not affected by varying thickness.

V.3.7. Trap distribution model at HfO_2/4H-SiC interface

As results, figure V.20 resume the relationship between trapping effects and main device electrical characteristics deduced from the predictive model finding [56].

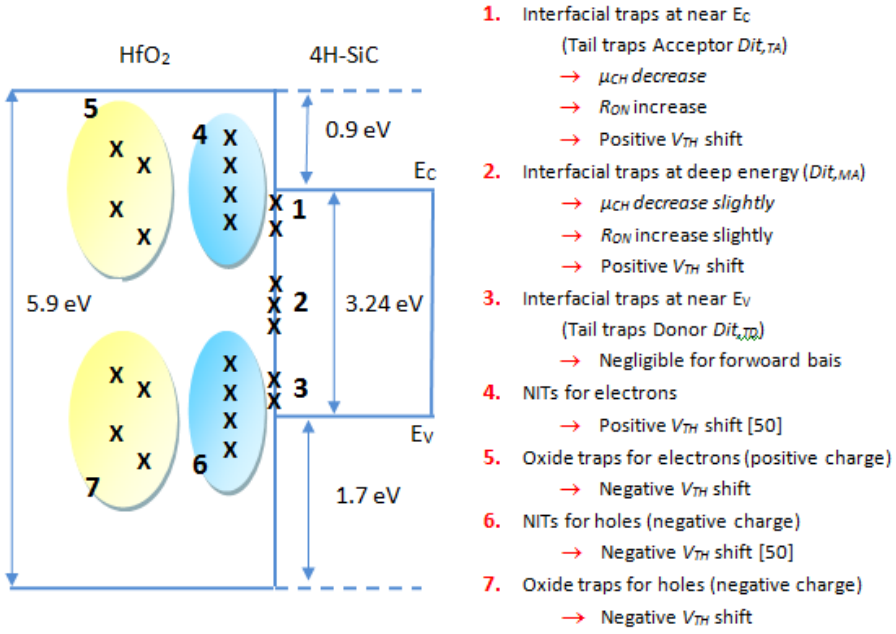

Figure V.20: Trap distribution model at HfO_2/4H-SiC interface for illustration of the relationship between different traps nature and main device electrical characteristics.

V.3.8. Interfacial layer effectiveness

In order to decrease the HfO_2/4H-SiC MOSFET leakage current an interfacial layer between HfO_2 and SiC is used. Large gate currents lead to premature breakdown of the device.

The dielectric stack thickness calculating using the following formula [57]

$$T_{high\text{-}k}=(EOT\text{-}SiO2)*\varepsilon_{high\text{-}k}/\varepsilon_{SiO2} \qquad (2)$$

The gate oxide material HfO_2 is substituted by introducing the interfacial layer as follows I) HfO_2 (18 nm) /Al_2O_3 (2 nm) and I) HfO_2 (18 nm) /SiO_2 (2 nm). The individual thickness values mentioned are fairly approximate values adjusted to *EOT* of 5 nm (SiO_2). Based on our results, we finally come up with the proposed dielectric structure of SiC MOSFET with the sketch of band alignment shown in figure V.21.

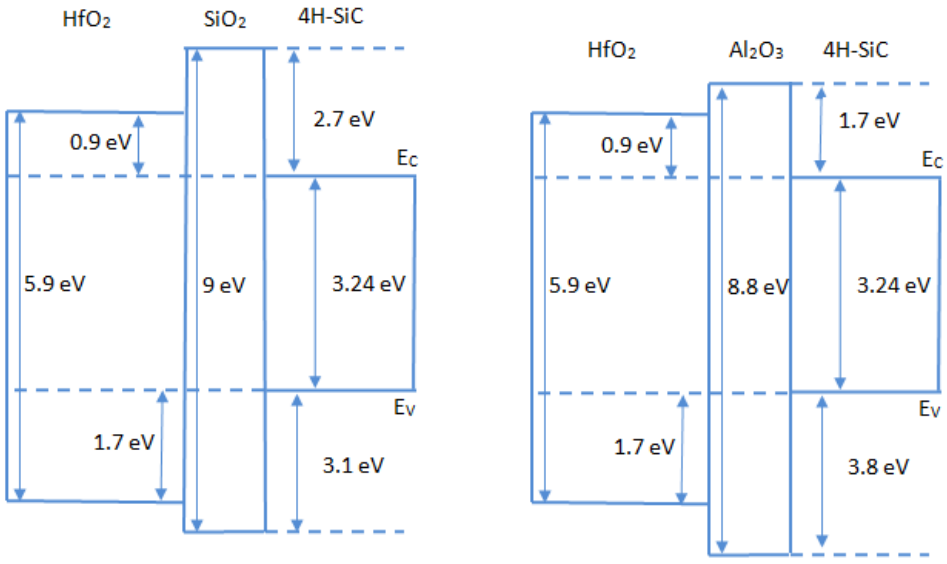

Figure V.21: The schematic band alignments for HfO_2/SiO_2/4H-SiC and HfO_2/Al_2O_3/4H-SiC systems.

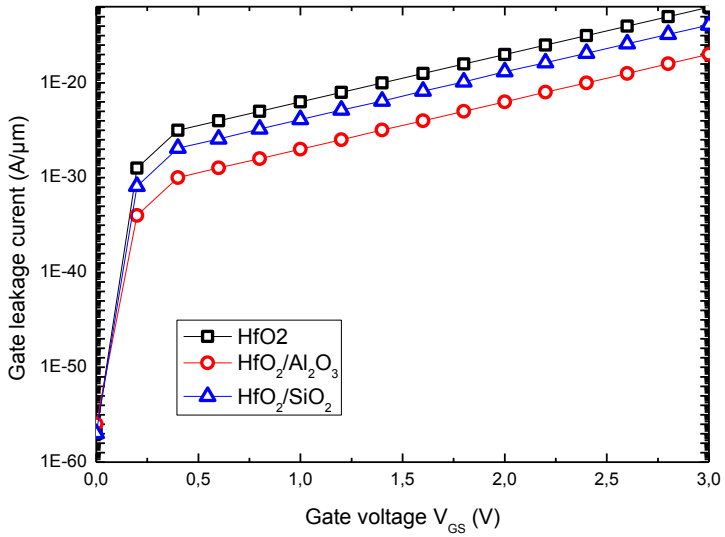

Figure V.22: Gate leakage current comparisons between gate oxide stack.

figure V.22 depicts the off state leakage current as function of V_{GS} for HfO_2/SiO_2 and HfO_2/Al_2O_3 structure. From this figure HfO_2 exhibits the higher leakage current compared to both stack combinations, HfO_2/SiO_2 and HfO_2/Al_2O_3 stack decrease considerably the leakage current by five and three orders of magnitude, respectively. The improvement in HfO_2/SiO_2 and HfO_2-Al_2O_3 stack combinations is due mainly to the lesser amount of conduction band discontinuity variation between the dielectric and 4H-SiC which cause a noticeable difference in the conduction band offset. However Al_2O_3 (k=9.3) as interfacial layer shows a decreased electric field in the oxide compared to SiO_2 and high current capabilities in terms of V_{th}, μ_{ch} and R_{ON} (see table V.3). HfO_2/Al_2O_3 is a better candidate to overcome the tradeoff between leakage current and on state operation mode figure of merits.

Table V.3: Comparison between the proposed 4H- SiC MOSFET, numerical model and commercial devices

Design parameters	**HfO_2**	**HfO_2/SiO_2**	**Proposed HfO_2/Al_2O_3**
Breakdown Voltage *BVL* [V]	150V	150V	150V
Thickness of the oxide t_{ox} [nm]	20	20	20
p-base region doping concentration N_a [cm^{-2}]	10^{17}	10^{17}	10^{17}
Gate voltage V_{GS} [V]	15	15	15
Objective functions			
Vth (V)			
On state resistance R_{on}	9.7 KΩ	10.3KΩ	9.85 KΩ
μ_{ch} cm2 V−1 s−1_	58	54.3	58
g_m (A/μm)	9.5	8.85	9.35
SS (mV dec−1)	380	405	390

V.4. Conclusion

The design of a 4H-SiC MOSFET for low power applications has been considered in terms of a non-uniform p-base doping profile. The impact of the base doping on the device forward current and blocking voltage characteristics has been evaluated. The proposed profile, with an increasing p-base doping concentration in the vertical direction, aids to improve the MOSFET on-state resistance while prevents a premature breakdown under reverse bias conditions. In addition, a lower doping concentration in the region next to the SiO_2/4H-SiC interface (channel region) assures a fast inversion and a decrease of the device threshold voltage. Furthermore, power SiC MOSFET gate dielectrics reliability against temperature and trapping effects has been predicted by means of numerical simulations. A specific carrier-trapping and temperature effects test has been developed to monitor and characterize the electrical parameters of the low breakdown SiC MOSFET with various gate dielectrics (SiO_2, Si_3N_4, AlN, Al_2O_3, Y_2O_3 and HfO_2). Gate oxide dielectric with high relative permittivity improves significantly the device output performance under harsh traps density ($10^{14}cm^{-2}$) condition. HfO_2 show a best immunity against interfacial traps and good threshold voltage stability. Nevertheless, a considerable leakage current is notable. This drawback is surpassed by introducing a thin interfacial Al_2O_3 layer. The HfO_2/Al_2O_3 stack exhibits improved performances in terms of V_{th}, μ_{ch} and R_{ON} and low gate leakage current make conduction band offset beneficial.

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General Conclusion

The research activity reported in this dissertation mainly concerns with the investigation via numerical simulation to assess the reliability and the electrical behavior of 4H-SiC power MOSFET. The basic theory of the physical characteristics of the Silicon Carbide has been introduced by referring to the models developed in the last years for this innovative material.

We have given a description of the main structures of DMOS transistors used in power electronics. We defined the theoretical limits of these components by looking at the interface SiO_2/SiC and the relationship between breakdown voltage and ideal ON resistance. This is how we were able to show that high voltage power MOS transistors are handicapped by the SiO_2/SiC interface quality and the on state resistance. This latter is responsible for the conduction losses of the transistor.

The key physical models are described, taken into account the material bandgap temperature dependence, apparent bandgap narrowing effect, Auger and Shockley–Read–Hall recombination phenomena, incomplete doping activation, impact ionization, and carrier lifetime and carrier mobility expressions depending on temperature and doping concentration. Moreover, Fermi–Dirac statistics and multidimensional dependent anisotropic effects as well as scattering mechanisms that degrade the channel mobility were considered during the simulations.

Proceeding in the way of surmounting the 4H-SiC MOS drawbacks, the electrical characteristics of the device were investigated in terms of the ON-state resistance and breakdown voltage using both analytical and numerical models, revealing good agreement in the considered voltage range. The simulation models were then used as fitness functions for a MOGA-based design with the aim of determining optimal values of the geometrical and physical parameters to minimize the ON-state resistance value for devices with different breakdown voltages in the range from 150 V to 800 V. The analytical and numerical results were also used to evaluate the effectiveness of the

MOGA analysis. With respect to a low-voltage DMOSFET dimensioned for B_{VDS} = 150 V, the optimized device achieved an R_{ON} value decreased by a factor of 20% with respect to that reported in previous work. Moreover, the carrier-trapping effects on the electrical characteristics of a 4H-SiC MOSFET have been predicted.

In order to investigate the device ruggedness, a combined model of both defect energy levels inside the 4H-SiC bandgap (tail and deep level traps) and oxide-fixed traps has been considered. The trap density reference values have been assumed referring to literature data. Starting from a fresh structure (defect-free) we have calculated an on-state resistance close to 140 kΩ×μm^2(V_{GS} = 10 V, V_{DS} = 1 V, and T = 300 K), which increases up to 200 kΩ×μm^2 for a defected device resulting comparable to that of a commercial Si-based MOSFET rated for the same voltage range. The device threshold voltage and carrier mobility in the channel region decrease as a function of both the temperature and trap density. In particular, the oxide-fixed traps have a severe impact on the V_{th} value.

The impact of the base doping on the device forward current and blocking voltage characteristics has been evaluated. The proposed profile, with an increasing p-base doping concentration in the vertical direction, aids to improve the MOSFET on-state resistance while prevents a premature breakdown under reverse bias conditions. In addition, a lower doping concentration in the region next to the SiO_2/4H-SiC interface (channel region) assures a fast inversion and a decrease of the device threshold voltage. Besides, a specific carrier-trapping and temperature effects test has been developed to monitor and characterize the electrical parameters of the low breakdown SiC MOSFET with various gate dielectrics (SiO_2, Si_3N_4, AlN, Al_2O_3, Y_2O_3 and HfO_2). Gate oxide dielectric with high relative permittivity improves significantly the device output performance under harsh traps density (10^{14}cm^{-2}) condition. HfO_2 show a best immunity against interfacial traps and good threshold voltage stability.

The results obtained through this dissertation also encourage us to carry out additional reflections in this field. For example, by investigate other phenomena that affect this device, where other models and approaches need to be developed.

Appendix A

Metaheuristic methods

A.1. Introduction

As modern computational and modeling technologies develop, technical design relies heavily on computer modeling and simulation to accelerate design cycles and reduce costs. A complex design problem will involve many parameters; and the search for optimal solutions remains a major challenge for these systems.

Optimization is a branch of mathematics that studies methods and techniques specifically designed to find the "best" solution to a given "optimization" problem. It aims to minimize or maximize one or more objective functions based on one or more dependent variables that may take whole or real values. Optimization is widely applied in areas such as engineering, commerce, transportation, finance, medicine, and all Many traditional optimization techniques have been designed to solve a wide range of problem optimization, such as linear programming, nonlinear programming, dynamic or combinatorial optimization programming [1]. However, many of the applied classical optimization techniques suffer from a sensitivity marked by problems such as: difficulties in overcoming local optimal solutions, risk of divergence, difficulties in constraints or others [1]. To overcome these problems, heuristics and metaheuristic techniques were proposed in the early 1970s [2]. Unlike classical methods, (Meta) heuristic methods have a simple and compact theoretical support and are often based on empirical criteria. Due to the great diversity and complexity of the problems encountered by microelectronic device engineers, researchers in this field were pioneers in using heuristics and metaheuristic techniques to solve optimization problems [3]. This chapter presents an overview of metaheuristic techniques used to solve optimization problems. In this thesis, we propose to use genetic algorithms to optimize GAAJ MOSFET performance.

A.2 Heuristic methods

Exact classical optimization methods often end up not determining a solution in a reasonable time. To avoid such cases, alternative methods have been proposed to determine good approximations to exact solutions. In particular, heuristic methods attempt through the knowledge and experience of experts to explore the space of research in a particularly practical way. The heuristic methods were introduced by G. Polya in 1945 [2] and developed later in the 1970s, where they were used for specific problems in different fields of science and technology [3]. Basically, a heuristic is designed to provide better computational performance over conventional optimization techniques to the detriment of lower accuracy. However, the "rules of thumb" underlying a heuristic are often very specific to the problem under consideration. Moreover, since heuristics are problem solving techniques based on the expertise of solvers, they use domain-specific representations [4]. A wide range of heuristic search strategies is mentioned in the literature. Examples include the best first search (BeFS), beam search (BeS) or search A * (A * S) [5-8].

Unsophisticated or blind search strategies are applied without any information about the search space, apart from the possibility of distinguishing between an intermediate state and a target state. Informed research strategies use problem-specific knowledge. Usually, this knowledge is represented using an evaluation function that evaluates either the quality of each state in the search space, or the cost of moving from the current state to an objective state using various paths. In the case of BeFS, among all possible states at one level, the algorithm chooses to extend the most "promising" in terms of a specified rule [9]. BeS is an improved version of the BeFS algorithm. The improvements consist in reducing memory requirements [66]. For this purpose, BeS is defined according to BrFS which is used to build the search tree. At each level, all new states are generated and the heuristic function is calculated for each state inserted in a list ordered by heuristic function values. The list, of limited length, is equal to the "beam width". This limits the memory requirements, but the compromise is likely to prune the path to the goal state.

The search algorithms *A** use a BeFS strategy and a heuristic function that combines two metrics: the cost of the origin at the current state and a cost-to-purpose estimate. The algorithm *A** is considered very efficient [6]. One of the drawbacks of the research

strategies presented above is the numerical inefficiency of the research process, especially for large-scale problems. Thus, significant efforts have been made to identify new heuristics that can cope with these problems.

A.3 Metaheuristic methods

The new paradigms were called metaheuristic and were first introduced in the mid-1980s as a family of algorithms that can approach and solve complex optimization problems using a set of multiple heuristics. The term metaheuristic has been proposed in [11] to define a high-level heuristic used to guide other heuristics for a better evolution in the research space. Although traditional stochastic research methods are mainly based on chance (solutions change randomly from one step to another), they can be used in combination with metaheuristic algorithms to guide the research process and accelerate convergence. Metaheuristic algorithms are only approximation algorithms because they can not always find the optimal overall solution. However, the most attractive feature of a metaheuristic is that its application does not require any particular knowledge of the optimization problem to be solved. This state makes metaheuristics a general tool for solving optimization problems [12, 13].

Since their introduction in the mid-1980s until now, metaheuristic methods to solve optimization problems have been continuously developed. They make it possible to address and solve a growing number of problems that were previously considered difficult or even impossible to solve. These methods include genetic algorithms, particle swarm optimization, and ant colony algorithm.

A.4 Genetic algorithms

Genetic algorithms are one of the most used optimization methods. They represent a branch of the field of research called evolutionary computation [14]. They make it possible to determine the maximum or minimum values of a given function. They mimic the biological processes of reproduction and natural selection to find solutions to a given problem [14]. Many processes of a genetic algorithm are random. However, this optimization technique makes it possible to set the level of probability and the level of control [14]. These algorithms are much more powerful and efficient than random search and exhaustive search algorithms [14], but do not require additional information about the given problem. This feature allows them to find solutions to problems that other optimization methods cannot handle due to lack of continuity, derivatives, linearity, or other features.

In what follows, we will give the basic elements of a genetic algorithm. The specific parts of the genetic algorithm that have a particular function are called operators. In its simplest form, a genetic algorithm is composed of three basic operators:

- Selection
- Crossover
- Mutation

In addition to these basic operators, the generation operator creates the chromosome population. In addition, the elitism operator is used to prevent the loss of successful individual chromosomes. These operators are applied to the current generation to form the next generation. The genetic algorithm continues to evolve until the design criteria are met. These criteria are defined by the user at the very beginning of the optimization.

Figure 1 presents the basic fundamentals of the genetic algorithm. In the beginning, the population is evaluated and their physical condition is determined. Then successful individuals are selected and they replace those who fail. The next step is to train the next population using elitism, crossover and mutation. These processes continue until the predefined population number is reached [14].

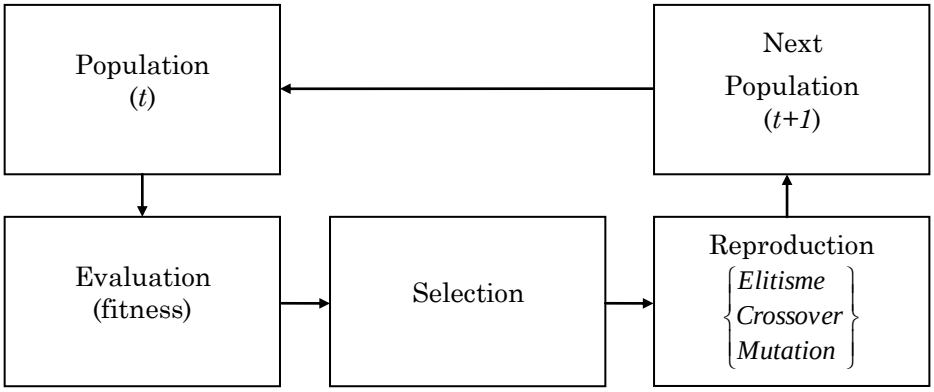

Figure 1. *Simple flow chart of the genetic algorithm*

A.4.1. Chromosome concept

The genetic algorithm uses the concept of chromosome to define the variables. Each decision variable is defined in genes to form chromosomes. The common means of coding is a binary string..

A.4.2. Generation

Based on the data we have, the genetic algorithm will generate an initial population. Each population is composed of chromosomes. Each solution (chromosome) will contain decision variables generated randomly. The random number generator assigns a 1 or a 0 to each bit position in the chromosome where the defined number of bits represents specific decision variables. This operator is called the "Generation" operator.

Once the initial population is generated, the genetic algorithm will translate each gene into the corresponding variable and calculate the objective function. Once the objective function is reached, an analysis must be carried out for each chromosome of the population [15].

A.4.3. Selection

This operator is used to eliminate the worst chromosomes because of their low fitness. Once their objective functions are determined at an earlier stage, a number of chromosomes with the worst fitness are replaced by the same number of better chromosomes [15].

A.4.4. Elitism

Elitism is used to protect the most suitable chromosomes of crossbreeding and mutation. The goal is to have some of the best chromosomes best suited in the next generation and not lose them. Elitism can quickly increase the performance of the genetic algorithm [15].

A.4.5. Crossover

The crossing operator is applied to initiate a partial exchange of bits (information) between the parent strings to form two descendants. The genetic algorithm will randomly choose two solutions for crossing.

The crossover rate is defined by the user at the beginning of the study. The most popular crossover types are single-point, two-point and multi-point crossings as shown in Figure 2. Note that all crosspoints are randomly selected [15].

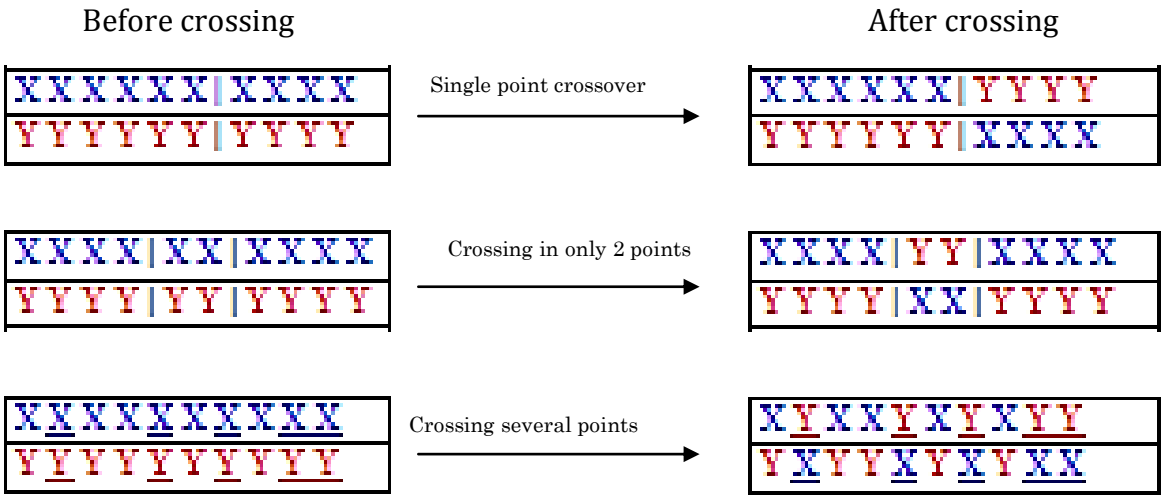

Figure.2. *Crossover Operator*

A.4.6. Mutation

Once the moment of application of the mutation is known, the mutation operator simply randomly changes the value of a gene. For real genes, this change could be done by selecting a number evenly across the range of possible values. Another possibility is to use a zero mean Gaussian distribution with a given variance where the number generated by this distribution is added to the value of the gene. This could be adjusted so that the variance decreases as the algorithm iterates [15].

A.5. Implementation of a genetic algorithm

Genetic algorithm follows the following steps [15]:

Step 1 : Define the number of chromosomes, generation, mutation and crossover rates.

Step 2 : Generate a number of population and initialize the value of the genes with a random number.

Step 3 : Done steps 4 to 7 until the generation number is reached.

Step 4 : Evaluation of the fitness value of chromosomes by calculating the objective function.

Step 5 : Evaluation of the fitness value of chromosomes by calculating the objective function.

Step 6 : Crossover

Step 7 : Mutation

Step 8 : Solution (best chromosome)

The flowchart of a genetic algorithm is shown below.

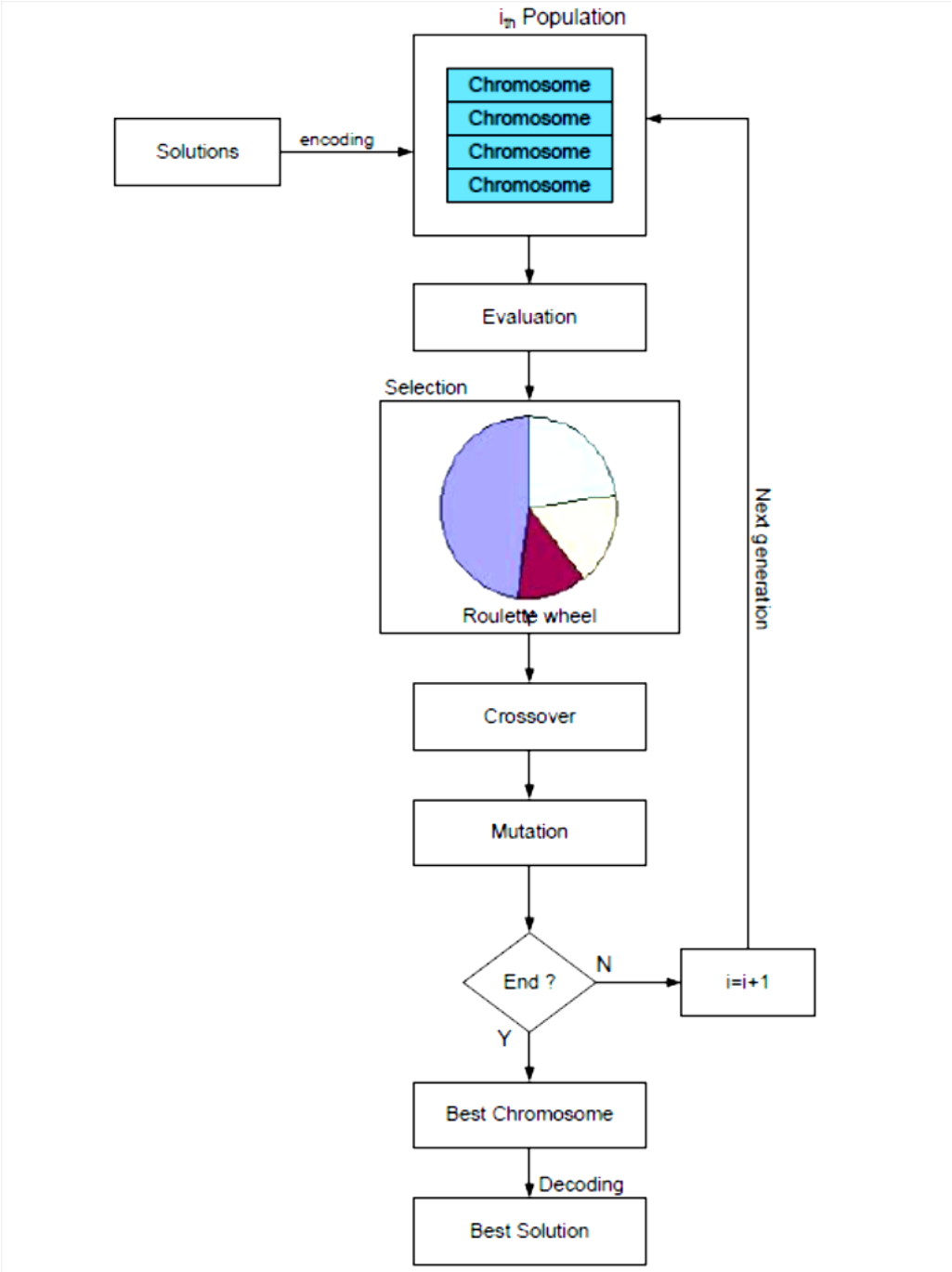

Figure.3. *Flowchart of a genetic algorithm*

A.6. Conclusion

Genetic algorithms provide solutions close to the optimal solution using selection, hybridization and mutation mechanisms. A genetic algorithm gives us great freedom in the setting and implementation of different treatments. We are then free to modify a particular parameter if the solutions obtained do not suit us.

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