République Algérienne Démocratique et Populaire
Ministère de l'Enseignement Supérieur et de la Recherche Scientifique

Université de Batna 2 – Mostefa Ben Boulaïd
Faculté de Technologie
Département d'Electronique

Thèse

Préparée au sein du Laboratoire d'Électronique Avancée (LEA)

Présentée pour l'obtention du titre de :

Docteur en Sciences en Électronique
Option : Composants

Sous le Thème :

Contribution to the study and the design of inverters control

« Contribution à l'étude et à la conception des commandes des onduleurs »

Présentée par :

BELKACEM Riadh EL Mehdi
Ingénieur d'état en Electronique, Magister en Electronique

Devant le jury composé de :

SAIDI Lamir	Prof.	Université de Batna 2	Président
BOUGUECHAL Nour-Eddine	Prof.	Université de Batna 2	Rapporteur
SRAIRI Kamel	Prof.	Université de Biskra	Examinateur
BENAKCHA Abdelhamid	Prof.	Université de Biskra	Examinateur
BARA Kamel	Prof.	Université d'Oum El-Bouaghi	Examinateur
ARAR Djemai	Prof.	Université de Batna 2	Examinateur

Juillet 2018

To my dear parents

To my dear wife

To my dear kids

To my sisters and brothers

Acknowledgments

First of all, I would like to express my appreciation and thank my advisor, Professor BOUGUECHAL Nour-Eddine, Prof at the university of Batna2, for his commitment, availability and patience during all the past years, without his valuable directions we would not be able to achieve this modest work that we are presenting through this dissertation.

Secondly, I would like to sincerely thank Professor SAIDI Lamir, from University of Batna2, for accepting to preside the committee of defence of my dissertation.

I also want to thank all the examination committee members, prof BENAKCHA Abdelhamid, from University of Biskra, Prof. SRAIRI Kamel, from University of Biskra, Prof. BARA Kamel from the university of Oum El-Bouaghi, and Prof. ARAR El Djemai from the university of Batna2, who accepted and agreed to be members of the examination board, and also for dedicating the time and the effort to review this modest work.

A very special gratitude to my friend Prof. Redha Benzid, at university of Batna2, who has been supportive during the entire journey, and very generous on ideas and time, from the start to the end.

Last and not least, I thank my friend and brother in low Karim Brioua from University of Batna2 for his stand and support which has given me the energy to continue all the way.

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List of Acronyms

AC	Alternating current
ANN	Artificial Neural Network
BA	Bee Algorithm
BBO	Biogeography Based Optimisation
BJT	Bipolar Junction Transistor
BOA	Bat Optimization Algorithm
CHB	cascaded H bridge
CM	common mode
CS	Cuckoo Search
DC	Direct current
DE	Differential Evolution
FF	Firefly
FFA	Firefly Algorithm
GA	Genetic Algorithm
GE	General Electric
GTO	gate turn-off thyristor
ICA	Imperial Competitive Algorithm
IGBT	Insulated Gate Bipolar Transistor
MLI	Multi level Inverter
MOSFET	metal–oxide–semiconductor field-effect transistor
NPC	neutral-point clamped
PA	photosynthetic algorithm
PSO	Practical Swarm Optimization
PWM	pulse width Modulation
SCR	silicon controlled rectifier

SHE	Selective Harmonic Elimination
SHEPWM	Selective Harmonic Elimination PWM
SPWM	Single-Triangle PWM
SVC	Space Vector Control
SVPWM	Space Vector PWM
THD	Total Harmonic Distortion
UPS	Uninterruptable Power Supply

Abstract

Inverters are DC-AC converters that are increasingly used in energy systems especially in renewable energies. For this, the inverters must use the available energy efficiently. They must therefore have a high efficiency and reliability.

Moreover, the performances of these systems are measured by their efficiency, waveform and harmonic distortion of the output, and finally their cost, which depend on the optimal choice of the components and the control strategy.

In this thesis, we will study some structures and control strategies, concentrate more on the Total Harmonic Distortion (THD) reduction.

Reduction of the THD in multilevel inverters requires resolution of complex nonlinear transcendental equations, without having to resolve these equations; we have proposed to use the recent firefly algorithm (FFA) to optimize the THD, through finding the best switching angles and guaranteeing the minimization of harmonics within a user-defined bandwidth. The FFA has been compared to some existing widely used algorithms such as genetic algorithm (GA), and has shown a faster convergence.

We have also chosen to use one of the best existing optimized hardware structures, where we have validated the simulation results through practical tests.

We stress on the fact that the best design alone or the best control strategy alone cannot solve the THD problem at a reasonable cost, it is imperative to address both subjetcs at the same time.

The obtained THD through the simulation of the thirteen-level symmetric inverter has been reduced down to 5% (FFT of 60 harmonics). In order to validate the simulation results, a thirteen-level symmetric inverter prototype has been made, and practically experimented and tested with different loads. Consequently, the measured THD with resistive load was 4.7% on a bandwidth of 3 kHz.

Key words: firefly algorithm (FFA), genetic algorithm (GA), inverter, multilevel, optimized THD

Résumé

Les onduleurs sont des convertisseurs DC-AC de plus en plus utilisés dans les systèmes énergétiques, en particulier dans les énergies renouvelables. Pour cela, les onduleurs doivent utiliser l'énergie disponible de manière efficace. Ils doivent donc avoir une efficacité et une fiabilité élevées.

De plus, les performances de ces systèmes sont mesurées par leur efficacité, forme d'onde et distorsion harmonique de la sortie, et enfin leur coût, qui dépendent du choix optimal des composants et de la stratégie de contrôle.

Dans cette thèse, nous étudierons certaines structures et stratégies de contrôle, en nous concentrant davantage sur la réduction de la distorsion harmonique totale (THD).

La réduction du THD dans les inverseurs multiniveaux nécessite la résolution d'équations transcendantales non linéaires complexes. Sans avoir à résoudre ces équations, nous avons proposé d'utiliser le récent algorithme firefly (FFA) pour optimiser le THD, en trouvant les meilleurs angles de commutation et en garantissant la minimisation des harmoniques dans une bande passante prédéfinie par l'utilisateur. Le FFA a été comparé à certains algorithmes largement utilisés existants tels que l'algorithme génétique (GA), et a montré une convergence plus rapide.

Nous avons également choisi d'utiliser l'une des meilleures structures matérielles optimisées existantes, où nous avons validé les résultats de la simulation par des tests pratiques.

Nous insistons sur le fait que la meilleure conception seule ou la meilleure stratégie de contrôle seule ne peut pas résoudre le problème THD à un coût raisonnable. Il est impératif d'aborder les deux sujets en même temps.

La THD obtenu grâce à la simulation de l'onduleur symétrique de treize niveaux a été réduite à 5% (FFT de 60 harmoniques). Afin de valider les résultats de la simulation, un prototype d'onduleur symétrique de treize niveaux a été réalisé et pratiquement expérimenté et testé avec différentes charges. Par conséquent, la THD mesurée avec une charge résistive était de 4,7% sur une bande passante de 3 kHz.

Mots clés: algorithme firefly (FFA), algorithme génétique (GA), inverseur, multiniveau, THD optimisé.

ملخص

تلقى المحولات الكهربائية رواجا كبيرا و خصوصا في مجال استغلال الطاقات المتجددة.

إحدى الميزات المهمة والمحددة لنوعية هذه المحولات هي القدرة على الاستعمال المثالي لطاقة المتوفرة لأجل الحصـــول على دقة و فعالية عالية.

أداء هذه المحولات يقاس بقياس نسبة الفعالية , شكل الموجة, التشوه التوافقي الناتج و التكلفة المحددة للاختيار الأمثل للعناصر المكونة للجهاز و الإستراتجية المنتهجة في التحكم في نظام الجهــاز.

في هذه الأطروحة تم دراسة بعض الأمثلة و الاستراتجيات المنتهجة في التحكم في أنظمه المحولات و ذلك بالتركيز على معالجة التشوه التوافقي الكلي THD من أجل تقليصه والحد منه . في مثل هذه المحولات ذات المستويات المتعددة يتطلب ذلك حل معادلات غير خطية و معقدة.

لتفادي حل هذه المعادلات تم اللجوء للاستعمال خوارزمية (Firefly algorithm).

وذلك لتحسين THD باختيار أفضل قيم الزوايا التي تمكننا من تقليص التشوه التوافقي في حدود عرض النطاق الترددي المعطى من قبل المستخدم.

هذه الطريقة FFA تم مقارنتها ببعض الخوارزميات ذات الاستعمــال الموسع على سبيل المثال (GA) وأظهرت تقارب أسرع من هذه الأخيرة.

في عملنا هذا تم اختيار أحسن الهياكل المتوفرة وتم التحقق من النتائج النظرية باختبارات عملية.

بعدها تأكدنا أن لا الاختيار الأمثل للهيكل لوحده ولا الاختيار الأفضل لإستراتجية التحكم في النظام لوحدها كافية لمعالجة مشكل (THD) بتكلفة معقولة. الحل هو تناول الموضوعين في آن واحد.

حسب الدراسة المحققة بمحاكاة محول متكون من ثلاثة عشرة مستوى تم تقليص (THD) بنسبة 5%.

من أجل التحقق من صحة النتائج المتحصل عليها تم استعمال نموذج متكون من ثلاثة عشرة مستوى وتم الاختبار بتطبيق حمولات مختلفة وأبانت التجربة أنه من أجل حمولة مقاوميه (charge resistive) قيمة (THD) كانت 4.7% من أجل عرض نطاق ترددي قيمته 3 kHz.

كلمات مفتاحية:

خوارزمية Firefly,خوارزمية GA, المحولات الكهربائية ,أحسن THD

Chapter 1

Introduction

1. 1 Introduction

Through the last few years, there have been extensive researches about substitutes of conventional energies through renewable energies. This new type of energy can be produced by wind turbines and Solar Photovoltaic Energy. Such a solution needs systems to stock and convert the energy. Considered as one of the crucial parts that allow delivering clean Alternating Current (AC), inverters have been one of the important research axes, the main ambition was to increase the quality of the output waveform, in addition to promote and improve friendly environment systems. [1, 2].

In general, the Electronic power converter technology has gradually become an important element in energy generation, transportation, storage and distribution. This discipline is now the heart of the industry and many domestic applications, and therefore the sector of power conversion is one of the fastest growing markets in the last 40 years [3]. In fact, electricity and electricity conversion are now a key part of our lives, and no one can imagine a world without Electricity. An essential part of the power electricity conversion is the power electronics, used in most of the appliances at home and in the industry. The evolution of the power semiconductor devices and technology devices has widely open the doors to the switching converters, as these last ones compose the heart of the modern power electronic equipment. The modern solid-state power electronics era started in 1957 by General Electric through the introduction of the silicon controlled rectifier, also known as thyristor ,which is still being used till today, the disadvantage of the SCR is its turn-off status not easily controlled , therefore other devices were invented. The GTO, gate turn-off thyristor was invented at GE in 1958, Power GTOs were introduced to the market in 1980s. [4]

While the Bipolar Junction Transistor (BJT) was invented in 1947, the power BJT was only introduced in 1970s, and considered now as obsolete in the area of power electronics. While the MOSFET transistor was known before the invention of the SCR and the bipolar transistor, the power MOSFET was introduced only in 1978 . 1980 is the beginning of the Insulated Gate Bipolar Transistor, The IGBT concept was made the first time by B. Jayant Baliga at GE. That was in response to answer a challenge of GE Vice President Tom Brock, who expressed a need of a new device to replace the Darlington bipolar transistors used in Air conditioners. [7].

The first IGBT wafers from the Intersil production line became available in August 1981. In 1983, the GE Semiconductor Products Department released the first IGBT product: a power-MOS IGT D94FQ4, R4 with ratings of 400, 500 V, and 18 A based on B. Jayant Baliga chip design and manufacturing process previously experimented at Intersil.

That was the beginning of a new era of power devices, since than the IGBT is still in use, and is the most important device for medium-to-high power applications, that was led by GE, who has its roots deep in technology from Thomas Eddisson to B Jayant Baliga. [5,6].

Power conversion is done from ac to dc in all possible combinations, ac-dc, dc-dc, dc-ac, and ac-ac. In our case, we will concentrate on the dc-ac conversion, or the inverters.

The performance of the inverter is generally related to the Total Harmonic Distortion at the output, while there are other characteristics to monitor as well, such as efficiency, power losses and reliability, optimal energy transfer, fault tolerance and cost.

It is well established that multilevel inverter (MLI) can produce a high quality signal and low Total Harmonics Distortion (THD). In fact, during these many years, several applications using multilevel inverters have been proposed and realized. The Aim of this thesis is a contribution of study of the inverters control. Reducing the THD will depend on the design and the adopted control strategy.

Without increasing the cost of the final product.

The cost of the inverter will depend on its power range, type, number and power range of the semiconductors, and the design of the inverter.

It is obvious that a system composed from less components is less susceptible to fail, and has a lower probability of faults.

The design of the inverter does not only depend on the topology of the hardware and the type of semiconductor devices but also the way of controlling them, how the PWM will be generated in order to allow a smooth transfer of energy. This is where the optimization is required. Choosing the right optimization method is also challenging. In our case, this was developed by introducing the most recent firefly algorithm, which had been used to contribute in THD improvement.

1.2. Motivation and objectives

We have analyzed the waveform on the output of many UPSs available in the Algerian market. The UPSs were used to feed mainly computers, and Voltage would be rectified. The signal was far from being a sin wave, with High THD not within the international standards, IEEE 519-1992.

The same UPSs would not be able to feed any AC Motors, because of the low quality of the signal. This is why we thought of designing our own inverter , with a THD within the international standard, where the THD is less than 5%, and provide a cost effective product and made it accessible to the wide Algerian Market, and consequently have a socioeconomic impact through this work.

We also want to make it a reference for an initiation of inverter controls, that can be used as a support guide for students.

Following our modest knowledge at the beginning of the project, we have asked many questions in different corners, and was imperative to direct them into the same way in order to achieve a pre-established goal, a better Inverter with less cost. This constraint has definitely introduced the optimization concept into the process.

1.3 Questions we have asked

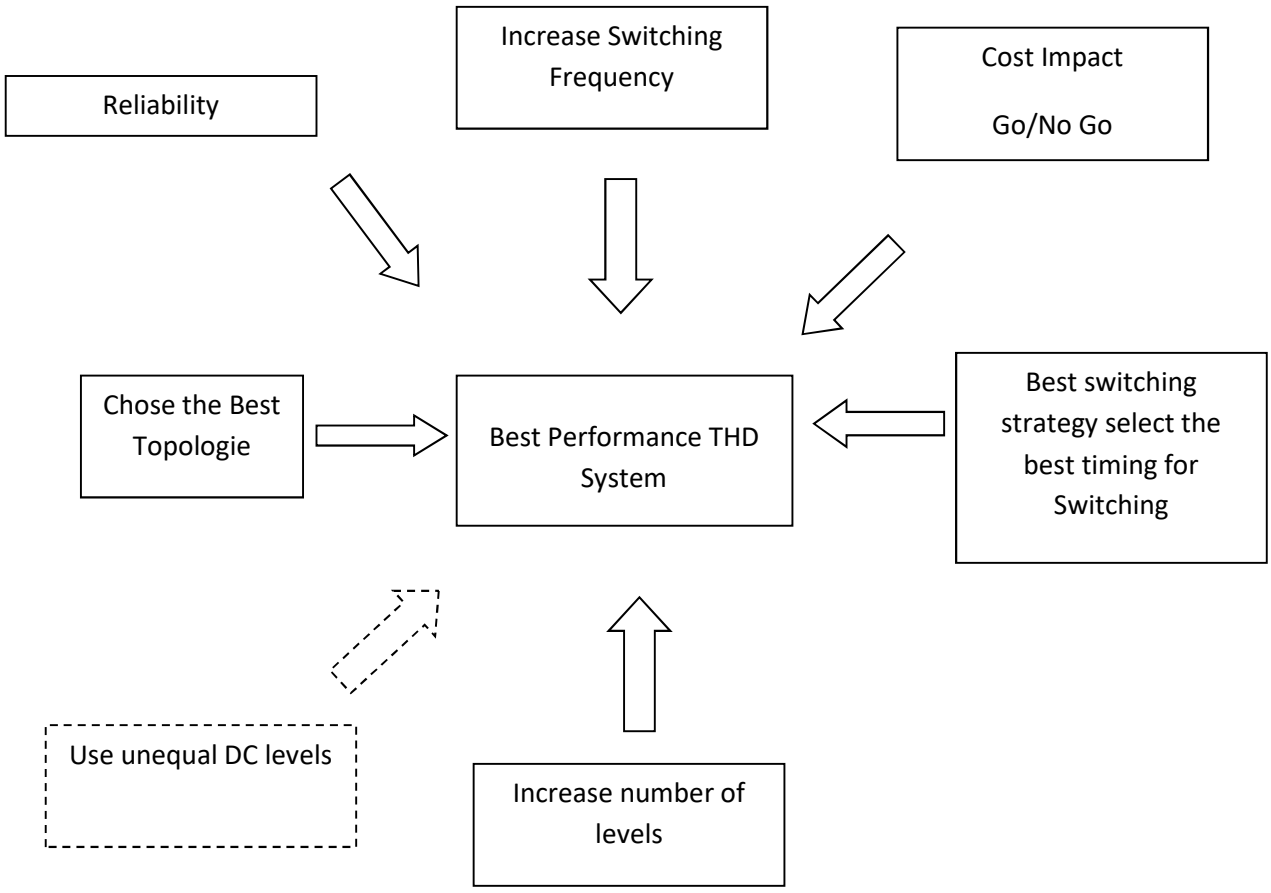


Figure 1.1: Problem statement illustration

- Increasing the number of levels can improve the THD, generating a staircase, will be closer to the pure sine wave as we increase the number of stair steps. What would be the acceptable level?
- Another important parameter comes into the equations, and that is the selection of switching angles, the switching angles can improve or degrade the THD. How to choose the angles?
- A good performing system would not rely only on an optimized structure, but requires also a strong control strategy in order to perform. What strategy we will use?

- The 3 levels inverter can produce an acceptable THD if the switching frequency is increased, and if the switching angles are the best switching angles. What would be the min frequency to get us to the 5% THD? is that achievable? What is the impact on the cost?
- That is where new parameters show up, the cost and the reliability of the final product. How far we want to increase and complicate the structure?

Figure1.1 illustrates the initial brainstorming around the multiple ideas.

First, we have assessed many structures and made various simulation programs through Matlab. Program was flexible to ensure we can choose the number of levels and the switching angles, a series of tests have been performed to ensure that theory is close enough to the real world. While we did not include a comprehensive study of semiconductor devices, electronic schematics, prototype boards and further hardware details in the thesis since this was not within our objective. It is important to mention that a thorough knowledge and understanding of these disciplines is required to perform the practical tests and develop the hardware. We are open to provide any details if requested. The hardware and all the programs are part of the intellectual property of university of Batna, were the work has been performed.

1.4 Organization of the thesis

This thesis is organized in 5 chapters and a conclusion.

Chapter 1

Introduction, energy growth and electrical energy is an essential part of our actual world, and explained the main problematic of the inverters and the goal of the project, reaching a THD at 5%, through the multilevel inverter, with the minimum cost.

Highlighted the fact that the best design alone or the best control strategy alone cannot solve the THD problem at a reasonable cost. It is imperative to address both at the same time, and introduce our proposed strategy of optimization to find the best switching angles in order to have the lowest THD. We have also stated what has motivated us to take this project and the different questions at early stage.

Chapter 2

state of the art1, Inverters topologies: where we have presented the three main topologies diode clamped, flying capacitor and cascaded H bridge, indicated the advantages and disadvantages of each one , some emerging multilevel inverter have been also presented.

Chapter 3

State of the art2, PWM Control methods:

In this chapter, we will present the most relevant control and modulation methods developed for the multilevel inverters, multilevel sinusoidal pulse width modulation, multilevel selective harmonic

elimination, space-vector modulation, space vector control, One-Dimensional Modulation and our proposed method Minimum THD PWM.

Chapter 4

Optimization algorithms, where a survey of the optimization algorithms has been presented, most of the algorithms that have been used to resolve reduce the THD. One scientific article published, we have used the recent firefly algorithm to find the best switching angles, up to 60 harmonics were analyzed, equivalent of 3 Khz bandwidth. Found the best Angles through the firefly algorithm who has show a faster convergence.

Chapter 5

Practical implementation, experimental tests & Results.

A survey of many proposed structures has been done, and we have selected the best one available in terms of reduction of power switches, less semiconductor devices, consequently using a simple control strategy. The optimized angles found in chapter 4 were used, in order to reduce the THD on all the spectrum of 60 harmonics.

The used structure, has been designed to be extensible in terms of number of levels , as it is modular, and also in terms of power, we can easily replace the existing MOSFET switches by IGBT switches, in few words the proposed inverter has several advantages such as: reduced number of switches, simple circuit design, simple control strategy and, finally, the inverter has only two isolated ground Gate driver power supplies and it can be extended to a higher number of levels by stacking more basic cells.

The prototype is built around a PIC16F628A has been produced and tested successfully. The inverter has been practically experimented to validate the simulations results. Consequently, the measured THD with resistive load was 4.7% on a bandwidth of 3 kHz.

Conclusion- Summary and future work

Contains a summary of the overall work performed, results and further work and developments that can be done in the future.

Chapter 2

State of the art 1- Multilevel inverts topologies

2.1. Introduction

In this chapter we will go through the 3 main topologies of MLIs, chronological evolution, advantages and weaknesses of each type, a flavor of the emerging hybrid topologies is also presented.

Multilevel inverters have been recently the subject of interest of many publications and appeared to be an excellent alternative in the class of high-power medium-voltage energy control [8-9].

Through the MLI inverter, the generated waveform has to be as close as possible to a pure sin wave, and known for the ability to decrease the THD better than the two levels inverters [8,9].

The type of the multilevel inverter can be defined by the way of connecting the DC sources, either separated DC sources or common DC sources [28].

Figure 2.1 summarizes the types of the MLIs.

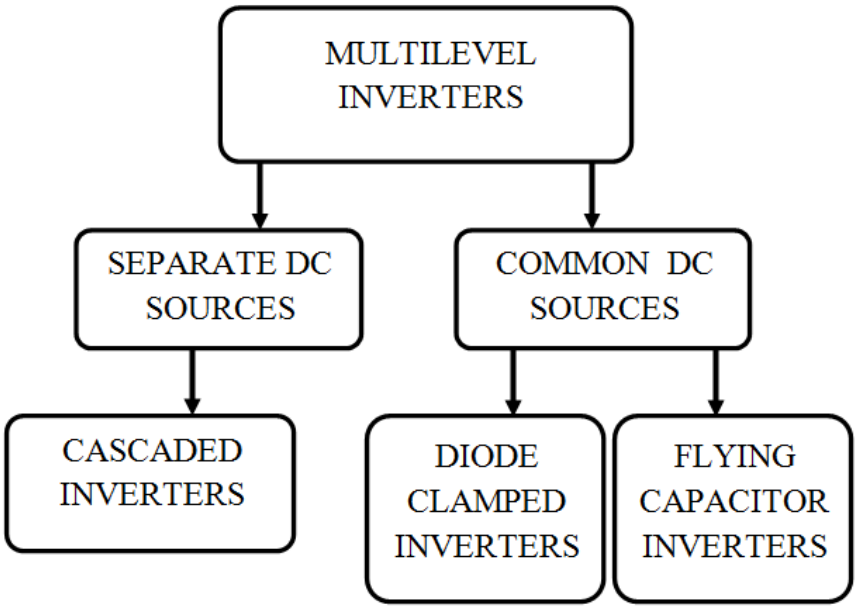


Figure 2.1: Types of multilevel inverters [28].

In This chapter, we will present the most important topologies of multilevel inverters:

- Diode-clamped inverter (neutral-point clamped).
- Flying capacitor (capacitor-clamped).
- Cascaded multilevel inverters with separated dc sources.

Emerging variants of these topologies like asymmetric hybrid MLI are also discussed.

Some applications in today's industry, as Controlled ac drives with high power demand, in the megawatt range are usually connected to the medium-voltage network.

Connecting one switch directly to the medium voltage grid is very challenging, a new generation of inverters has appeared to interface with the medium and High voltage grids, by using multiple switches instead of one, the multilevel inverters consists of array of power semiconductor switches and capacitors or dc sources.

The control of the different switches will allow generating the desired voltage by adding a combination of voltages across the capacitors or the dc sources, the output voltage will look like a staircase waveform. In this case, the switch will only hold a fraction of the high voltage.

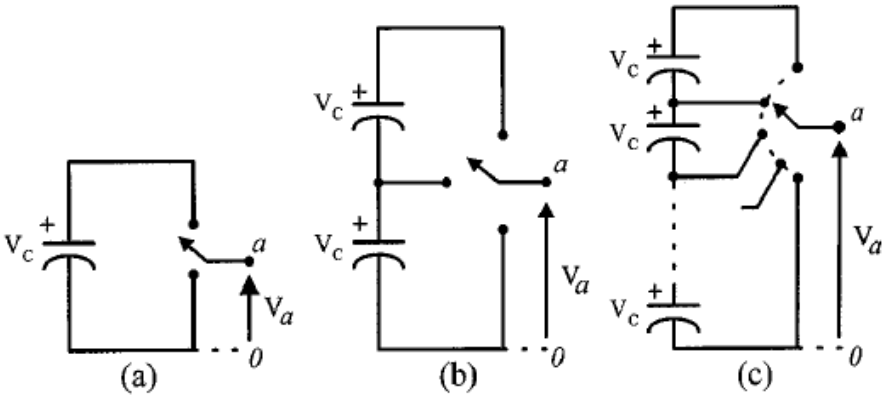


Figure 2.2: One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels [8].

Figure 2.2 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor (see figure 2.2(a)) [8], while the three-level inverter generates three voltages, and so on.

The word multilevel starts with the three-level inverter introduced by Nabae et al. [10]. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems. Three different topologies have been proposed for multilevel inverters: diode-

clamped (neutral-clamped) [10]; capacitor-clamped (flying capacitors) [11], [12] and [13]; and cascaded H bridges with separate dc sources [11], [14] and [15].

The most attractive features of multilevel inverters are:

1) They can generate output voltages with extremely low distortion and lower dv/dt.

2) They draw input current with very low distortion.

3) They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated [16].

4) They can operate with a lower switching frequency.

The term multilevel starts with the three-level inverter introduced by Nabae et al. [10].

One of the earliest papers regarding the MLI was published by JR Baker et al more than 45 years ago, through US patent in 1975. The earliest MLI was described as a programmed switching system, that can provide a stair case signal, and used to convert direct current into alternating current , and produce a quasi-sinusoidal output, with the ability of controlling the harmonic content. A further object was to provide a converter where alternating current of one frequency is converted to alternating current of another frequency. [15]

In 1980 the diode-clamped multilevel inverter has been presented in [17]. The diode-clamped inverter was also known as the neutral-point clamped (NPC), because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching, the circuit topology succeeded in the 1980s. The application of the NPC inverter and its extension to multilevel converter was found in [18].

Even though the cascade inverters were invented earlier, their applications did not succeed until the mid of the 1990s. Two important patents [19], [20] were filed in 1997 to indicate the superiority of cascade inverters for motor drive , static VAR compensators, and photovoltaic utility interface systems.

Due to the great demand of medium-voltage high-power inverters, the cascade inverter has drawn remarkable interest ever since, in the early 2000. More inventions were registered in US patent including the cascade inverters in regenerative-type motor drive applications [21],[22].

The third type of multilevel inverters is the flying capacitors Multilevel inverter. The first one was shown by Meynard in 1992 , that was followed later by a couple of U.S. patents, which were defined [23], [24] in 1997 and 1998.

Nowadays, multilevel inverters are widely used in high-power applications with medium voltage levels.

2.2. Inverters topologies

2.2.1. Diode clamped inverter

The first diode clamped inverter and also called neutral-point clamped was introduced the first time by Nabae in 1981 and was essentially a three level clamped inverter, where during the off period of the PWM each output terminal will be clamped to the neutral potential [10, 29].

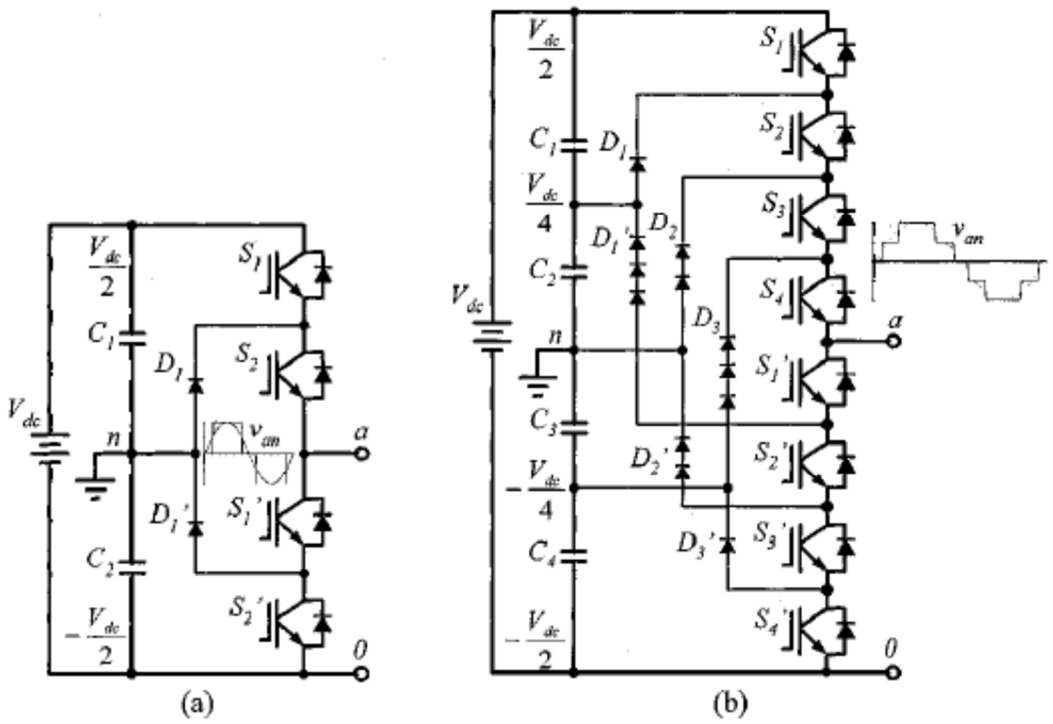


Figure 2.3: Diode-Clamped Multilevel Inverter Circuit Topologies. a) Three Levels. b) Five-Levels.[8]

A three-level diode-clamped inverter is shown in Figure 2.3a.

The two capacitors C_1 and C_2 in place are defining the three levels, $V_{dc}/2$, 0 and $-V_{dc}/2$.

Output level achieved by combining switches S_1,...S_4. D_1 and D_1 ' are the clamping diodes, they limit the stress on the switches when they are in Off position, and limit the output voltage to $V_{dc}/2$.

The contact point between the C_1 and C_2 is the neutral point.

- S_1=ON, S_2= ON $V_{an} = V_{dc}/2$
- S_2=ON, S_1'=ON $V_{an} = 0$
- S_1'=ON S_2'=ON $V_{an} = -V_{dc}/2$

Figure 2b shows the five levels clamping diode inverter. We have 4 capacitors connected, each one will have $V_{dc}/4$.

The staircase is obtained by acting on the switches as per the below table.

Voltage output	Switch Status (ON=1, OFF=0)							
	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

Table 2.1: diode clamped inverter output Voltage Vs switch status

One of the important rules to apply in this case is complementary switch pairs are not to be active at the same time.

S_1, S_1' S_2,S_2' S_3,S3' and S_4,S_4', as activating any combination is an equivalent of short circuit.

Even though each active switching device is only required to block a voltage level of $V_{dc}/4$, the clamping diodes must have different voltage ratings for reverse voltage blocking. as an example, D_1' needs to be able to block $3V_{dc}/4$ when lower devices S2', S3' and S_4' are switched on.

For each leg, an *m* level inverter needs (*m*-1) voltage sources, 2(*m*-1) switching devices and (*m*-1) (*m*-2) diodes. This is a quadratic increase in *m*, for 3 phases we will multiply the previous number by 3. Increasing *m* will significantly increase the number of diodes and will make the system unrealistic to implement.

That is one of the disadvantages and limitation of the diode clamping inverters, as the hardware has a direct impact on the cost of the inverter, another issues has been seen is also the clamping diode reverse recovery under PWM becomes a real challenge in High Voltage and High power application design.

In summary, advantages and disadvantages of a diode-clamp multilevel voltage source converter are as follows [11].

Advantages of the diode clamped inverter:

- When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.
- Efficiency is high because all devices are switched at the fundamental frequency, for the simple staircase waveform.

- Reactive power flow can be controlled.
- The control method is simple for a back-to-back intertie.

Disadvantages of the diode clamped inverter:

- Excessive clamping diodes are required when the number of levels increases.
- clamping diode reverse recovery under PWM.

2.2.2. Flying capacitor inverter (capacitor-clamped inverter)

The first flying capacitors inverter has been introduced by Meynard in 1992. A 3 level topology single phase of this inverter is illustrated on Figure 2.4a. It is similar to the first type but the clamping diodes are replaced by a Capacitor.[29,30].

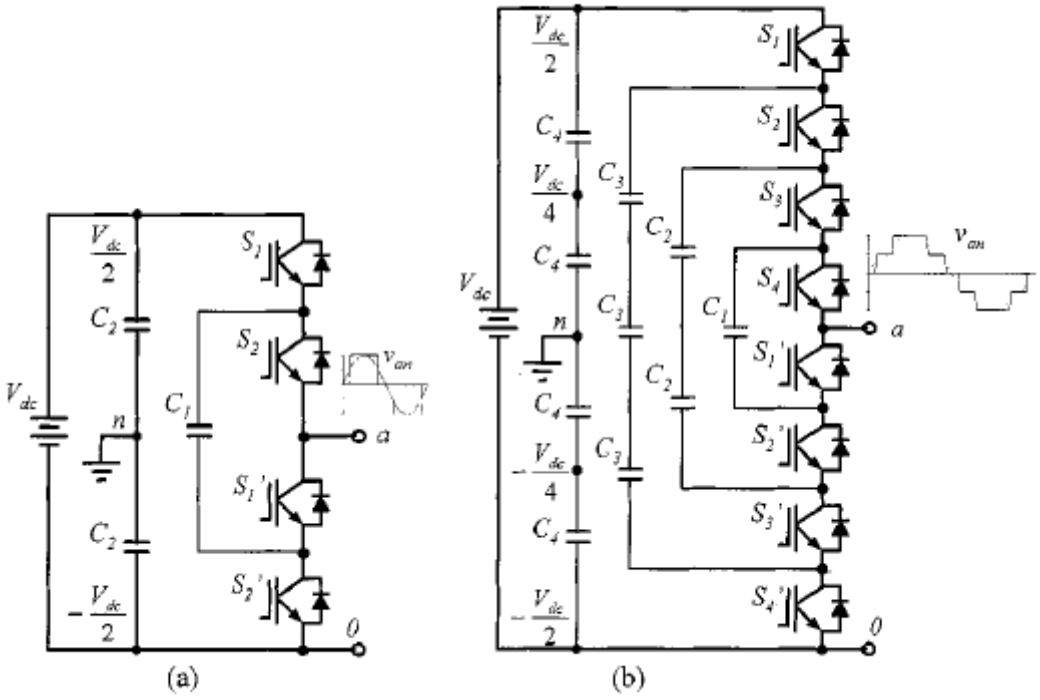


Figure 2.4: Capacitor-clamped multilevel inverter circuit topologies. (a) Three-level. (b) Five-level.[8]

Figure 2.4 shows one phase flying capacitor inverter, or capacitor clamped inverter, for 3 levels and 5 levels inverter. This topology is very similar to the diode clamped inverter, where the clamping diodes are replaced with a clamping capacitors. The inverter in figure 2.4a provides a three-level output across a and *n*, $V_{an}=V_{dc}/2$, 0, or $-V_{dc}/2$.

The contact point between the C1 and C2 is the neutral point.

- $V_{an}= V_{dc}/2$, S_1=ON, S_2=ON.
- $V_{an}= -V_{dc}/2$, S_1'=ON, S_2'=ON.

- V_{an}=0, S_1=ON, S_1'=ON , or S_2=ON and S_2'=ON.

When S_1=ON, S_1'=ON C_1 is in charging, when S_2=ON and S_2'=ON C_1 is discharging.

The charge of C_1 can be balanced by proper selection of the 0-level switch combination.

let us discuss now the 5 levels flying capacitors inverter showed on figure 2.5b, the five levels are $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$ and $-V_{dc}/2$.

The table 2.2 summarizes the output versus the switch combinations.

- Van=$V_{dc}/2$, S_1-S_4=1
- Van=$V_{dc}/4$, we have 4 possible combinations
    1. Switch on S_1,S_2,S_3,S_1' , all the other switches Off. Van= $V_{dc}/2$ of upper C_4 - $V_{dc}/4$ of C_1.
    2. Switch on S_2,S_3,S_4,S_4' , all the other switches off. Van= 3 $V_{dc}/2$ of C_3 - $V_{dc}/4$ of lower C_4.
    3. Switch on S_1,S_3,S_4,S_3' ,all other switches off. V_{an}=$V_{dc}/2$ of upper C_4 - $3V_{dc}/4$ of C_3s+$2V_{dc}/4$ of C_2s
    4. Switch on S_1,S_2,S4,S_2', all other switches off. V_{an}= $V_{dc}/2$ of upper C_4- $2V_{dc}/4$of C_2s+$V_{dc}/4$ of C1.
- Van=0, six combinations are possible.
    1. Switch on S_1,S_2,S_1',S_2', all the other switches off. V_{an}=$V_{dc}/2$ of upper C_4s -$2V_{dc}/4$ of C_2s
    2. Switch on S_3,S_4,S_3',S_4', all the other switches off. V_{an}=$2V_{dc}/4$ of C_2s- $V_{dc}/2$ of C_4.
    3. Switch on S_1,S_3,S_1',S_3', all the other switches off. V_{an}=$2V_{dc}/4$ of C_2s- $V_{dc}/2$ of C_4.
    4. Switch on S_1,S_4,S_2',S3', all the other switches off. V_{an}=$V_{dc}/2$ of upper C_4-$3V_{dc}/4$ of C_3+$V_{dc}/4$ of C_1.
    5. Switch on S_2,S_4,S_2',S_4', all the other switches off . V_{an}=$3V_{dc}/4$of C_3- $V_{dc}/2$ of C_2s+$V_{dc}/4$ of C_1-$V_{dc}/2$ of lower C_4s.
    6. Switch on S_2,S_3,S_1'S_4', all the other switches off. $3V_{dc}/4$ of C_3s-$V_{dc}/4$ of C_1-$V_{dc}/2$ of lower C_4.
- Van=$-V_{dc}/4$, 4 combinations are possible.
    1. Switch on S_1,S_1',S_2',S_3', all the other switches off. V_{an}=$V_{dc}/2$ of upper C4s-$3V_{dc}/4$ of C_3s

2. Switch on S_4,S_2',S_3',S_4', all the other switches off. $V_{an}=V_{dc}/4$ of C_1-$V_{dc}/2$ of lower C_4.
3. Switch on S_3,S_1',S_3',S_4', all the other switches off. $V_{an}=V_{dc}/2$ of C_2s -$V_{dc}/4$of C_1-$V_{dc}/2$ of lower C_4s
4. switch on S_2,S_1',S_2',S_4', $V_{an}= -V_{dc}/2$ of lower C_4s+$3V_{dc}/4$ of C_3s-$2V_{dc}/4$ of C_2s

- $V_{an}=-V_{dc}/2$.one possible combination. Switch on S_1'-S4', all the other switches off. One possible switching sequence is given on table2.2.

Van	Switch ON=1, OFF=0							
	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$-V_{dc}/4$	1	0	0	0	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

Table 2.2: Flying capacitors inverter output Voltage Vs switch status

Table 2.2 lists a possible combination of the voltage levels and their corresponding switch states. Using such a switch combination, in the case of simple staircase wave, each device needs to be switched only once per cycle.

The most important trouble in this inverter is the requirement of a high number of storage capacitors. assuming that voltage rating of all the storage capacitors is the same as the ones used in the main of power switch, an *m*-level converter will require a total of (*m* - 1) x (*m* - 2)/2 auxiliary capacitors per phase leg in addition to (*m* - 1) main dc bus capacitors.

With the same previous assumption, the equivalent m-level diode-clamp inverter requires only (*m* - 1) capacitors.

In the previous description, the capacitors with positive signs are in discharging mode, while those with negative sign are in charging mode.

In order to balance the capacitor charge and discharge, we can consider using two or more switch combinations for middle voltage levels (Vdc/4, 0, and -Vdc/4) in one or several fundamental cycles. Consequently, the selection of the right switch combination can become very complicated, and the switching frequency needs to be higher than the fundamental frequency.

In summary, advantages and disadvantages of a flying capacitor multilevel voltage source converter are as follows.

Advantages of the flying capacitor MLI:

- Large amount of storage capacitors provides extra ride through capabilities during power outage.
- Provides switch combination redundancy for balancing different voltage levels.
- When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.

Disadvantages of the flying capacitor MLI:

- An excessive number of storage capacitors is required when the number of converter levels is high.
- High-level systems are more difficult to package and more expensive with the required large capacitors.

2.2.3. Cascaded H bridge multilevel inverter

The third type is the cascaded H-bridge multilevel inverter, which offers a design with less power devices. This design offers a higher number of levels, but requires an isolated and separated DC source for each H-bridge [8].

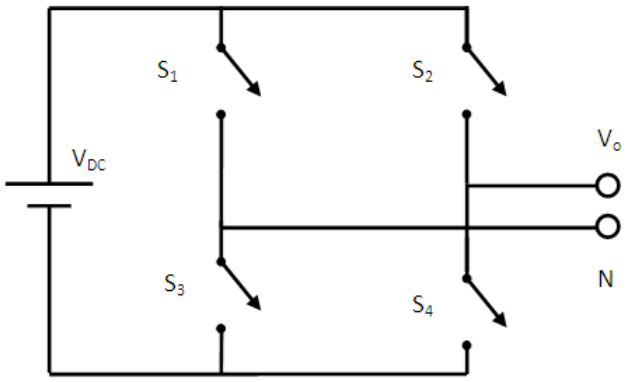


Figure 2.5: Three level H Bridge inverter

This structure has been introduced the first time by Hammond in 1997, Figure 2.5 [8, 14].

The cascaded multilevel inverter has been previously designed for Static VAR compensator and motor drives, but the topology has been also used to interface with renewable energy

sources, because it uses separated dc sources. [8, 29, 14], accordingly, the produced AC voltage is generated by connecting multiple Cells in series. Each cell will generate three levels +*Vdc*, 0 and -*Vdc*. Consequently, connecting *n* cells will generate 2*n* + 1 levels.

Figure 2.6 shows the basic structure of the cascaded-inverters with separated dc sources. One phase leg of a nine-level inverter consists of four cells in each phase, the ac terminal voltages of different level inverters are connected in series..

Figure. 2.5(b) shows the synthesized phase voltage waveform of a 9-level cascaded inverter with four separated dc sources.

The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell.

The Phase output: $V_{an} = V_1 + V_2 + V_3 + V_4$

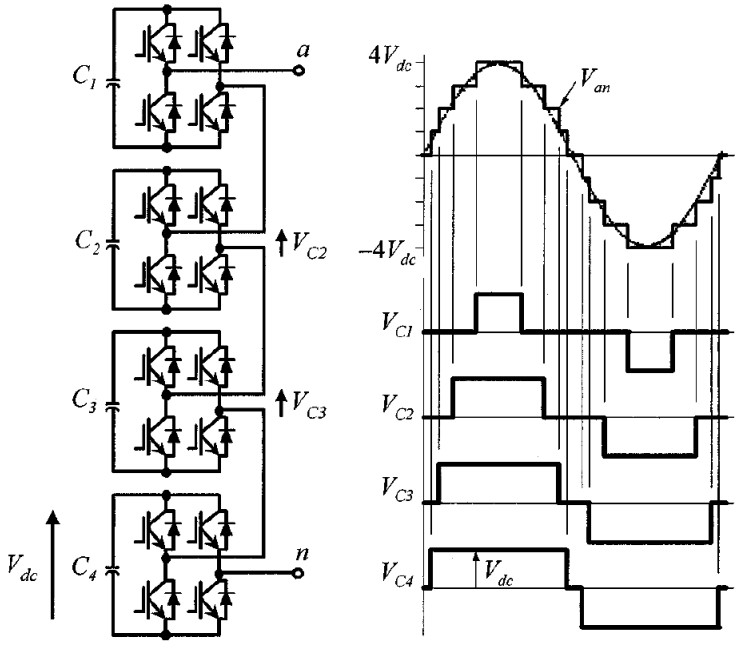


Figure 2.6: Cascaded H bridge inverter circuit topology and its associated waveform [8].

V_i is the output of H-bridge *i* containg capacity C_i.

An H-Bridge consists of a dc power source and 4 switches. Generates three voltages at the output: +Vdc, 0, -Vdc. This is shown on figure 2.7.

V_{dc} is obtained by connecting S_1 and S_4, $-V_{dc}$ is obtained by connecting S_2 and S_3. Zero is obtained by disconnecting all the switches.

The switching angles can be chosen in such a way that the total harmonic distortion is minimized.

For an $_m$ level H-Bridge converter, which contains *k* number of separated sources $m = 2k + 1$, where *m* is the output phase voltage level, and *k* is the number of dc sources. For example, a 9-level cascaded inverters based converter will have four separated dc sources and four H-bridges cells.

This type of inverters, with separated dc sources is well appropriate for various renewable energy sources such as fuel cell, photovoltaic... etc.

Advantages Cascaded H bridge MLI:

- Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.
- Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors.
- Easier control strategy than the diode clamping and flying capacitor.

Disadvantages Cascaded H bridge MLI:

- Needs separate dc sources.

Table 2.3 shows the comparison of power components requirement per phase of the three multilevel inverters presented previously.

The cost of the multilevel inverter will depend on the number of levels, which will dictate the number of switches, diodes , capacitors ...etc , it will also depend on the type of switches , transistors, Thiristors, GTO,...and the power range of all the component in general.

Reducing the number of component will reduce the cost of the multilevel inverter.

Inverter Topology	**diode-clamped**	**Flying-capacitors**	**cascaded H-bridge**
Number of levels	*m*	*m*	*m*
Main switching devices	*2(m-1)*	*2(m-1)*	*2(m-1)*
Clamping diode	*(m-1)x(m-2)*	*0*	*0*
DC bus capacitors (DC sources)	*(m-1)*	*(m-1)*	*(m-1)/2*
Balancing capacitors	0	(m-1)x(m-2)/2	0
Voltage Unbalancing	Average	High	Small

Table 2.3: Comparison table between the main MLI topologies.

2.2.4. Emerging multilevel inverter topology

2.2.4.1. Mixed-level Hybrid Multilevel cells

For some high-voltage high-power applications, it is possible to have a hybrid configuration, H-bridge cell in a cascaded inverter, with a diode clamped inverter or a flying capacitor inverter [25].

The reason for doing so is to reduce the amount of separate dc sources. The nine-level cascaded inverter shown in figure. 2.6 requires four separate dc sources for one phase leg. If a three-level inverter replaces the H-bridge block, the voltage level is doubled for each block. Consequently, a nine-voltage levels inverter will require only two separate dc sources. This is shown on figure 2.7. [8].

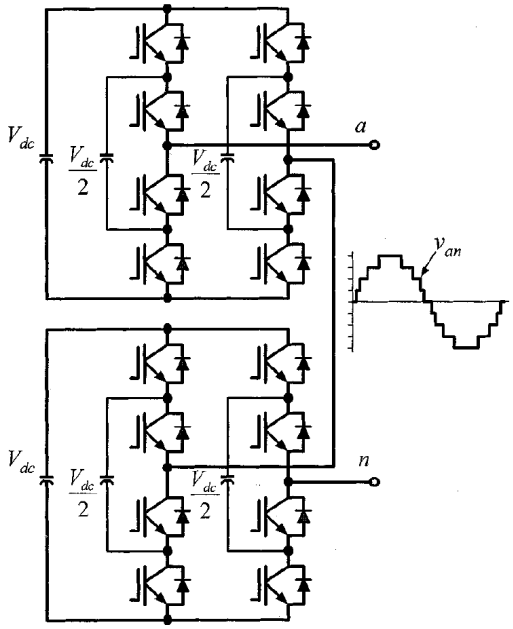


Figure 2.7: A mixed-level hybrid cell configuration using the thee-level diode-clamped inverter & the cascaded inverter cell to increase the voltage levels [8].

Figure 2.7 shows the nine-level cascaded inverter incorporating a three-level flying capacitor inverter as the cell. It is obvious that a diode-clamped inverter can replace the flying capacitor inverter in the previous configuration.

2.2.4.2. Asymmetric hybrid multilevel inverters

In previously presented topologies, the dc sources were assumed to be identical and can generate equal dc voltage. On the other hand, it is possible to have dc sources with unequal output. [26], [27], and the new topology can be called asymmetric hybrid multilevel inverter. Figure 2.8 shows an example of having two different sources and consequently two different levels.

This element allows more levels to be created at the output voltage, and consequently can reduce the THD with less cells.

Another variant can be seen, with the same voltage level on all dc sources , high-frequency PWM for one block can be considered , or all of them .

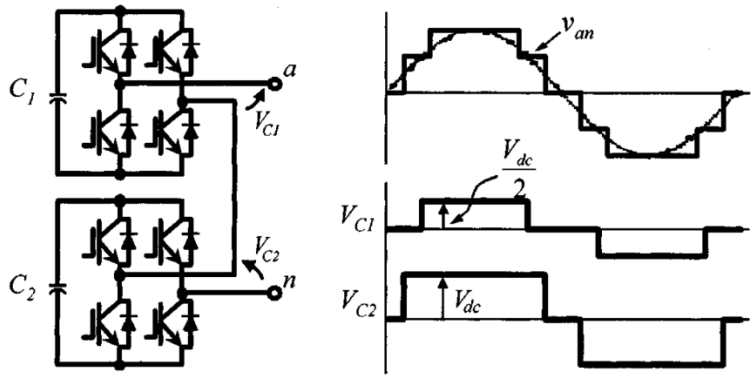


Figure 2.8: Asymmetric cascaded inverter cell arrangement with different voltage levels [8].

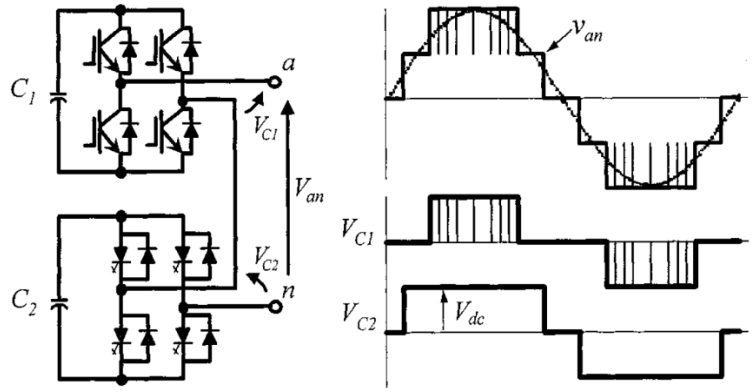


Figure 2.9: Asymmetric cascade inverter cell arrangement with different switching frequencies [8].

Figure 2.9 shows an example with two different devices. The top full-bridge cell uses the insulated gate bipolar transistor (IGBT), and the low cell uses the gate-turn-off thyristor

(GTO) as its switching device. The GTO-based cell switches at a lower frequency, typically the fundamental frequency, and the IGBT-based cell switches at a PWM frequency to smooth the waveform [26], [27].

2.3. Conclusion

In this chapter, we have presented a summary of the three main topologies of the multi levels inverters, diode clamped inverter or neutral-point clamped (NPC) inverter, Flying capacitor inverter (capacitor-clamped inverter) and Cascaded H bridge multilevel inverter.
We have drilled down to the earliest MLI presented by Baker in 1975. We have also presented some of the emerging topologies, asymmetric and symmetric dc sources and the hybrid topologies.
Following the comparison table we see that the CHB has offered new ways and new options, seems to be the correct choice in some applications, like renewable energies, when we have independent cells.

Chapter 3

State of the art2- PWM controls and strategies

3.1 Introduction:

In this chapter we will present the most relevant control and modulation methods developed for the multilevel inverters, multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, space-vector modulation, space vector control , One-Dimensional Modulation and our proposed method Minimum THD PWM ,published in 2017 [31].

we have developed into some extend to make this thesis a good support for our student, references are also clearly cited in case someone wants to develop the subject more.

3.2. PWM control methods

Classifying the multilevel inverters can be done based on the operating frequency, where The modulation methods used in multilevel inverters can be classified according to the switching frequency, as shown in figure 3.1. [8], [9], [32] and [33].

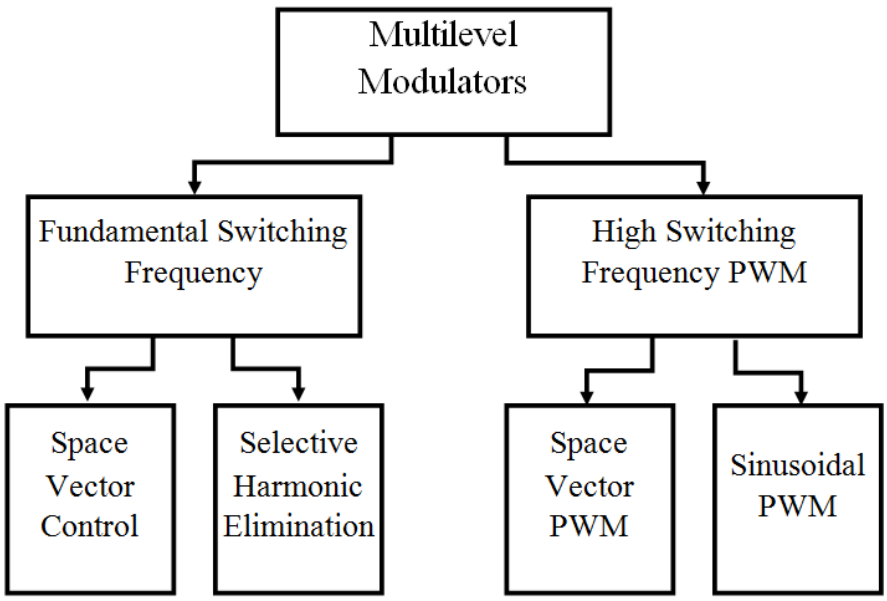


Figure 3.1: Classification of modulation strategies.

We distinguish two main classes, the first one is the Fundamental switching frequency, methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform.

Representatives of this family are the multilevel selective harmonic elimination [34], [35] and the space-vector control (SVC) [36].

The second class is the high switching frequency PWM, have many commutations for the power semiconductors in one period of the fundamental output voltage.

A common method used in many applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage [37], [38], [39].

The Space Vector Modulation strategy is an additional alternative method, and has been initially used for controlling the three-level inverters [33].

The quality of the output signal does not depend only on the topology of the inverter , but depends also on the number of switches and the switch type, within the topology, and more important determined by the way of controlling the individual switches, the manner or the strategy of acting on the switches must have a direct impact on the quality of the signal and will improve or degrade the THD.

3.2.1. Sine-Triangle PWM

This method was first presented by Bowes in 1975, [40] and [41], where the first 2-levels inverter has been presented. Figure 3.2 illustrates the output signal and the building blocks of a 2-level uniform-sampled PWM, in 1981 there was the introduction of the Microcontroller to generate the signal, instead of using complex logic circuits [41].

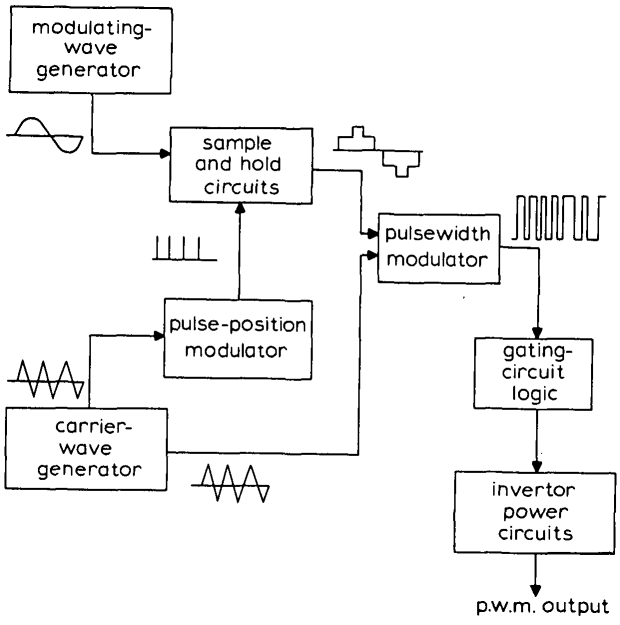


Figure 3.2: 2-level uniform-sampled PWM [40].

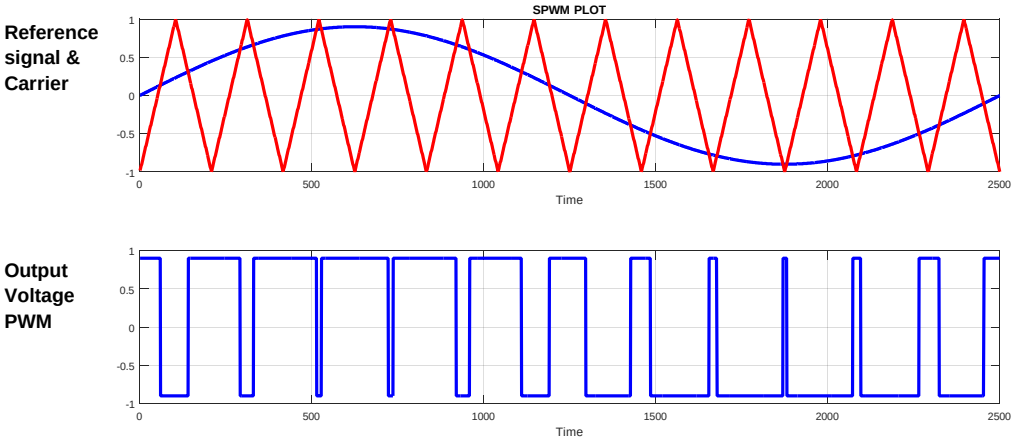


Figure 3.3: Sine-triangle PWM

The output control signals are generated by comparing a sampled sinusoidal reference signal with a triangular carrier, this is shown on figure 3.3.

When the reference is superior than the triangular carrier level, the dc link is connected to the output via the upper switch, otherwise the lower-side switch is connected to the output, that is the negative dc link potential.

The switching frequency is defined by the carrier frequency, while the output amplitude is controlled through the reference sinusoid amplitude.

The two key control parameters related to the SPWM are the amplitude modulation index and the frequency modulation index.

The amplitude modulation index is the ratio of reference peak-to-peak to the dc link voltage

The frequency modulation index is the ratio of carrier frequency to reference frequency.

When we have a multilevel inverter, The SPWM MLIs can be categorized into two groups depending on the control strategy , both cases use a reference signal , to generate the MLI control , we either use carrier disposition where each carrier covers a level of voltage , this is the case shown on figure 3.4 , or use phase shifting, this is shown on figure 3.5 . Each one can have slightly different performance.

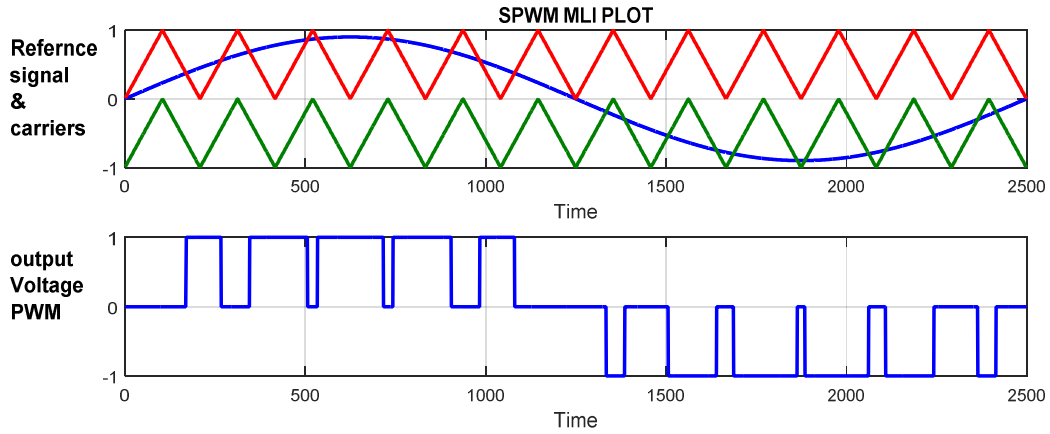


Figure 3.4: 3 levels - In phase disposition SPWM waveforms (m_a = 0.9, m_f = 12)

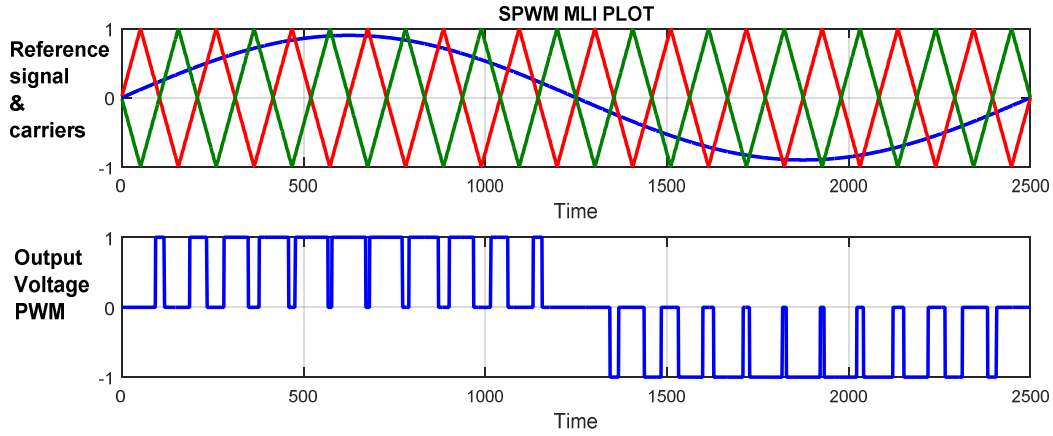


Figure 3.5: 3 levels - Phase shifted SPWM waveforms (m_a = 0.9, m_f = 12)

3.2.2. Selective Harmonic elimination

Ideally, the applications of the multilevel inverters require the output voltage to be a pure sin wave, the selective harmonic elimination method (SHE), was one of the earliest control techniques, in order to eliminate some unwanted harmonic components in the two level inverter. That is achieved by calculating the switching angles of each thyristor. The work published by Turnbull in 1964 was one of the earliest papers on the subject [42], that was investigated further by Patel and Hoft [43],[44]. In 2004 Chiasson et al. have published a very good paper about the Harmonic Elimination Problem [45] , by a mathematical modeling the problem ,they have converted the transcendental equations that specify the harmonic elimination into an equivalent set of polynomial equations. New set of solution were found and presented.

The multilevel inverters offers an easier way to produce a close signal to the sinusoid, and that is accomplished by applying across the load a certain level during a calculated period or angle during the cycle.

The angles where each level is applied is computed in order to achieve the condition of being as close as possible to the sinusoid.

Nabae has introduced this approach with the NPC Inverter in 1981 [46], additional control schemes were also presented in different papers additional , PWM switching on the individual levels, like the work presented by Sirisukprasert in [35] , the work can be extended further by additional switching sequences within each voltage level , and or , using non-equal DC sources. [47] and [48].

The first step is to build the model, by choosing the switching angles we aim to eliminate a preselected Harmonics.

A typical 3 levels inverter with K switching angles can be represented as per figure 3.6, in general a number K of switching Angles will allow elimination of K-1 Harmonics, and the THD is not necessarily at the minimum value.

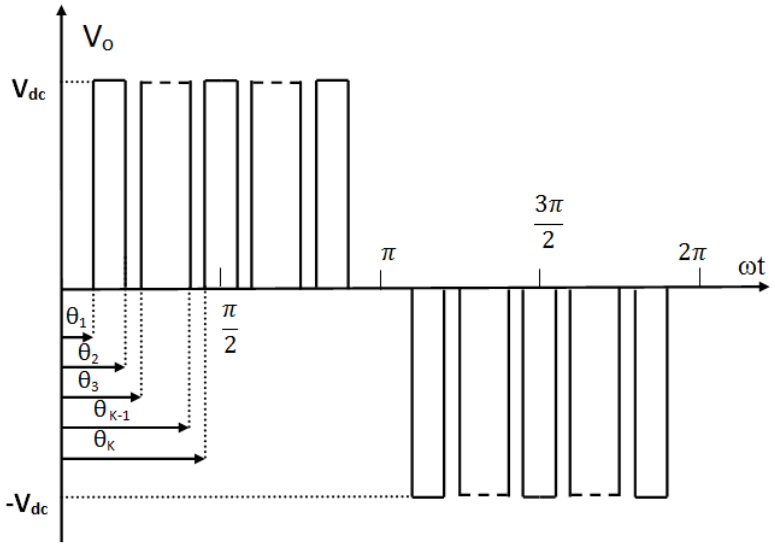


Figure 3.6: Typical 3 levels inverter with K switching angles

$$f(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4Vdc}{n\pi} \left[\sum_{i=1}^{k} (-1)^{i+1} \cos(n\theta_i)\right] \sin n\omega t \quad (3.1)$$

$$THD(\theta_1, \theta_2, \theta_3 \dots \theta_k) = \sqrt{\frac{V_3^2 + V_5^2 + V_7^2 + \cdots .. V_n^2}{V_1^2}} \times 100 \quad (3.2)$$

Applying the case where we have only 3 switching angles,

We can write:

$$f(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4Vdc}{n\pi} [\cos(n\theta_1) - \cos(n\theta_2) + \cos(n\theta_3)] \sin n\omega t \quad (3.3)$$

We can write the following equations:

$$cos(\theta_1) - \cos(\theta_2) + \cos(\theta_3) = \frac{V_1 \pi}{4Vdc} \quad (3.4)$$

$$\cos(3\theta_1) - \cos(3\theta_2) + \cos(3\theta_3) = 0 \quad (3.5)$$

$$\cos(5\theta_1) - \cos(5\theta_2) + \cos(5\theta_3) = 0 \quad (3.6)$$

By solving the system of equations (3.4),(3.5) and (3.6), the solution will fulfil the requirements of having V_3 and V_5 equal to zero.

The algorithm has been implemented on Matlab to illustrate the SHE, transcendental equations in equation (3.4) to (3.6) have been resolved and plots are shown on figure 3.7, to not that the overall THD is at 40%.

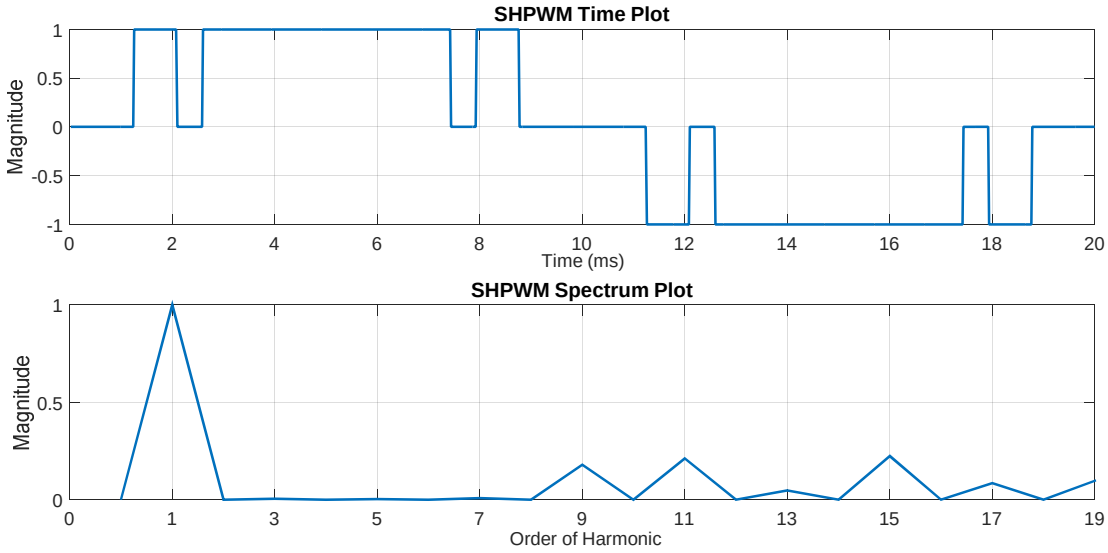


Figure 3.7: Selective Harmonic Elimination, 3rd and 5th harmonics eliminated. (THD=40%)

On figure 3.8 we have chosen to eliminate 4 harmonics, therefore we require 5 Angles, the overall THD is 37%.

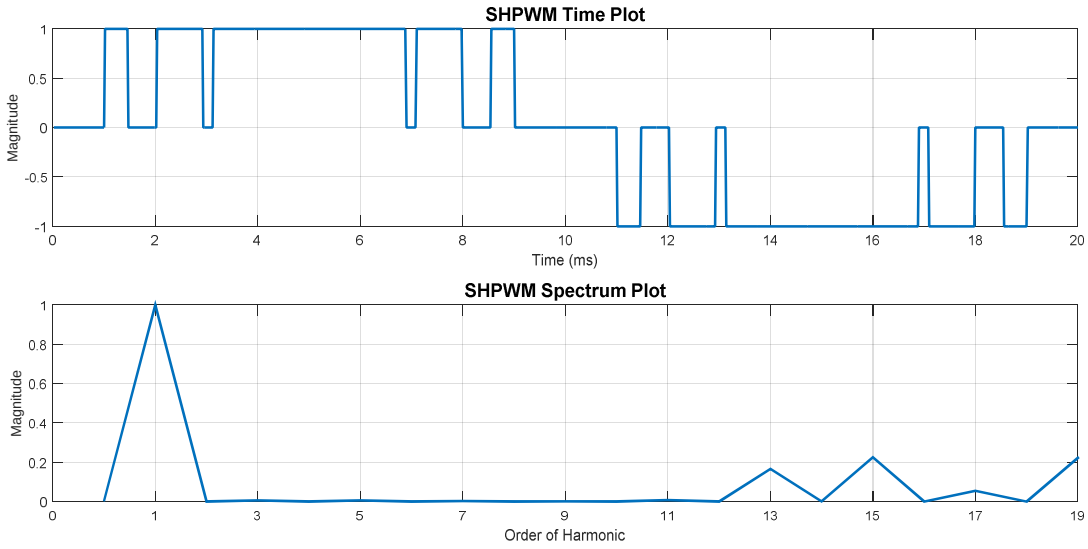


Figure 3.8: Selective Harmonic Elimination, 3rd to 9th Harmonic eliminated.

On the same subject, if we change the strategy for going from three levels to multilevels inverters, the target signal will look like a basic staircase as shown on figure 3.9. In other words, figure 3.9 is showing a typical 2K+1 levels, basic staircase MLI output voltage waveform.

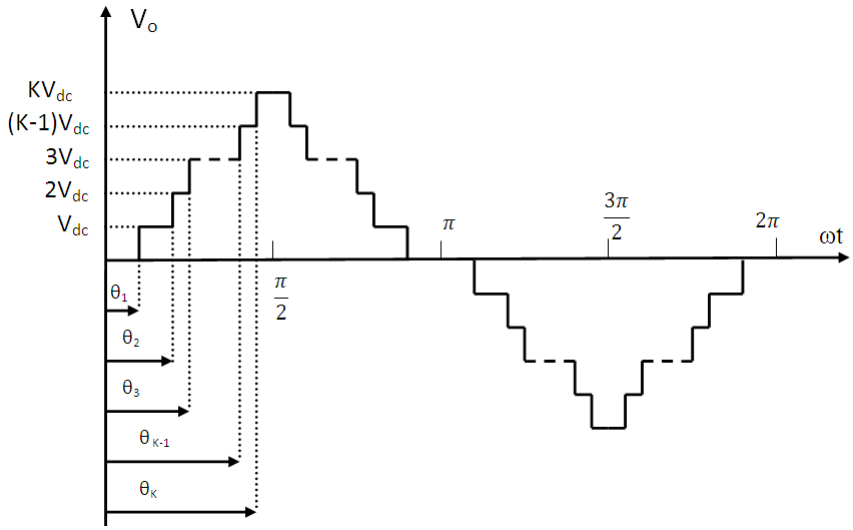


Figure 3.9: Typical 2K+1 Multilevel inverter output waveform.

Where $\theta_1, \theta_2 \ldots \theta_K$ are the switching angles, $\theta_1 < \theta_2 < \ldots < \theta_K < \pi/2$. [49]

Since this function is periodic, as per Fourier theory the function can be expressed by a sum of sines and cosines

The output voltage function can be expressed by:

$$f(t) = a_0 + \sum_{n=1}^{\infty} An\ cos(n\omega t) + Bn\ sin(n\omega t) \quad (3.7)$$

Where:

$$\omega = \frac{2\pi}{T} \quad (3.8)$$

T is the period of the function.

The reference signal is half wave symmetry and odd at the same time, therefore we can write it as:

$$f(t) = \sum_{n=1}^{\infty} Bn \sin(n\omega t) \quad (3.9)$$

$$Bn = \frac{8}{T}\int_0^{\frac{T}{4}} f(t).\sin n\omega t.\, dt \quad (3.10)$$

For odd ns, Zero for the others.

$$Bn = \frac{4Vdc}{n\pi}\sum_{i=1}^{K} \cos n\theta i \quad (3.11)$$

For odd ns, and zero for even ns. [49] and [50].

K is the number of switching angles.

$$f(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4Vdc}{n\pi}[\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_K)]\sin n\omega t \quad (3.12)$$

Our objective is to have a pure sine wave at the output. Therefore, It is possible to find the angles $\theta_1<\theta_2<\ldots<\theta_K<\pi/2$, in order to eliminate the lower order harmonics and have the THD at minimum (ideally zero). The desired output signal is in equation (3.13).

$$f(\omega t) = V_1\ sin\ \omega t \quad (3.13)$$

V_1 is the fundamental.

Actually, this will be achieved by targeting maximum value of V_1, and minimize the amplitude of the other harmonics. In order to solve our problem we have gathered all the parameters in the system of equations (3.14). [49] and [50].

$$\left.\begin{aligned} B_1 &= \frac{4Vdc}{\pi}\sum_{i=1}^{K} cos\ \theta_i = V_1 \\ B_3 &= \frac{4Vdc}{3\pi}\sum_{i=1}^{K} \cos 3\theta_i = V_3 \\ B_5 &= \frac{4Vdc}{5\pi}\sum_{i=1}^{K} \cos 5\theta_i = V_5 \\ &\vdots \\ B_n &= \frac{4Vdc}{n\pi}\sum_{i=1}^{K} \cos n\theta_i = V_n \end{aligned}\right\} \quad (3.14)$$

For n=1,3,5……∞ (for odd ns), Zero for the others.

One solution set is found by zeroing the K-1 equations, in (3.14). Where $\theta_1<\theta_2<\ldots<\theta_k<\pi/2$.

As an example ,for K=6, The target solution will eliminate all the harmonics up to the 11th one, (3,5,7,9,11) or we can select 5 harmonics to be zeroed for example 5,7,11,13,19....

The methods used to find solution are including but not limited to iterative approaches and optimization methods [50].

In order to process the optimization and find the best angles, we need to define an objective function , this one will need to maintain the fundamental harmonic at maximum , and minimize the effects of the other harmonics up to a predefined range, under the constraint $\theta_1<\theta_2<\ldots<\theta_k<\pi/2$.

The Total Harmonic Distortion (THD) is given on equation (3.2):

$$THD(\theta_1,\theta_2,\theta_3\ldots\theta_k)=\sqrt{\frac{V_3^2+V_5^2+V_7^2+\cdots..V_n^2}{V_1^2}}\times 100 \quad (3.2)$$

By reducing the THD, we ensure that our signal strongest contributor is coming from the first harmonic.

In the selective harmonic elimination, we will target harmonics to eliminate, when we have *k* angles we can only eliminate K-1 harmonics.

For 7 levels inverter we can simply write:

K=3,

$$\frac{4Vdc}{\pi}(cos(\theta_1)+cos(\theta_2)+\cos(\theta_3))=V_1 \quad (3.15)$$

$$\frac{4\mathrm{Vdc}}{3\pi}(cos(3\,\theta_1)+cos(3\theta_2)+\cos(3\theta_3))=V_3 \quad (3.16)$$

$$\frac{4\mathrm{Vdc}}{5\pi}(cos(5\,\theta_1)+cos(5\theta_2)+\cos(5\theta_3))=V_5 \quad (3.17)$$

We also consider that:

$$V_1=3V_{dc} \quad (3.18)$$

$$cos(\theta_1)+cos(\theta_2)+\cos(\theta_3)=\frac{3\pi}{4} \quad (3.19)$$

$$cos(3\,\theta_1)+cos(3\theta_2)+\cos(3\theta_3)=0 \quad (3.20)$$

$$cos(5\,\theta_1)+cos(5\theta_2)+\cos(5\theta_3)=0 \quad (3.21)$$

This will eliminate the 3rd and the 5th and Total THD is: 9%

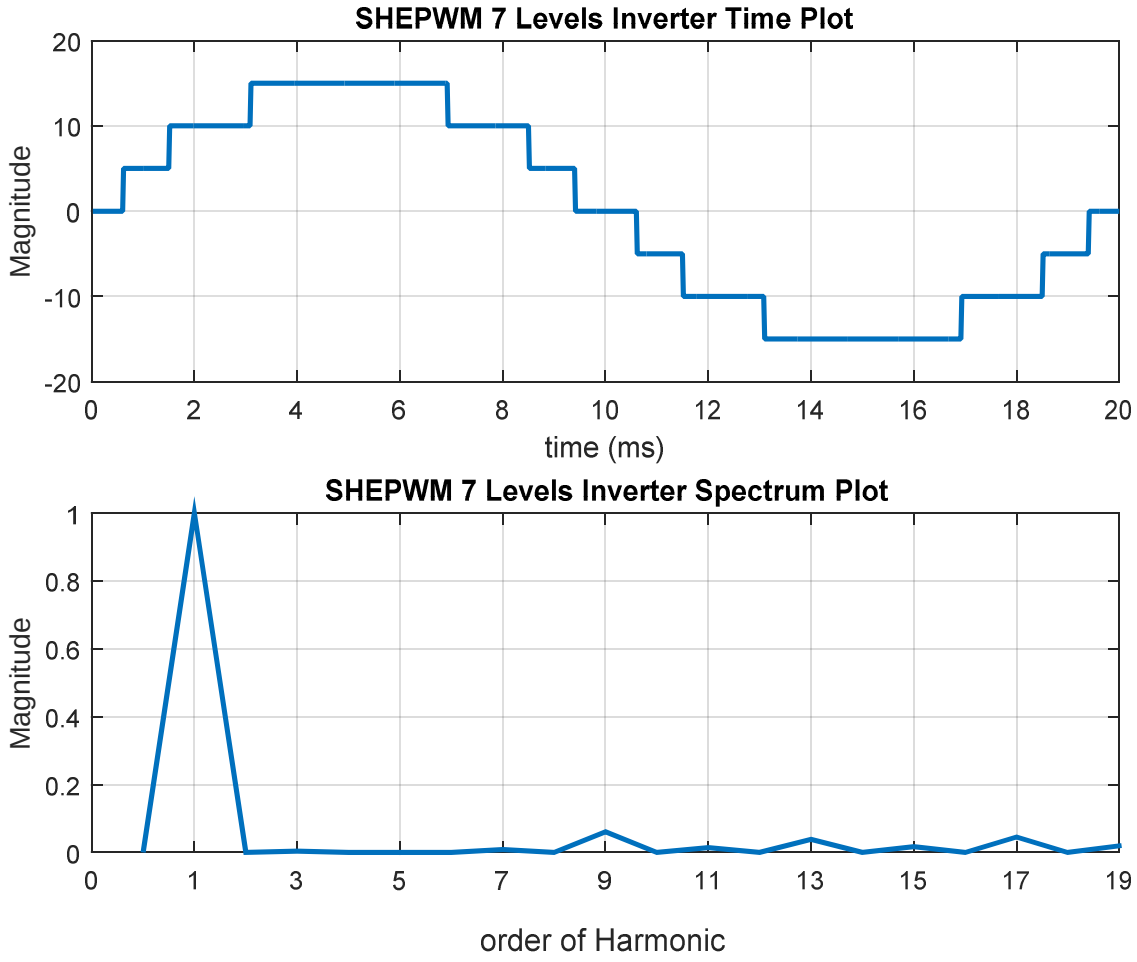


Figure 3.10: SHE of 7 levels MLI, elimination of 3rd and 5th harmonics. Time domain and spectrum

3.2.3. Space Vector PWM or Space Vector Modulation (SVM)

The space Vector PWM (SVPWM) is another control method presented the first time by H. van der Broeck, H.-C. Skudelny, and G. Stanke. This method was mainly designed to drive 3 Phased induction motors. [51].

The aim of the SVPWM is to compose the desired drive space vector voltage by applying a switching pattern on the system phases. The calculation of the switching timing is performed in the α-β space vector plane, based on the Clarke Transform developed by lady Edith Clark in 1938.[52].

The circuit in figure 3.11 shows the basic of a two-level voltage source converter. It has six switches (S_1-S_6).

Va, *Vb* and *Vc* are the sinusoidal output of the three Phase system.

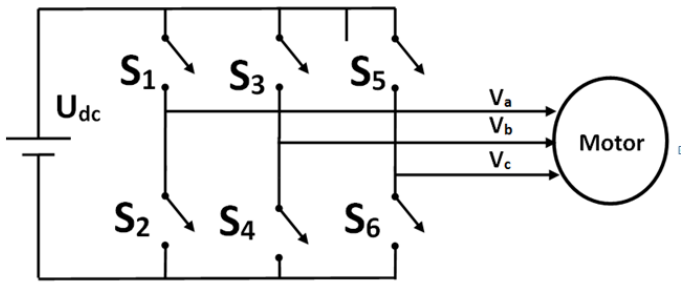


Figure 3.11: Basic three Phase two levels inverter.

Depending on the switching combination, the inverter will produce different outputs, creating the two-level signals.

The principle of the SVPWM is based on representing the control signal V_{ref} as a space vector, figure.3.12. shows V_{ref} and the Space voltage vectors in different sectors.

Assuming that the switches of the same phase can only operate in complementary mod , A three-phase inverter has only eight possible switching combinations. [51] . in other words the control signals of the switches of the same phase are out of phase they are never both “ON” or both “OFF” at the same time.

The three switching arms of the inverter will have eight base states as shown in figure 3.12. They will be represented by 8 vectors, where 2 vectors are zero length vectors. We are assuming a balanced system. This can more clearly be seen in Table 1.

Switching State	power Switch status			Phase			Space Vector
	S_1-S_2	S_3-S_4	S_5-S_6	V_a	V_b	V_c	
0	00	00	00	0	0	0	V_0
1	10	01	01	1	0	0	V_1
2	10	10	01	1	1	0	V_2
3	01	10	01	0	1	0	V_3
4	01	10	10	0	1	1	V_4
5	01	01	10	0	0	1	V_5
6	10	01	10	1	0	1	V_6
7	10	10	10	1	1	1	V_7

Table 1: Switching States for three phase three level Inverter

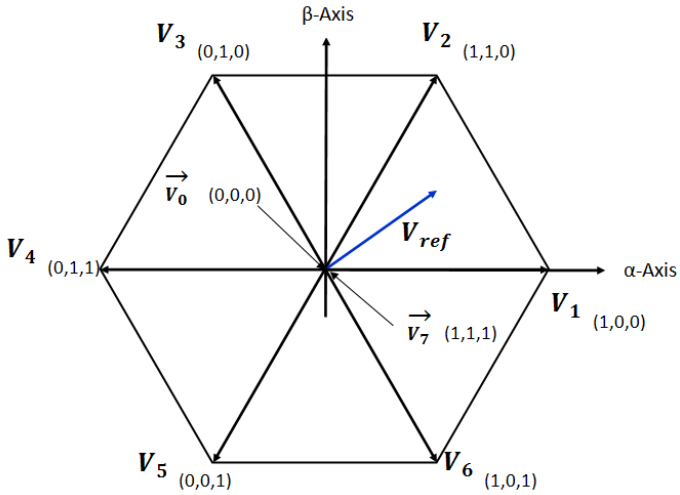


Figure 3.12: Space voltage vectors in different sectors

The system is assumed balanced therefore:

$$V_a + V_b + V_c = 0 \tag{3.22}$$

Where V_a, V_b and V_c are the three phases vectors.

In the time domain, we can write the below:

$$V_a = Vsin(\omega t) \tag{3.23}$$

$$V_b = Vsin(\omega t + \frac{2\pi}{3}) \tag{3.24}$$

$$V_c = Vsin(\omega t + \frac{4\pi}{3}) \tag{3.25}$$

When the three phases are applied on AC motor a rotating flux will be generated, this flux will be represented by a rotating vector , the angular speed is ω, the angle and the magnitude can be calculated through Clark Transform:

$$V_{ref} = V_\alpha + jV_\beta = \frac{2}{3}(V_a + aV_b + a^2V_c) = |V_{ref}|e^{j\theta} \tag{3.26}$$

Where:

$$a = e^{j\frac{2\pi}{3}} \tag{3.27}$$

Therefore:

$$|V_{ref}| = \sqrt{{V_\alpha}^2 + {V_\beta}^2} \tag{3.28}$$

$$\theta = tan^{-1}\frac{V_\beta}{V_\alpha} \tag{3.29}$$

Developing the below, and replacing *Va*, *Vb* and *Vc*:

$$V_\alpha + jV_\beta = \frac{2}{3}(V_a + aV_b + a^2V_c) \tag{3.30}$$

This can be expressed as per equation (3.31)

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{3.31}$$

By developing, we can have:

$$V_\alpha = \frac{2}{3}(V_a - \frac{1}{2}V_b - \frac{1}{2}V_c) \tag{3.32}$$

$$V_\beta = \frac{2}{3}(\frac{\sqrt{3}}{2}V_b - \frac{\sqrt{3}}{2}V_c) \tag{3.33}$$

Knowing V_α andV_β from equation (3.32) and (3.33), we will be able to calculate $|V_{ref}|$ and θ, from equations (3.28) and (3.29).

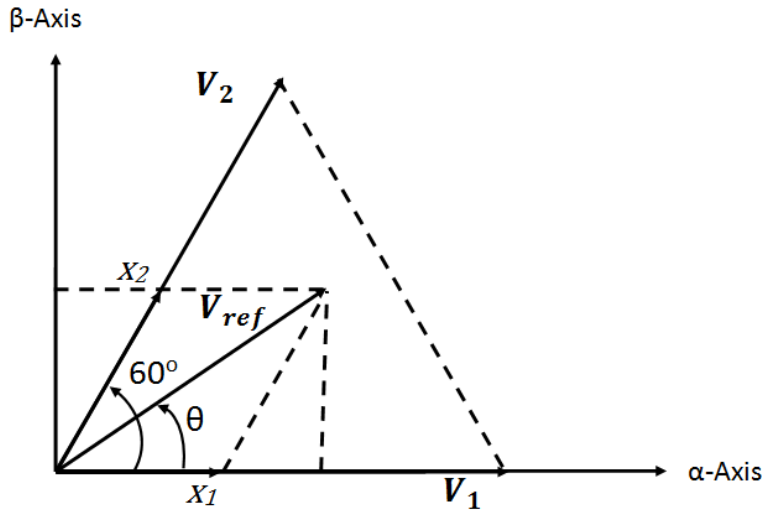


Figure 3.13: Reference Vector using base vectors of first sector

In order to obtain the reference voltage we need to combine V_1 and V_2, as illustrated on figure 3.13.

$$Vref = X_1V_1 + X_2V_2 \tag{3.34}$$

This can be done by activating V_1 during T_1 and V_2 during T_2, the period is T, if $T_1+T_2<T$, we need to activate the zero vector during T_0,

$$T_0 = T - (T_1 + T_2) \tag{3.35}$$

During T_1 $V_{ref} = V_1$, during T_2 $V_{ref} = V_2$ the rest is the 0.

$$\int_0^{\mathrm{T}} \mathrm{V_{ref}dt} = \int_0^{\mathrm{T_1}} \mathrm{V_{ref}dt} + \int_{\mathrm{T_1}}^{\mathrm{T_2}} \mathrm{V_{ref}dt} + \int_{\mathrm{T_2}}^{\mathrm{T}} \mathrm{V_{ref}dt} \tag{3.36}$$

Therefore:

$$TV_{ref} = T_1V_1 + T_2V_2 + T_0V_0 \tag{3.37}$$

As a result:

$$V_{ref} = \frac{T_1}{T}V_1 + \frac{T_2}{T}V_2 \tag{3.38}$$

$$X_1 = \frac{T_1}{T} \tag{3.39}$$

$$X_2 = \frac{T_2}{T} \tag{3.40}$$

$$T\left|V_{ref}\right|\begin{bmatrix}cos(\alpha)\\ sin(\alpha)\end{bmatrix} = T_1|V_1|\begin{bmatrix}cos(0)\\ sin(0)\end{bmatrix} + T_2|V_2|\begin{bmatrix}cos\left(\frac{\pi}{3}\right)\\ sin\left(\frac{\pi}{3}\right)\end{bmatrix} \tag{3.41}$$

Thus:

$$T\left|V_{ref}\right|\begin{bmatrix}\cos(\alpha)\\ \sin(\alpha)\end{bmatrix} = T_1|V_1|\begin{bmatrix}1\\ 0\end{bmatrix} + T_2|V_2|\begin{bmatrix}\frac{1}{2}\\ \frac{\sqrt{3}}{2}\end{bmatrix} \tag{3.42}$$

$$|V_1| = |V_2| = |V| = \frac{2}{3}U_{dc} \tag{3.43}$$

Udc is the dc link Voltage, the ratio $\frac{2}{3}$ is coming from the fact that the two-phase Space Vector Modulation provides a 33% reduction of effective switching frequency. [67] Consequently equation (3.42) can be developed as follows:

$$T\left|V_{ref}\right| cos(\alpha) = T_1V + T_2Vcos\left(\frac{\pi}{3}\right) \tag{3.44}$$

$$T\left|V_{ref}\right| sin(\alpha) = T_2Vsin\left(\frac{\pi}{3}\right) \tag{3.45}$$

$$T_2 = T\frac{|V_{ref}|}{V}\frac{sin(\alpha)}{sin(\frac{\pi}{3})} \tag{3.46}$$

Substituting the value of T2 in equation (3.35), we obtain:

$$T\left|V_{ref}\right| \cos(\alpha) = T_1V + T\frac{|V_{ref}|}{V}\frac{sin(\alpha)}{sin(\frac{\pi}{3})}V\cos\left(\frac{\pi}{3}\right) \tag{3.47}$$

$$T_1V = T\left|V_{ref}\right| \cos(\alpha) - T\frac{\left|V_{ref}\right|}{V}\frac{sin(\alpha)}{sin(\frac{\pi}{3})}V\cos\left(\frac{\pi}{3}\right) \quad (3.48)$$

$$T_1V = T\left|V_{ref}\right| \cos(\alpha) - T\left|V_{ref}\right|\frac{sin(\alpha)}{sin(\frac{\pi}{3})}\cos\left(\frac{\pi}{3}\right) \quad (3.49)$$

$$T_1 = T\left|\frac{V_{ref}}{V}\right| \cos(\alpha) - T\left|\frac{V_{ref}}{V}\right|\frac{sin(\alpha)}{sin(\frac{\pi}{3})}\cos\left(\frac{\pi}{3}\right) \quad (3.50)$$

$$T_1 = T\left|\frac{V_{ref}}{V}\right|\left(\cos(\alpha) - \frac{sin(\alpha)}{sin(\frac{\pi}{3})}\cos\left(\frac{\pi}{3}\right)\right) \quad (3.51)$$

$$|V| = \frac{2}{3}U_{dc} \quad (3.52)$$

$$T_1 = T\sqrt{3}\left|\frac{V_{ref}}{u_{dc}}\right|\sin\left(\frac{\pi}{3} - \alpha\right) \quad (3.53)$$

$$T_2 = T\sqrt{3}\left|\frac{V_{ref}}{u_{dc}}\right|\sin(\alpha) \quad (3.54)$$

T_0 Is obtained from (3.36),

$$T_0 = T - (T_1 + T_2) \quad (3.55)$$

That can be symmetrical or asymmetrical, and the zero can be the result of V_0 (0 0 0) or V_7 (1 1 1) .

As long as we keep the equations (3.35) satisfied, we can think about other ways of distributing T_1, T_2 and T_0.

The best is to keep a certain symmetry around the zero, we need to remember that the zero can be represented by either V0 or V7, the choice will be dictated by the previous and the succeeding status , where only one inverter leg switches between each transition, resulting in minimum switching frequency in the three-phase modulation case.[53]

$T_0/3$, and make $T_1/2$ and $T_2/2$ in between.

Sequence of activating will be as follows, 000 100 110 111 110 100 000, during the associated time, and T will be written as per equation (3.56)

$$T = T_0/3 + T_1/2 + T_2/2 + T_0/3 + T_2/2 + T_1/2 + T_0/3 \quad (3.56)$$

These results mean that an arbitrary space vector within the triangle defined by the two adjacent base vectors, between which the expected vector is located, can be represented by the sum of these two vectors. This is realized by timely activating the two vectors combined with zero vectors sequentially. If the switching process is fast enough, meaning the period *T*

is short, the approximation can precisely represent the reference vector. Figure 3.14 shows the switching sequence of the space vector modulation when Vref is in sector1.

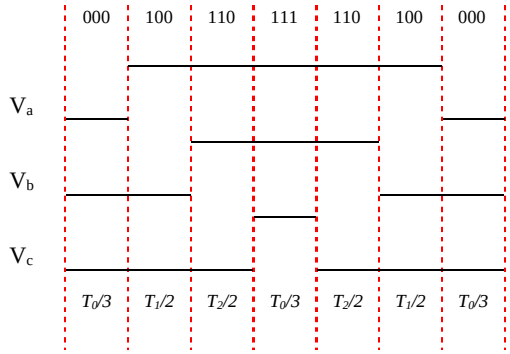
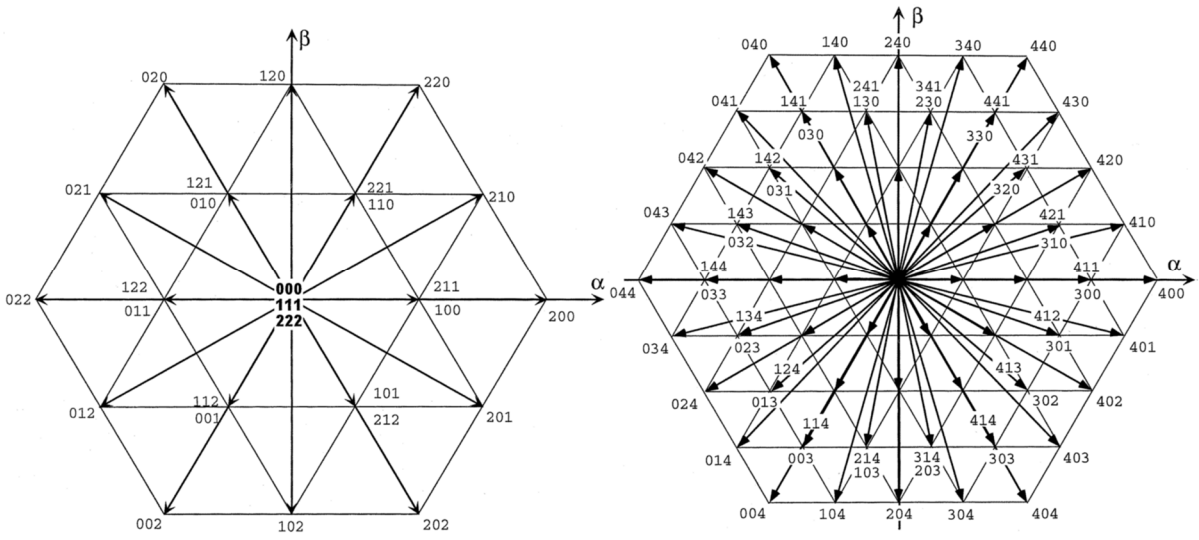


Figure.3.14: Switching sequence of SVM , V_{ref} in Sector 1.

Space-vector modulation is a regularly-sampled modulation technique for three phase inverters. Instead of modulating each phase leg inverter individually, the space Vector Modulation selects switching states of the entire three-phase converter based on a mathematical transformation of the reference and of the line voltages generated by each switching state. [53].

The SVM technique can be easily extended to all multilevel inverters [54- 60].

Figure 3.15 shows space vectors for the traditional three, and five-level inverters. [55]



(a) (b)

Figure 3.15:

(a) Space vector states for three-level diode clamped converter.

(b) Space vector states for five-level diode clamped converter. [55].

These vector diagrams are universal regardless of the type of multilevel inverter.

In other words, figure 3.14(b) is valid for five-level diode-clamped, capacitor-clamped, or cascaded inverter. The adjacent three vectors can synthesize a desired voltage vector V_{ref} by computing the duty cycle of the adjacent vectors.

Space-vector PWM methods generally have the following features:

- Good utilization of dc-link voltage, low current ripple, and relatively easy hardware implementation by a digital signal processor (DSP). These features make it suitable for high-voltage.
- High-power applications.
- As the number of levels increases, redundant switching states and the complexity of selecting switching states increase dramatically.

3.2.4. Space Vector Control

A conceptually different control method for multilevel inverters, based on the space-vector theory, a simple space-vector selection method was introduced without duty cycle computation of the adjacent three vectors [33][36].

This control strategy, called SVC, works with low switching frequencies and does not generate the mean value of the desired load voltage in every switching interval, as is the principle of SVM. The SVC main goal is to deliver the load a voltage Vector that minimizes the space error or distance to the reference vector.

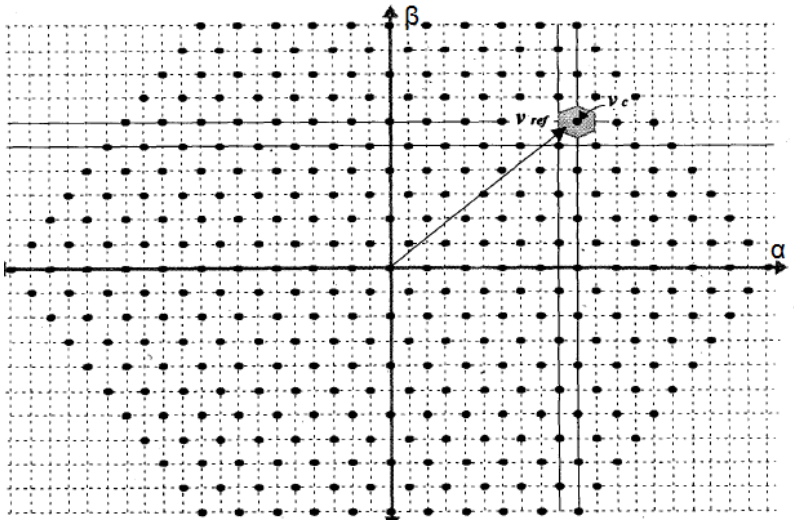


Figure 3.16: 311 Voltage vectors generated by an 11 level inverter [33]

Figure 3.16 shows the total number of 311 different space vectors generated by an 11-level inverter. The reference load voltage vector is also included in this figure. The main idea in SVC is to deliver to the load a voltage vector that minimizes the space error or distance to the reference vector. The high density of vectors produced by the 11-level inverter will generate only small errors in relation to the reference vector; it is, therefore, unnecessary to use a more complex modulation scheme involving the three vectors adjacent to the reference.

3.2.5. One dimensional modulation

One-dimensional modulation is another regularly sampled modulation method which, like to space-vector modulation, allows flexibility over the choice of redundant switching states [61] and [62].

One-dimensional modulation is a single-phase modulation technique that synthesizes an output voltage reference using selected switching states. This modulation method has been described extensively for two-cell converters [62], [63], and [64] has been shown to be capable of compensating for changing capacitor voltages [67] and of maintaining a specific ratio of capacitor voltages [65], [66], [64].

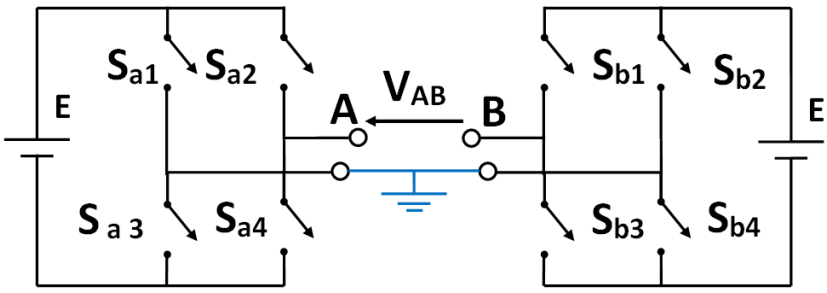


Figure 3.17: Single-phase five-level CHB.

It is to be high-lighted that if the one-dimensional modulation technique is applied on three-phased system, it must be applied individually to each phase leg.

The foundation of the one-dimensional modulation is one-dimensional control region, such as the control region for a 5-level converter shown in Figure 3.17.

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	V_A	V_B	V_{AB}
1	0	1	0	1	0	1	0	E	E	0
1	0	1	0	0	1	0	1	E	-E	2E
1	0	1	0	0	0	0	0	E	0	E
0	0	0	0	1	0	1	0	0	E	-E
0	0	0	0	0	1	0	1	0	-E	E
0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	1	0	1	0	-E	E	-2E
0	1	0	1	0	1	0	1	-E	-E	0
0	1	0	1	0	0	0	0	-E	0	-E

Table 2: Possible switching configurations for 5 level cascaded H Bridge converter.

The one dimensional control has been inspired from the space vector control, The control region of the inverter can be presented in a plan similar to (α, β), by Presenting the possible status on Table 2 in a plan.

The possible state vectors of the inverter are labeled using a couple of numbers *SA SB* denoting the state of phase A and B respectively.

SA has three possible entries,0,1 and 2, zero is the lowest voltage value state , (-E,0,+E).

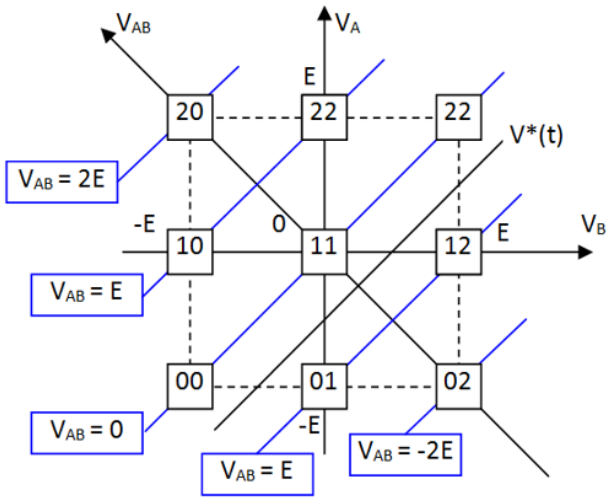


Figure 3.18: Control region of a single-phase five-level converter.

As shown on Figure 3.18 switching states of a single-phase inverter can be expressed as line vectors, the states of each bridge and the output voltage produced by each state is given on a horizontal voltage range.

At each sampling instant *t*, the voltage reference voltage is located in the control region and nearby switching states are chosen.

Figure 3.19 shows the shows the switching states on V_{AB}, $V_*(t)$ is generated by combining the adjacent position on V_{AB}.

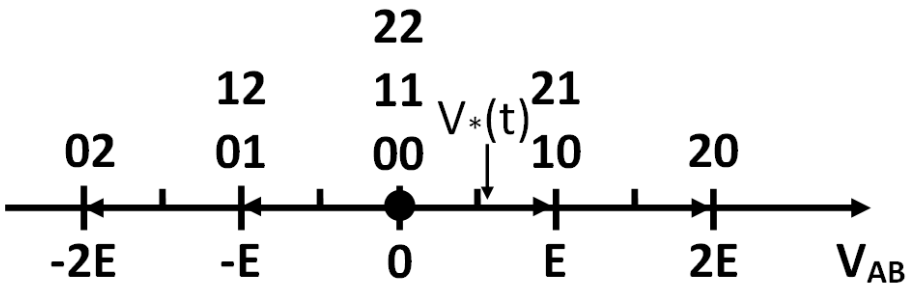


Figure 3.19: Control region for V_{AB} for a single-phase five-level converter

The chosen switching states are applied for time intervals calculated to produce the same average output as the reference during the sampling period. The selection of redundant states is left to the implementation, allowing optimization of the modulation.

The Algorithm can be implemented on Matlab, and of course will depend on the sampling frequency for one and gives also the choice to use different carrier frequencies for each range. A simple approach is shown on figure.3.20.

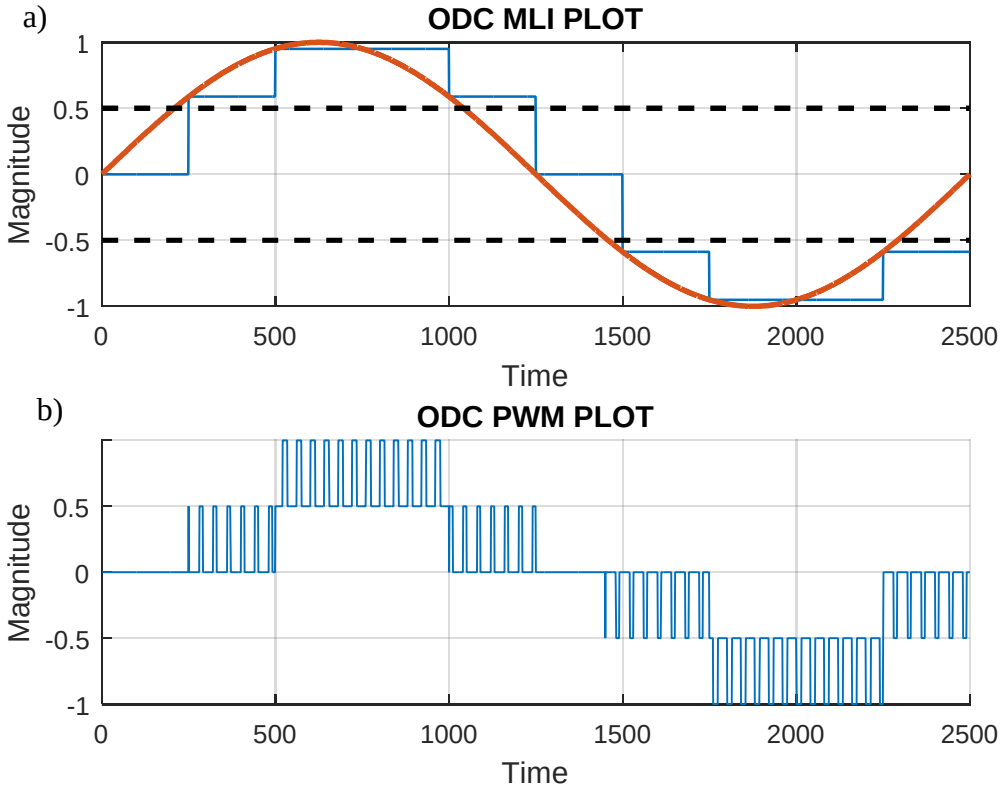


Figure 3.20: One-dimensional modulation, a) reference signal and sampling. b) Output.

3.2.6. Minimum THD PWM Method

This is mainly our contribution, the Min THD PWM Method concentrates on optimizing the usage of the existing hardware with a better efficiency, by minimizing the THD equation in (3.15), this is done through finding the best switching angles and guaranteeing the minimization of harmonics within a user defined bandwidth.

Some of the methods presented in [8], do not guaranty that the THD is at its minimum, and targeting the elimination of some harmonics like the SHE, but does not guaranty that the THD is at its minimum.

Optimization can be done through different optimization methods like the metaheuristic methods.

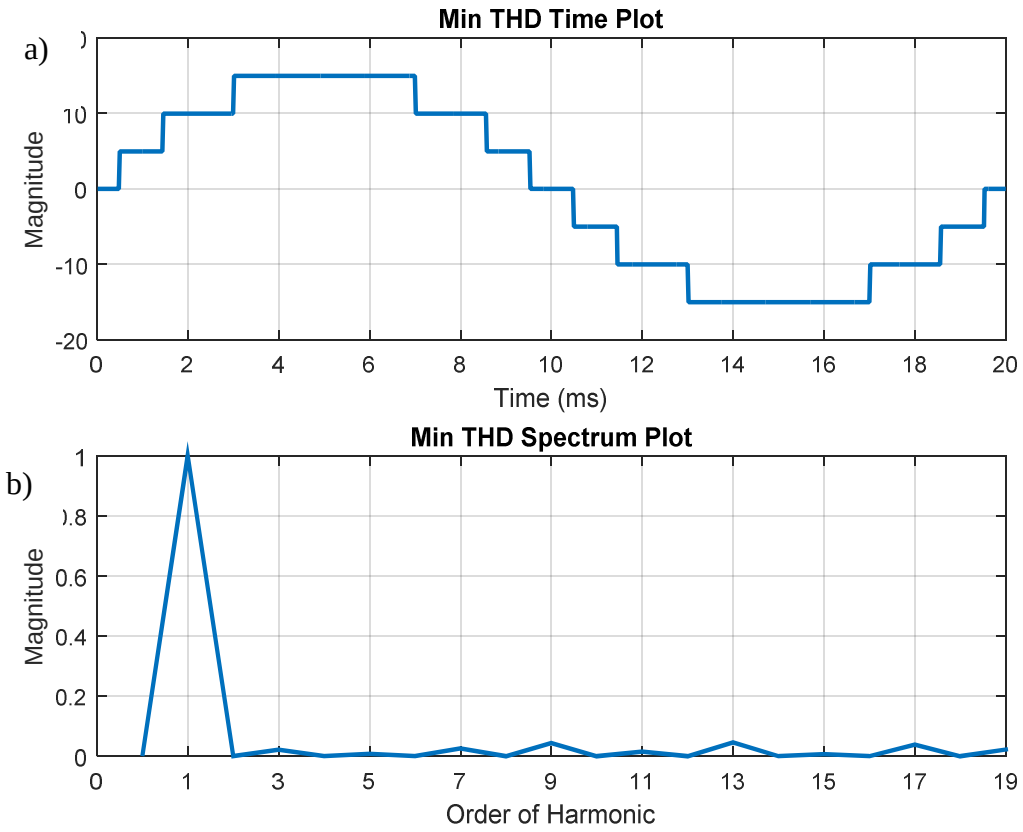


Figure 3.21: Minimum THD method, a) output, time domain, b) spectrum. THD=8%.

The Min THD is targeting the overall THD on a range of frequencies to be at the minimum possible, and not targeting specific ones to be eliminated, like the SHE.

Figure 3.21 (a), shows the signal in the time domain of a 7 levels inverts , basic staircase signal , switching angles optimized to have the minimum THD .

Figure 3.21 (b), shows the spectrum over 19 Harmonics, the reached THD is 8%, while with the SHE method on figure 3.10, the THD is 9%.

3.3. Conclusion

The main control strategies were presented on this chapter, multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, and space-vector modulation. Space Vector control and One-dimensional modulation, and the minimum THD strategy method used in [31].

The performance of the MLI does not only depend on the hardware , but also narrowly on the control strategy, we have drilled down to the early control strategies, SPWM [40], wich was published in 1975, the block functions can now be integrated in one microcontroller, the technology evolution is giving us access to simulate the inverter performance before implementation. The actual semiconductor technology is offering also a way to go to higher frequencies and higher power. We have also detailed some methods like the space vector modulation, to make this thesis a good support to our students, and provide the basics to the reader interested in the subject.

We have also introduced the minimum THD PWM Method that we have published in [31], which gives a certainty of THD reduction within the predefined bandwidth.

Chapter 4

Optimization Algorithms

4.1. Introduction

Today's world development and growth are calling for more and more resources, with the fact that most of the resources are limited, this reality has called for a new ways to manage the available resources, and optimization is one of these preferred methods. The evolution of computers has given to the optimization a wide space of interest, as many new optimization methods are being developed, such as artificial intelligence and nature –inspired metaheuristic algorithms [68].

In this chapter we will mention some of the optimization methods in general and specify the ones used to optimize the THD, the exercise of finding the switching angles in order to find the minimum THD, we will discuss some of these methods in details.

In English the word optimization is:

-The action of making the best or most effective use of a situation or resource.(Oxford)

-The act of making something as good as possible (Cambridge).

Algorithm is defined as:

-A process or set of rules to be followed in calculations or other problem-solving operations, especially by a computer (oxford).

-A set of mathematical instructions or rules that, especially if given to a computer, will help to calculate an answer to a problem. (Cambridge).

Optimization theory is a set of mathematical results and numerical methods for finding and identify the best candidate from a set of options without having to explicitly list and appraise all the possible options. [69].

Since the typical purpose of the engineer is to design more efficient, better new designs with the lowest possible cost, optimization falls at the basics of the engineering problems.

Instead of setting up expensive complicated experiments, and trying to tweak and adjust all the control parameters, which require time and resources, as well as the risks of failures and the resulting consequences during experiments, the optimization has proven to be the most effective way to save, time, money and other resources. That is where resides the brilliance of the optimization methods in determining the best case without having to test or experiment all the possible cases at the cost of running a calculator or a computer. That will require a thorough understanding of the problem and a precise mathematical modeling, during the execution of the algorithm by the calculator , the logical steps are clearly defined, and they are translated to the language that the calculating machine understands, the final solution is

obtained by running numerical iterations, a wide range of numerical methods have been developed .

4.2. Methods of reducing and optimizing THD

Referring to Chapter 3, solving the SHE or reducing the THD problem will go through optimizing the THD in equation (3.2).

$$THD(\theta_1, \theta_2, \theta_3 \dots \theta_k) = \sqrt{\frac{V_3^2+V_5^2+V_7^2+\cdots..V_n^2}{V_1^2}} \times 100 \quad (3.2)$$

In General, the existing methods used to solve the SHE problem can be categorized in three types, numerical methods, algebraic methods and intelligent methods [70].
This is summarized on figure 4.1.

4.2.1. Numerical methods

Numerical methods are characterized by being high efficiency iteration algorithms, but also very depending on the initial values.[70]. Most of numerical methods can converge very fast if the initial values are chosen correctly . [71]. These methods are extremely tied to the initial values, and can get stack at local minimum solution if the proper initial values are not selected.
Within the numerical methods we cite Newton Raphson, Gradient optimization Walsh function...etc
Some other good examples and referenced are mentioned below, in case of deep researches on the subject they can be for good guidance.
[72] has also showed the superiority of the programmed PWM techniques over the conventional carrier modulated PWM's.
[73] used Newton method, and has suggested a predictive method for the initial values.
[74] also used Newton method but has solved the initial values problem by finding them through PSO algorithm.
[75]has presented another way of generating the initial values , through GA and PSO, and proposed a Hybrid (GA, PSO)-Newton Raphson method.
[76] has also used Newton Raphson method, but has overcome the main initial values problem through the GA algorithm.
In [77] improved Newton Raphson algorithm is proposed, to eliminate some frequencies.
[78] has also proposed a solution for the initial values for the Newton Raphson method.

4.2.2. Algebraic methods

In this case, the resulting nonlinear transcendental equations are converted into polynomial equations. By resolving these equations the optimized firing angles are obtained.

The major benefit of this method is that it is not dependent on the initial values and will not need any guess. On the other hand they tend to be very complex and not efficient when the number of levels increases and is more than 4 [70].

Within the Algebraic methods we cite the Resultant theory was used to solve the Selective Harmonic problem and find the best angles and minimize the THD [45] [79].Wu method was presented in [80], Groebner bases theory [70], symmetric polynomial theory [81], and power sum [82].

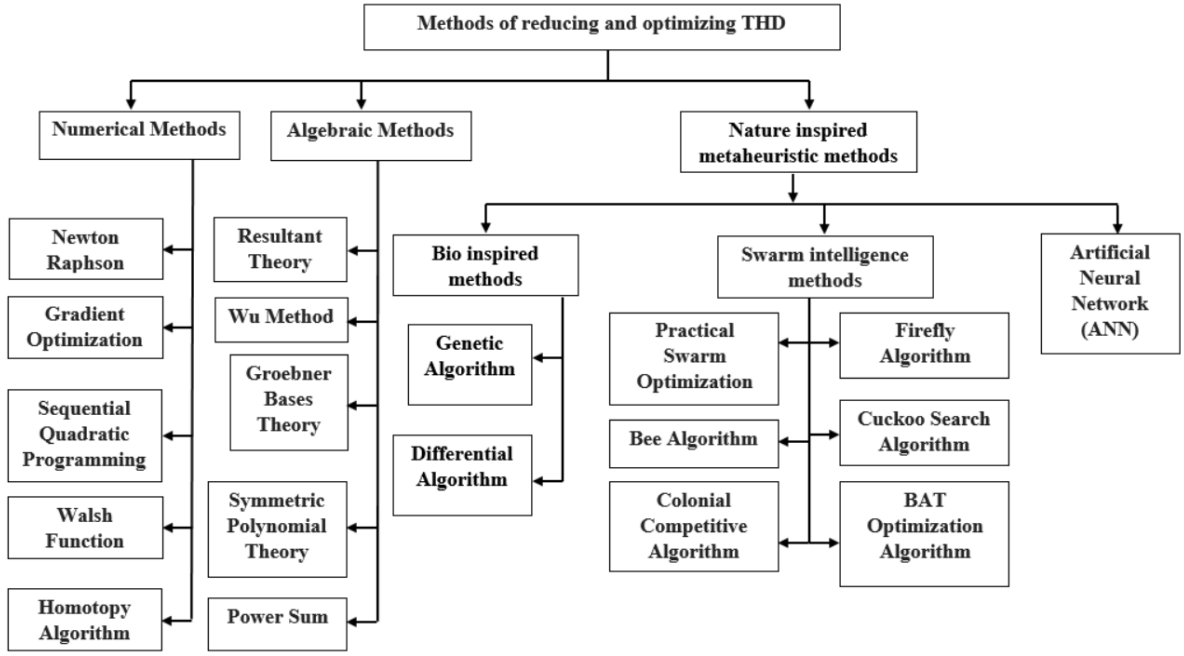


Figure 4.1: Methods of reducing and optimizing the THD [71].

4.2.3. Nature inspired metaheuristic methods

These nature-inspired metaheuristic algorithms can be categorized into two classes, Swarm intelligence and bio-inspired algorithms. They can be called can be called swarm-intelligence-based, bio-inspired or more specific to the source of inspiration, bee, ant , bat… We will be presenting just the ones which have showed interests of resolving the THD optimization problematic.

Recently, Nature-inspired algorithms are among the most powerful algorithms for optimization, and becoming among the preferred tools to resolve the optimization problems in particular the NP-hard problems [83].

4.2.3.1. Bio inspired methods

Biology-derived algorithms are an essential part of computational sciences, which are important to many scientific disciplines and engineering applications. These methods are originating from or based on the similarity to natural evolution and biological activities, and these biologically inspired computations include genetic algorithms, cellular automata, and other algorithms.

Many biology-inspired algorithms are popular in evolutionary computations. For engineering applications in particular, four types of algorithms are very useful and hence relevant. They are GAs, photosynthetic algorithms (PAs), neural networks, and cellular automata [87]. We will limit to the two methods referenced to solve the THD problem.

4.2.3.1.1. Genetic Algorithm (GA)

Genetic Algorithms (GAs) begun with biologists in the 1940 who were mainly interested in Natural selection , GAs are adaptive heuristic search technique. They were invented by John Holland in the 1960s and were developed by Holland and his students and colleagues at the University of Michigan in the 1960s and the 1970s [84].

Contrarily to the evolution strategies and evolutionary programming, Holland's original aim was to study the phenomena of adaptation as it takes place in the nature, and develop ways to implement it on a computer system, and explore some of the biological applications.

Holland's Book Adaptation in Natural and Artificial Systems [85] , has presented a set up of mathematical framework which makes it possible to extract and generalize critical factors of the biological processes [71][85-86].

GA is a method where we move from one population to another by applying "natural selection" or "survival of the fittest " criteria, with genetic inspired operators such as crossover , mutation and inversion.

A generation is one iteration, where a new population is created, through the genetic operators.

The main operator is the crossover of two parents, which has the highest probability (0.6 to 1.0) .the crossover, is achieved by switching segment of one string with the corresponding

segment on another string at a random position. Figure 4.2. shows a single point crossover. [87]

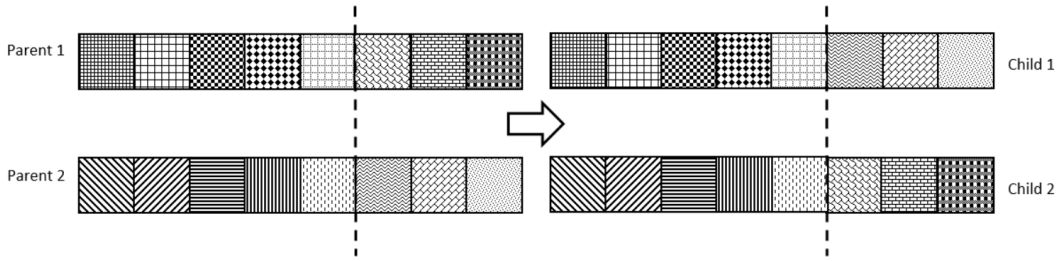


Figure 4.2: Crossover.

Mutation process is done by replacing the gen at random position with a new value. For simplicity the example below on figure 4.3 is showing the mutation in binary string.
The mutation operation is carried out by the flopping of randomly selected bits, with a smaller probability, (0.001 to 0.05). [87]

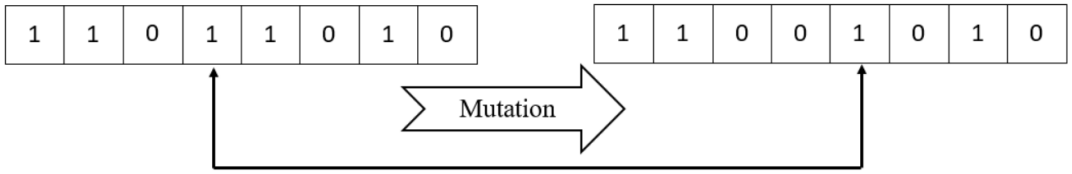


Figure 4.3: Mutation.

```
Genetic Algorithm
     1.    Objective(Cost) function f(x)
     2.    Initial parameters CR,MR and population size
     3.    Generate an initial population of chromosomes
     4.    Evaluate the fitness of each chromosome
     5.    while (t< Max Generation) or (stop criteria)
     6.          Select the best parents for reproduction
     7.          Create offspring through crossover operation between
                 selected parents with probability CR
     8.          Mutate some chromosomes with probability MR
     9.          Evaluate the fitness of the new chromosomes
     10.         Find the best chromosome
     11.   end While
```

Figure 4.4: Pseudo code of the GA [71].

Population is a collection of chromosomes. Each chromosome consists of gens. Each gene is being an instance of a particular "allele". The selection process is the one defining which

chromosome will be allowed to reproduce, the fitter chromosomes will produce more offspring than the less fit ones.

The same idea has been implemented on PCs and now famous and is a frequently used tool available on Matlab toolbox.

The pseudo cod of the GA is given on figure 4.4. [71]. In [50] and [76] the GA has been used to solve the THD problem.

4.2.3.1.2. Differential Evolution (DE) algorithm

Differential Evolution algorithm (DE) was presented the first time in 1997 by Storn and Price [88] (see Figure 4.5). It is a population based algorithm, stochastic direct search method designed for, and has the Ability to handle non-differentiable, nonlinear and multimodal cost functions. The evolution of the solution goes through the strategy below:

a. Mutation

For each target vector $x_{i,G}$, $i = 1,2,3 \ldots., NP$, a mutant vector is generated according to:

$$u_{i,G+1} = x_{r_1,G} + F \times (x_{r_2,G} - x_{r_3,G}) \tag{4.1}$$

With random indexes, r_1, r_2 ,r_3 $\in$\{1,2....,NP\}, integers, mutually different and F>0.

r_1, r_2 and r_3 are randomly chosen different from the running index, therefore NP must be greater than 3.

F is a real and constant factor $\in$ [0, 2], which controls the amplification of the differential variation $(x_{r_2,G} - x_{r_3,G})$.

b. Crossover

In order to increase the diversity of the perturbed parameter vectors, crossover is introduced. To this end, the trial vector is:

$$u_{i,G+1} = (u_{1i,G+1}, u_{2i,G+1}, \ldots. u_{Di,G+1}) \tag{4.2}$$

$$u_{ji,G+1} = \begin{cases} v_{ji,G+1} & if\ (randb(j) \le CR) or\ j = rnbr(i) \\ x_{ji,G} & if\ (randb(j) > CR) \ne rnbr(i) \end{cases} \tag{4.3}$$

$j = 1,2,3, \ldots \ldots D$

randb (j) is the j^{th} evaluation of a uniform random number generator with outcome $\in$ [0; 1]. CR is the crossover constant $\in$ [4.0; 1] which has to be determined by the user. *rnbr(i)* is a randomly chosen index $\in$ 1; 2; :::;D which ensures that $u_{i,G+1}$ gets at least

one parameter from $u_{i;G+1}$. Figure 2 gives an example of the crossover mechanism for 7-dimensional vectors.

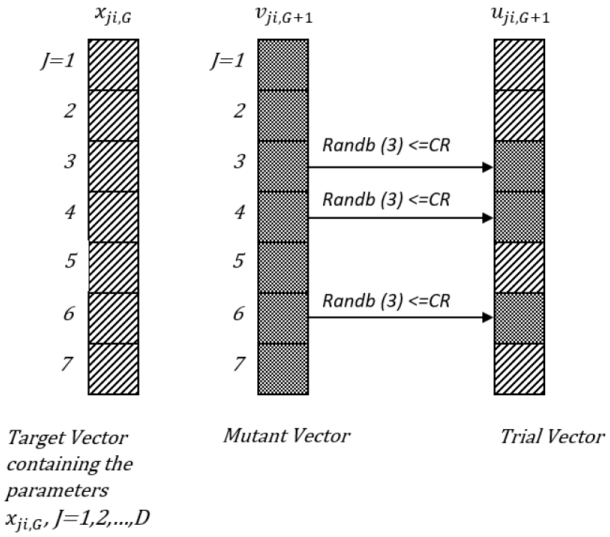


Figure 4.5: illustration of the crossover process for D = 7 parameters [88].

c. Selection

To decide whether or not it should become a member of generation *G+1*, the trial vector $u_{i,G+1}$ is compared to the target vector $x_{i,G}$ using the greedy criterion. If vector $u_{i;G+1}$ yields a smaller cost function value than $x_{i;G}$, then $x_{i;G+1}$ is set to $u_{i,G+1}$; otherwise, the old value $x_{i,G}$ is retained.

The pseudocode of the differential evaluation algorithm is given on figure 4.6.

In [89][90][91][92][93] the DE algorithm has been used to solve the THD problem.

```
Differential Evolution Algorithm
1.  Objective function f(x)
2.  Initial parameters CR, F, and population size nPop.
3.  Generate an initial population of agents.
4.  Evaluate the fitness of each agent.
5.  while (t< Max Generation) or (stop criteria)
6.       for i=1:nPop
7.          Randomly select three agents, A, B and C, from the
            population and generate noisy vector Y.
8.          Create offspring vector Z via crossover operation
            between target vector xi and noisy vector Y.
9.          Create trail vector T using vector Z or target vector
            xi based on probability of CR.
10.         Evaluate the fitness of the trial vector.
11.         If f(T) < f(xi),
12.           Replace agent xi with trial vector T.
13.         End if
14.      End for i
15.      Find the best agent.
16.      end While
```

Figure 4.6: Pseudo code of the Differential Evolution algorithm [71].

4.2.3.2. Swarm intelligence methods

The swarm intelligence is another nature-inspired discipline, watching the social behavior of different insects or animals, foraging or reproducing. Many species have survived despite the harsh environment around. These behaviors have been translated to strong methods and contributed in the resolution of the most complicated problems.

Bonabeau, has defined the swarm intelligence as “any attempt to design algorithms or distributed problem-solving devices inspired by the collective behavior of social insect colonies and other animal societies” [95]

Below we are limiting to the methods used and referenced or contributed the to resolve THD problem.

4.2.3.2.1. Practical Swarm Optimization algorithm (PSO)

PSO (practical swarm optimization), was developed in 1995 by Kennedy and Eberhart [94] , The authors of this paper are a social psychologist and an electrical engineer , that was based on The behavior of bird and fish teaching in nature , which is known as swarm intelligence.

PSO consists of a swarm or group of particles moving in a search space of possible solutions for a problem. Each particle has a position vector representing a candidate solution to the problem and a velocity vector and also contains a small memory that stores its own best

position seen so far and a global best position obtained through communication with its neighbor particles [95].

The fitness of each particle is evaluated through an objective function.

The movement or the velocity of a particle is influenced by three major parameters [95] [49]:

- The momentum, inertia or habit.
- Attractiveness towards the best position ever found, best self experience.
- Attraction towards the best position found by any particle, Global best particle, social knowledge.

The velocity expression can be written as follows:

$$V_{ij}^{t+1}=V_{ij}^{t} \times w^{t} + C_1 e_{1j} \times \left(g_{ij} - x_{ij}^{t}\right) + C_2 e_{2j} \times \left(p_{ij} - x_{ij}^{t}\right) \quad (4.4)$$

$$x_{ij}^{t+1}=x_{ij}^{t} + V_{ij}^{t+1} \quad (4.5)$$

W is the inertia function,

where i is the particle index, j is the index of parameter of concern to be optimized, x is the position of the i^{th} particle and j^{th} parameter, t is the discrete time index, v is the velocity of the i^{th} particle and j^{th} parameter, P is the best position found by the i^{th} particle and j^{th} parameter (personal best), G is the best position found by swarm (global best), e is a random uniform number between [0,1] applied to the i^{th} particle, C1 and C2 are the learning parameters or acceleration constants, are selected between [0,2] the pseudo code of the PSO is also given on figure 4.7.

```
Particle Swarm Optimization
1.  Objective function f(x)
2.  Initial parameters C1, C2, Wmax, Wmin, and population size nPop.
3.  Generate an initial population of particles.
4.  Evaluate the fitness of each particle and set all initial
    positions as P_Best_xi.
5.  while (t< Max Generation) or (stop criteria)
6.        Select the G_Best particle in the swarm, which has the
          minimum fitness value.
7.        for i=1:nPop
8.             Calculate the velocity of particle xi.
9.             Update the position of particle xi.
10.       end for i
11.       for i=1:nPop
12.            Evaluate the fitness of updated particle xi.
13.            If f(xi)<f(P_Best_xi),
14.            Set current position as P_Best_xi.
15.            end if
16.       end for i
17.       Find the best particle.
18. end While
```

Figure 4.7: Pseudo code of practical swarm optimization algorithm.

Figure 4.8 shows the concept of particle movement influenced by the three terms.

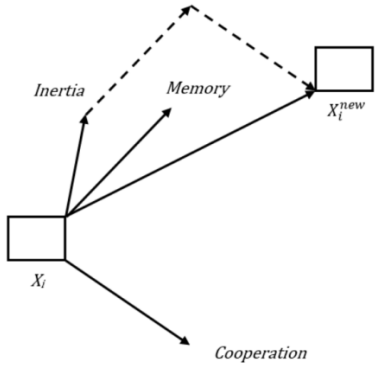


Figure 4.8: Illustration of a particle movement influenced by three terms.

For the application in reducing the THD, many articles have proposed solutions for the HE problem through the PSO. For more details, please refer to [49], [75] and [104-106].

4.2.3.2.2. Bee Algorithm (BA)

The Bee algorithm is one of the Swarm algorithms developed by Karaboga and Yang in 2005[96], inspired from the work previously done by Bonabeau [71][95-97].

This algorithm is principally inspired by the foraging behavior of honey bees, and simulating their strategy in finding the food sources, and used to look for the best solution to an optimization problem.

As presented by the original author, the colony of artificial bees consists of three groups of bees: employed bees, onlookers and scouts. [98-100].

The solution to the optimum goes through three phases:

a. The Search Phase of Employed Bees.

It is to be considered that the number of employed bees is equal to the number of the food sources.

The employed bee brings some nectar back to the hive , it communicates the information to the onlookers and hires more , this communication is done through Wangle Dance , this seem too communicate the direction and the distance .

The virtual bee evaluates the food source through the objective function, in each iteration the employed bees search for new food sources v_{ij} in the neighborhood of x_{ij} through equation (4.7), and memorize the best ones through a greedy selection if a better nectar is found.

$$v_{ij} = x_{ij} + \varphi_{ij}(x_{ij} - x_{kj}) \tag{4.6}$$

Where $j \in \{1, 2, \ldots, D\}$ and $\mathrm{k} \in \{1, 2, \ldots, \mathrm{Npop}\}$, Npop is the initial population, are randomly chosen indexes. Although k is determined randomly, it has to be different from i. φ_{ij} is a random number in the range [−1, 1].

Equation (4.7) denotes that, within the neighborhood of every food source site represented by x_i, a food source v_i is determined by changing one parameter of x_i.

b. The Selection Phase of Onlooker Bees

In this phase, each onlooker bee selects one of the food sources depending on the

fitness value obtained from the employed bees. The best food sources will attract more onlookers, The fitness based probability selection, scheme may be a roulette wheel, ranking based, stochastic universal sampling, tournament, the roulette wheel was used in the original BA.

Onlookers will go to the food sources and will improve them through equation (4.7), in the same way of the employed bees.

c. Scout Bee Phase:

After the previous phases are finished , the BA checks if there is any depleted sources to be abandoned, if a solution cannot be enhanced through a number of cycles , the

source is to be considered as depleted . The scout will randomly move and can find new rich sources. This cycle is repeated until the termination criteria is satisfied.

The pseudo code of the BA is shown of figure 4.9.

```
Bee Algorithm
1.  Objective function f(x)
2.  Initial parameters L and population size nPop.
3.  Generate an initial population of food sources.
4.  Evaluate the fitness of each food source.
5.  while (t< Max Generation) or (stop criteria)
6.       for i=1:nPop     %employed bee phase
7.            Generate new solution v_{i,j} in the neighborhood of x_{i,j}
8.            If f(v_{i,j})<f(x_{i,j}),
9.                 Replace x_{i,j} with the new food source v_{i,j} .
10.           end if
11.      end for i
12.      Select the best food sources using the roulette wheel
         method.
13.      for i=1:nPop    %onlooker bee phase
14.           Generate new solution v_i from solution x_i.
15.           if f(v_i)<f(x_i),
16.                Replace x_i with the new food source v_i.
17.           end if
18.      end for i
19.      if any food source does not improve  %scout bee phase
         for an L number of trials, then change it with new food
         source.
20.      Save the best food source
21.  end While
```

Figure 4.9 Pseudo code of Bee optimization algorithm [71].

The bee algorithm has been used the first time to eliminate the unwanted harmonics from 7-level MLI in [97].

4.2.3.2.3. Imperial Competitive Algorithm (ICA)

ICA was introduced the first time by Esmail &Caro in 2007 [101]. This algorithm is inspired by imperialistic competition. Population individuals called country, empires are formed from colonies and imperialists. The ICA is based on imperialistic competition among these empires , during this competition. Powerful empires will confiscate over colonies from the weaker empires, till the weakest empires will eventually collapse, and we end up with only one empire.

a. Initialization

The country dimension is the number of Variables to be optimized, N_{var}.

$$country = [p_1, p_2, \ldots., p_{N_{var}}] \quad (4.7)$$

The countries are ranked as per their power, the power of country is inversely proportional to its fitness. If N_{pop} is the initial population of the countries,N_{imp} is number of imperial countries, N_{col} is the number of colonies, we can write:

$$N_{pop} = N_{imp} + N_{col} \quad (4.8)$$

The colonies are divided between the imperial countries depending on their power.

C_n is the normalized cost of an imperialist.

$$C_n = c_n - max(c_i) \quad (4.9)$$

Normalized power of each colony is

$$p_n = \left| \frac{C_n}{\sum_{i=1}^{N_{imp}} C_i} \right| \quad (4.10)$$

The initial number of colonies of each empire will be

$$N.C_n = round\ \{p_n.N_{col}\} \quad (4.11)$$

b. Moving the colonies of an empire toward the imperialist

$$x_{new} = x_{old} + \beta \times rand \times [x_{imp} - x_{old}] \quad (4.12)$$

Where β is the constant number that must be selected greater than 1, and rand is the uniformly distributed random number generated between [0, 1].

c. Exchanging position between the imperialist and a colony

while moving toward the imperialist , the colony may find a position with less cost , and become more powerful than the imperialist , in this case an exchange of roles is executed, Algorithm will continue , colonies start moving towards the new imperialist.

d. Total power of the empire

The total power of an empire is mainly affected by the power of the imperialist country, and the colonies through the expression below:

$$T.C_n = cost(imperialist_n) + \xi\ mean\{cost\ (colonies\ of\ empire\ _n)\} \quad (4.13)$$

$T.C_n$ is the total cost of the *n*th empire, ξ is the positive number that must be less than 1, and $colonies\ of\ empire\ _n$ denotes the colonies of empire *n*.

To ensure the fair competition, the normalized total cost of each empire is calculated using equation (4.14).

$$N.T.C_n = T.C_n - max\{T.C_i\} \quad (4.14)$$

Where $T.C_n$ is the total cost of *n*th empire.

e. Imperialistic competition

The possession probability of empire *n* is defined as:

$$P_{P_n} = \left| \frac{N.T.C_n}{\sum_{i=1}^{N_{imp}} N.T.C_i} \right| \tag{4.15}$$

to hand over the weak colony , the possession probabilty of each empire is arranged in vector P:

$$P = \left[P_{P_1}, P_{P_2}, P_{P_3}, \ldots . P_{P_{N_{imp}}} \right] \tag{4.16}$$

Another vector *R* with the same size of *P* is created , contains uniformly distributed random numbers between [0, 1].

$$R = \left[r_1, r_2, r_3, \ldots r_{N_{imp}} \right] \tag{4.17}$$

Than another vector *D* is created by substracting *R* from *P* ,

$$D = P - R \tag{4.18}$$

The weak colony is handed to the empire with the index of the highest value in D.

f. Eliminating the powerless Empires

Powerless empires will collapse, and its colonies will be divided amog the other ones. Different criteria can be chosen to consider an empire as powerless. The first authors have considered an empire collapsed and eliminate it when it loses all of its colonies.

g. Convergence

The competiton continues in each itteration, after a while all the empires expect the most powerfull one will collapse and the powerfull empire will extend its pwer under all the colonies, in this ideal world end The imperialist of a powerful empire and its colonies hold the same value of the objective function that means, there is no any difference between them. The program will be terminated when all the empires, except the most powerful one, have collapsed, and all the colonies have been captured by the most powerful empire, or if the iterations reached to the maximum number.

The pseudo code of the ICA is given on figure 4.10.

ICA has been used in [102] and [103] to solve the problem of Selective Harmonic Elimination. On figure is the pseudocode of the Imperial Competitive Algorithm

```
Imperialist Colony Algorithm
1.  Objective function f(x)
2.  Initial parameters, β, ε, and population size nPop.
3.  Generate an initial population of countries.
4.  Evaluate the fitness of each country.
5.  Create n empires and assign one imperialist imp_n to each
    empire based on the minimum fitness value.
6.  Assign the remaining countries N_col as colonies to the empires.
    The empire with the maximum power P_n holds the maximum number
    of colonies N.C_n
7.  while (t< Max Generation) or (stop criteria)
8.        for i=1:n
9.            Move colonies_i of empire I toward their imperialist
              imp_i.
10.       end for i.
11.       for i=1:n
12.           Evaluate the fitness of each colony_i in empire i.
13.           if f(colony_i)< f(imp_i),
14.                 Exchange their positions.
15.           end if
16.       end for i
17.       if n>1
18.           Compute the total cost T.C_n of empires.
19.            Pick the weakest colony from the weakest empire and
               give it to the empire that has the most likelihood
               to possess it.
20.           for i=1:n
21.                if number of colonies_i in empire i=0,
22.                     Eliminate empire i
23.                     n=n-1
24.                end if
25.           end for i
26.       end if
27.       save the best Imperialist
28.  end While
```

Figure 4.10: Pseudo code of Imperial colony algorithm [71].

4.2.3.2.4. Cuckoo Search Algorithm (CS)

Cuckoo search (CS) is one of the latest nature-inspired metaheuristic algorithms, developed in 2009 by Xin-She Yang and Suash Deb.

CS is based on the brood parasitism of some cuckoo species. In addition, this algorithm is enhanced by the so-called Lévy flights [68], rather than by simple isotropic random walks. Cukoos are very known for their aggressive reproduction strategy. Some species lay their eggs in communal nests, though they may remove others' eggs to increase the hatching probability of their own eggs. Quite a number of species engage the obligate brood parasitism by laying their eggs in the nests of other host birds (often other species).

For simplicity the three idealized rules are set by the authors:

- Each cuckoo lays one egg at a time, and dumps it in a randomly chosen nest.
- The best nests with high-quality eggs will be carried over to the next generations.
- The number of available host nests is fixed, and the egg laid by a cuckoo is discovered by the host bird with a probability pa ϵ [0, 1]. In this case, the host bird can either get rid of the egg, or simply abandon the nest and build a completely new nest.

Authors have chosen to use the following simple representations that each egg in a nest represents a solution, and each cuckoo can lay only one egg (thus representing one solution), the aim is to use the new and potentially better solutions (cuckoos) to replace a not-so-good solution in the nests.

In this case, there is no distinction between an egg, a nest or a cuckoo, as each nest corresponds to one egg which also represents one cuckoo.

The cuckoo egg is generated using Eq. (4.19). After obtaining the cuckoo egg, its fitness is compared with that of a randomly selected egg from the nest. If the fitness of the cuckoo egg is better than that of the selected egg, then the cuckoo solution is replaced with the host nest solution. At the end of each iteration, fraction pa of the worst nest is abandoned and new solutions are generated.

$$x_i^{t+1} = x_i^t + \alpha . L\grave{e}vy(\lambda) \tag{4.19}$$

Where α is the step size, and its value is dependent on the scales of an interested problem. The term Levy indicated lèvy flight, which is responsible for random walks. Lèvy flight played an important role in the exploration of a search space and it is calculated using equation (4.20).

$$L\grave{e}vy(\lambda) \sim u = t^{-\lambda}, (1 < \lambda < 3) \tag{4.20}$$

The pseudo algorithm of the CSA is shown in figure.4.11

```
Cuckoo Search algorithm
1.  Objective function f(x)
2.  Initial parameter p_a and population size nPop.
3.  Generate an initial population of host nests.
4.  Evaluate the fitness of all host nests.
5.  while (t< Max Generation) or (stop criteria)
6.        Randomly select a Cuckoo/generate a solution via Lèvy
          flights.
7.        Evaluate its fitness F_i.
8.        Randomly select a nest, x_j.
9.        if (F_i < F_xj),
10.            Replace x_j with the new solution.
11.       end if
12.       A fraction (p_a) of worse nests are abandoned and new
          solutions are generated.
13.       Keep best solutions.
14.       Rank the solutions and find the current best.
15. end While
```

Figure 4.11: Pseudo code of Cuckoo Search algorithm [71].

The CS algorithm has been used for the THD problem in [107] and in [108], to find the optimum switch angles to eliminate the lower order harmonics.

4.2.3.2.5. Bat Optimization Algorithm (BOA)

The BAT optimization Algorithm was developed by Yang [109][110] in 2010. It is mainly inspired from echolocation behavior of the bats.

Bats use a type of sonar, also known as, echolocation, to detect prey, avoid obstacles, and locate their roosting crevices in the dark. These bats emit a very loud sound pulse and listen for the echo that returns back from the surrounding objects.

Studies showed that bats use the time delay from the emission and detection of the echo, the time difference between their two ears, and the loudness variations of the echoes to build up three dimensional scenario of the area where they are, that is building an acoustic image of the scene, based on the travel time of the wave, they can detect the distance and orientation of the target, the type of prey, and even the moving speed of the prey such as small insects. This is just giving how fast is the processing of the acoustic data acquired by the bat.

As described by the Xin-She Yang the following approximate or idealized rules were used.

1. All bats use echolocation to sense distance, and they also ‘know’ the difference between food/prey and background barriers in some magical way.

2. Bats fly randomly with velocity v_i at position xi with a frequency f_{min}, varying wavelength and loudness A_0 to search for prey. They can automatically adjust the wavelength (or frequency) of their emitted pulses and adjust the rate of pulse emission r $\in$ [0, 1], depending on the proximity of their target.

3. Although the loudness can vary in many ways, we assume that the loudness varies from a large (positive) A_0 to a minimum constant value A_{min}.

```
BAT Optimization Algorithm
1. Objective functions f(x).
2. Initialize parameters, fi at xi, ri, Ai, and population
   size nPop
3. Generate an initial population of bats.
4. while (t <Max number of iterations)
5.      Generate new solutions by adjusting the frequency and
        updating velocities and locations.
6.       if (rand > ri)
7.       Then select a solution among the best solutions.
8.       Generate a local solution around the selected best
         solution
9.       end if
10.     Generate a new solution by flying randomly.
11.     if (rand < Ai & f(xi) < f(x*))
12.     Accept the new solutions.
13.     and increase ri & reduce Ai
14.     end if
15.Rank the bats and find the current best x*
16.end while
17.Record x* as a non-dominated solution
18.end
19.Postprocess results and visualization
```

Figure 4.12: Pseudo code of the bat optimization algorithm [71].

For each bat, the position and velocity are obtained through equations (4.21) and (4.22),

$$x_i^{t+1} = x_i^t + v_i^t \tag{4.21}$$

$$v_i^{t+1} = v_i^t + (x_i^t - x_*)f_i \tag{4.22}$$

Where f_i is a fixed frequency calculated as per equation (4.22) , and x_* is the current global best location.

$$f_i = f_{min} + (f_{max} - f_{min})\beta \tag{4.23}$$

$\beta \in [0, 1]$ is a random vector drawn from a uniform distribution.

fmin and *fmax* are the minimum and maximum frequency ranges, respectively. The term *fi* controlled the range and pace of bat movement. The pseudo code of the BAT algorithm is shown on figure.4.12.

The bat algorithm has been used in [111] in order to solve the THD problem.

4.2.3.2.6. Firefly Algorithm (FFA)

In the late of 2007 and early 2008, Xin-She Yang has developed a new Firefly Algorithm (FA), which is one of the metaheuristic algorithms, and is based on social behavior, interaction and communication between fireflies .Fireflies generate bioluminescence flashes to communicate with mates or to attract prey.

Different studies demonstrated that PSO algorithms can do better than genetic algorithms, this is somewhat due to that fact that the broadcasting ability of the current best estimates gives better and faster convergence towards the optimality, While the new firefly algorithm is superior to both PSO and GA in terms of both efficiency and success rate.[83]

Yang discussed FA parameter tuning, compared and contrasted it with particle swarm optimization (PSO) and genetic algorithms (GA), and used 10 benchmark problems to demonstrate that FA can be superior to these alternative methods. Yang showed that FA converged to the global minimum in 99% of his simulations, 11% more often than GA and 6% more often than PSO, while requiring only 19% of GA's function evaluations and 40% of PSO's. [83]

As previously introduced, Fireflies generate bioluminescence flashes to communicate with mates or to attract prey.

Three rules below are defining the firefly algorithm [68]:

Fireflies are unisex so that one firefly will be attracted to other fireflies regardless of their sex.

The attractiveness is proportional to the brightness, and they both decrease as their distance increases. Thus for any two flashing fireflies, the less brighter one will move towards the brighter one. If there is no brighter one than a particular firefly, it will move randomly.

The brightness of a firefly is determined by the landscape of the objective function.

Fireflies' attractiveness is proportional to the light intensity seen by adjacent fireflies. We can now define the variation of fireflies attractiveness β with the distance *r* by:

$$\beta = \beta_0 e^{-\gamma r^2} \tag{4.24}$$

Where β_0 is the attractiveness at $r = 0$.

Considering fireflies $\mathbf{X}_i$ and $\mathbf{X}_j$, r_{ij} is *the* distance between firefly $\mathbf{X}_i$ and $\mathbf{X}_j$.

$$r_{ij} = \left\| \boldsymbol{X}_i - \boldsymbol{X}_j \right\| \tag{4.25}$$

The attractiveness will be expressed as per equation (13):

$$\beta = \beta_0 e^{-\gamma r_{ij}^2} \tag{4.26}$$

The firefly *i* is attracted to another more attractive (brighter) firefly *j* according to movement equation:

$$\boldsymbol{X}_i^{t+1} = \boldsymbol{X}_i^t + \beta_0 e^{-\gamma r_{ij}^2} \left(\boldsymbol{X}_j^t - \boldsymbol{X}_i^t \right) + \alpha_t \varepsilon_i^t \tag{4.27}$$

The second term is due to the attraction. The third term is randomization with α_t the randomization parameter, and $\boldsymbol{\varepsilon}_i^t$ is a vector of random numbers drawn from a Gaussian distribution or uniform distribution at time *t*. [68].

The FFA has been developed and executed through MATLAB, the pseudo code of the FFA is given in Figure 4.13.

```
Firefly Algorithm
Objective(Cost) function
f(x), x = (x1, ..., xd)^T
Generate initial population of fireflies xi (i = 1, 2, ..., n)
Light intensity Ii at xi is evaluated as f(xi)
Define light absorption coefficient γ
while (t <MaxGeneration)
for i = 1 : n all n fireflies
for j = 1 : i all n fireflies
if (Ii > Ij) /*in the case of maximization Ii < Ij  */
 Move firefly i towards j in d-dimension;
end if
Attractiveness varies according to the distance r via exp[-γr]
Evaluate new solutions and update light intensity
end for j
end for i
Rank the fireflies and find the current best
end while

  Postprocess results and visualization
```

Figure 4.13: Pseudo code of the firefly algorithm (FA)[83].

The work done in [112] has used more complex hardware structure, cascaded H-Bridges, and has used the FFA not to optimize directly the THD, but to resolve the nonlinear transcendental equations. A similar approach has been also used in [113],[114], in our case

we have used the THD ($\theta_1, \theta_2, \ldots, \theta_K$) as the light intensity *I*, the best solution will check $F(\mathbf{X}_{best}) = THD(\theta_1^*, \theta_2^*, ..., \theta_k^*)$ which is the lowest THD.

The optimization of the THD will guarantee the minimization of the harmonics within the selected bandwidth in our case 60 Harmonics, 3kHz (assuming the fundamental is 50 Hz), while in [112], the author is targeting the minimization of the first 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic are reduced to minimum, this will not be efficient for the higher Harmonics.

The firefly algorithm has been used to resolve the THD problem by M Belkacem, R Benzid and N Bouguechal in [31], [71], this is what we will develop later in the simulation part.

4.2.3.3. Artificial Neural Network (ANN)

The Human brain is unique and extremely complex, the discovery of actual processing in the human brain (consisting of 10^{11} neurons, participating in perhaps 10^{15} interconnections over transmission paths). An average of 10,000 connections / neuron, making functional model to simulate the brain function in the near future is not likely to happen soon. [115]

The Artificial Neural networks (ANN) is inspired from the nature, imitating the human nervous system neurons. [95], [116].

The mathematical model of the neutron was introduced the first time by McCulloch and Pitts in 1943

McCulloch and Pitts were the first to introduce a mathematical model of a neuron in 1943, the work was developed further and announced the principle of the perceptrons in 1947. [117],[118].

Based on the previous work, in 1958, Rosenblatt has modeled the visual perception phenomena in 1960, and in 1962 proved a theorem about perceptron learning. on [119] in 1969 Minsky has proven that single layer perceptrons has restrictions on learning , this one has slowed down the ANN researches till 1977, new connection models were introduced and that has widely open again the pathways of the ANN, like associative memories [120],[121], multi-layer perceptron (MLP) and back propagation learning algorithm [122],[123]; adaptive resonance theory (ART) [124][125].

The four elements of ANN are type of Neurons, type of connections, learning algorithm and training algorithm.

An Artificial Neural Network consists of processing elements (called neurons), and connections between them with coefficients (weights) bound to the connections.

These connections constitute the neuronal structure and attached to this structure are training and recall algorithms [115]

The following are the parameters that describe a neuron based on figure 4.12.

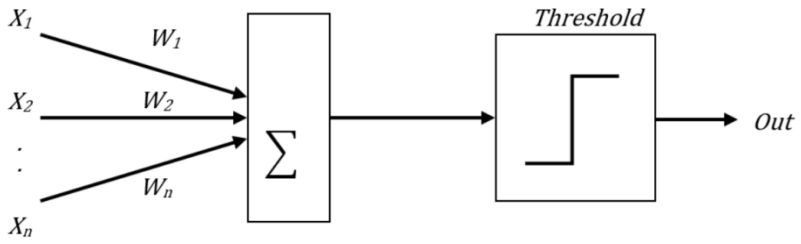


Figure 4.14: Perceptron neuron of Pitts and McCulloch.

1. Input connections (inputs): x_1, x_2, …, x_n. There are weights bound to the input connections: w_1, w_2… w_n. One input to the neuron, called the bias has a constant value of 1 and is usually represented as a separate input, let's refer to as x0, but for simplicity it is treated here just as an input, clamped to a constant value.
2. Input functions *f*: Calculates the aggregated net input signal to the neuron

$$u = f(x, w) \tag{4.28}$$

Where *x* and *w* are the input and weight vectors correspondingly; f is usually the summation function;

$$u = \sum i = 1, nxi.wi \tag{4.29}$$

3. An activation (signal) function s calculates the activation level of the neuron

$$a = s(u) \tag{4.30}$$

4. An output function calculates the output signal value emitted through the output (the axon) of the neuron;

$$o = g(a) \tag{4.31}$$

The output signal is usually assumed to be equal to the activation level of the neuron, that is,

$$o = a \tag{4.32}$$

The ANN have been used the first time to resolve the THD problem in [126], where the angles were chosen such that the fundamental was kept constant and the low-order harmonics were minimized or eliminated.

4.3. Optimization Simulations

The objective of this section is to find the best Angles in order to generate the lowest possible THD.

We have chosen to select the FFA to optimize the MLI. As a first step we increase the number of angles and we have chosen to optimize the THD of the 6 levels Multilevel inverters. We need to find the best switching angles in order to have the minimum THD.

The FA Pseudo-code presented in Figure 4.11 has been translated to a Matlab program. In all performed simulations we have used the parameters below:

IT = 40 maximum generation,

P = 50 population size,

K = 6 number of variables,

$\beta 0 = 100$ attractiveness at $r = 0$,

$\gamma = 1$ light absorption coefficient,

$\alpha = 100$ randomization parameter

We have built in a program to reduce the THD for *K* levels inverter. Program entries are the number of switching angles.

N is the order of the highest harmonic of the spectrum.

The fitness function we have used is the $\mathrm{THD}(\theta_1, \theta_2, \ldots . \theta_K)$ of the produced signal based on the first N harmonics of the FFT. The order of the highest harmonic N has been chosen as 60 to cover for all the low frequencies, practically we are working up to 3 KHz.

It is obvious that more switching angles will generate a better signal and therefore less THD. Below are simulation results for 1, 2, 3,4,5 and 6 angles, which correspond to 3,5,7,9,11 and 13 levels inverts.

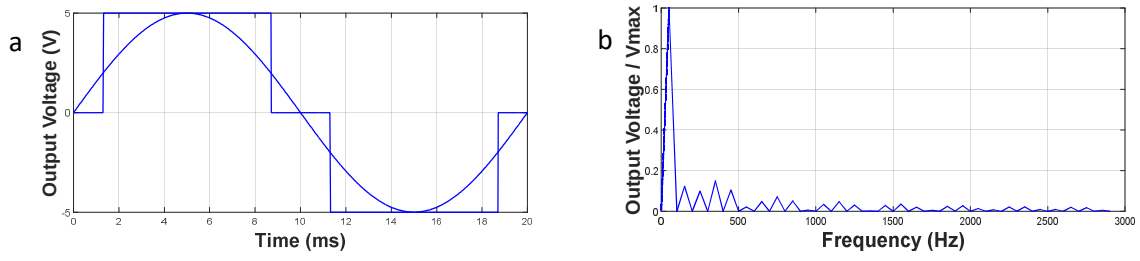


Figure 4.15: Three levels inverter output. (a) Time domain, θ_1=23.7˚. (b) FFT, THD= 28%.

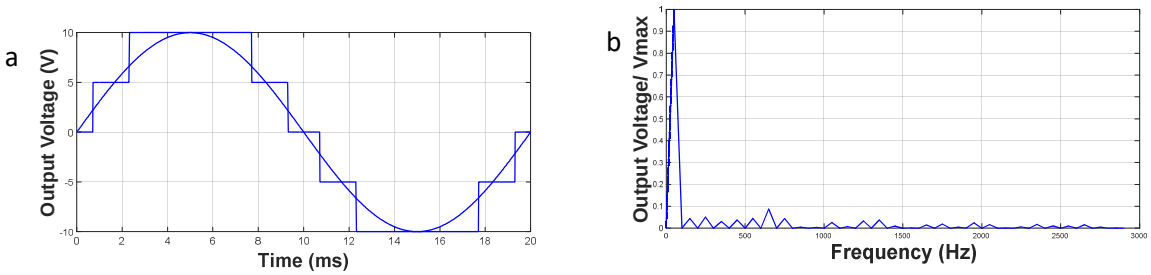


Figure 4.16: Five levels inverter output. (a) Time domain, θ1=12.8˚, θ_2=41.7˚. (b) FFT, THD =16%.

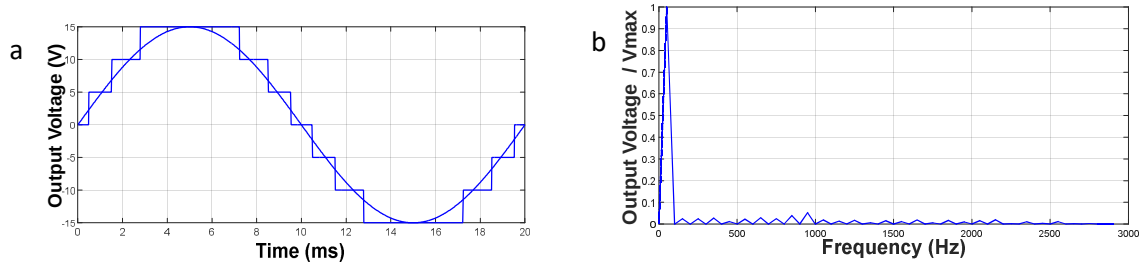


Figure 4.17: Seven levels inverter output. (a) Time domain, θ1=9.1˚, θ2=27.5˚, θ3=50.4˚. (b) FFT, THD= 11%.

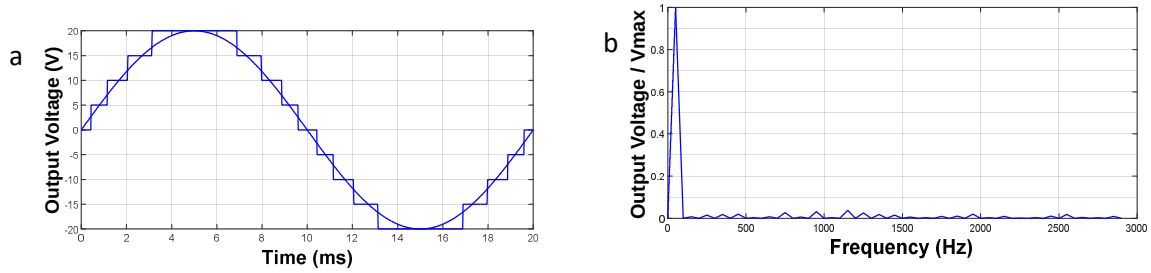


Figure 4.18: Nine levels inverter output. (a) Time domain θ1=8.0˚, θ2=21.0˚, θ3=37.1˚,θ4=56.5˚. (b) FFT, THD= 8%.

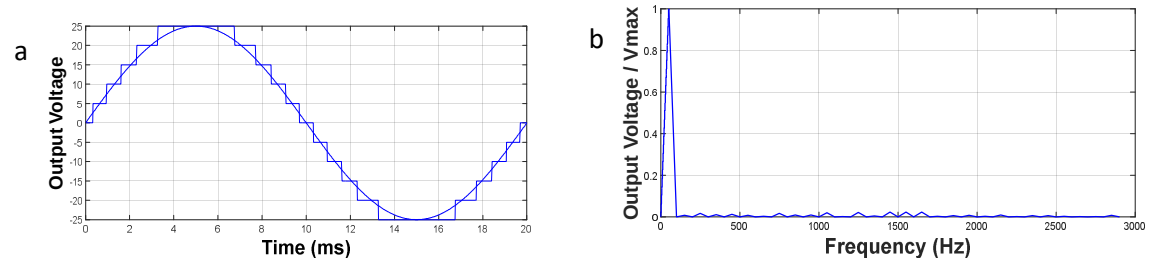


Figure 4.19: Eleven levels inverter output. (a) Time domain θ1=6.0˚, θ2=17.3˚, θ3=29.1˚ θ4=41.9˚, θ5=59.0˚. (b) FFT, THD= 6%.

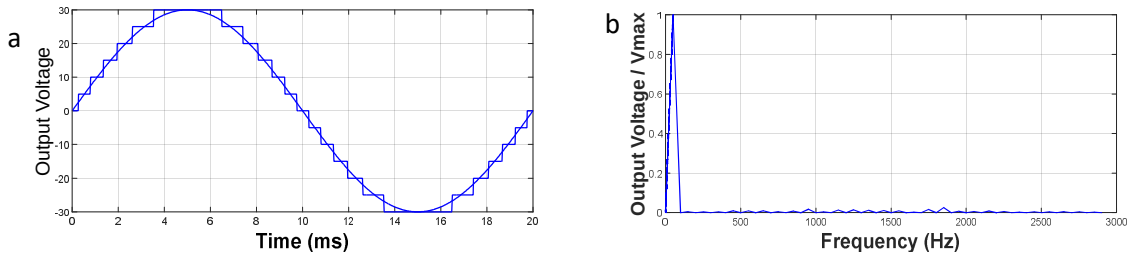


Figure 4.20: Thirteen levels inverter output. (a) Time domain θ1=5.0˚, θ2=14.3˚, θ 3=24.5˚, θ4=35.3˚, θ5=46.2˚, θ6=63.7˚. (b) FFT, THD = 5%.

Figure 4.15. shows the simulation results and the output of the 3 levels inverter, figure.4.13.a shows the waveform in the time domain, with the perfect waveform, a pure sin wave, Figure 4.15.b. Shows the FFT of the output signal.

Figure.4.16., figure.4.17., figure.4.18., figure.4.19. and figure.4.20. show the simulation results of level , 5,7,9,11 and 13 respectively.

Table 1 summarizes the simulation results, for level, 3, 5, 7, 9, 11 and 13 levels.

N˚ of Levels	THD	Max output Voltage	Optimum Angles
3	28%	Vdc	θ1=23.7˚
5	16%	2Vdc	θ1=12.8˚ θ2=41,7˚
7	11%	3Vdc	θ1=9,1˚ θ2=27,5˚ θ3=50,4˚
9	8%	4Vdc	θ1=8,0˚ θ2=21.0˚ θ3=37,1˚ θ4=56.5˚
11	6%	5Vdc	θ1=6.0˚ θ2=17.3˚ θ3=29.1˚ θ4=41.9˚ θ5=59,0˚
13	5%	6Vdc	θ1=5.0˚θ2=14.3˚ θ3=24.5˚ θ4=35.3˚ θ5=46.2˚ θ6=63.7˚

Table 1: Summary of simulation results, N˚ of Levels VS THD on 3K Spectrum.

The best THD has been found to be 5% for N=60, N is the order of the highest harmonic of the spectrum, corresponds to 3 kHz.

It is obvious that more switching angles will generate a better signal and therefore less THD.

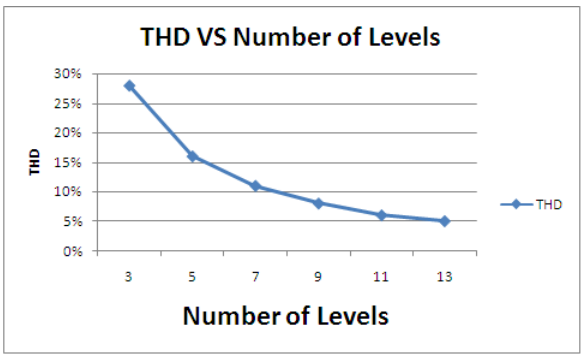


Figure 4.21: THD versus Number of Levels.

Compared to the work done in [127], where the obtained THD through the simulation was 12.39%, the optimized Angles were found through the Biogeography Based Optimisation algorithm, the waveform is similar to the one generated by a symmetrical multilevel inverter , with a step of 100. While in our proposed method we have reached 11% THD, result obtained by running 10 iterations of the built program based on the recent FFA.

In order to reach the 5% THD we had to go up to 13 levels inverters, simulation results summary are shown on Figure 4.21.

We have also compared the proposed FFA to the GA tool on Matlab see Figure 4.22, the proposed FFA with the suggested parameters converges faster, it is 90% close to the optimum solution after the fourth iteration, usually the optimum solution is obtained before the 10^{th} iteration .

In order to resolve the same problem, when using the GA with parameters, IT=20, Population size=50, the best obtained fitness value with the GA is 3.9 times the value obtained by the FFA. To obtain similar result with the GA we need 150 Generations.

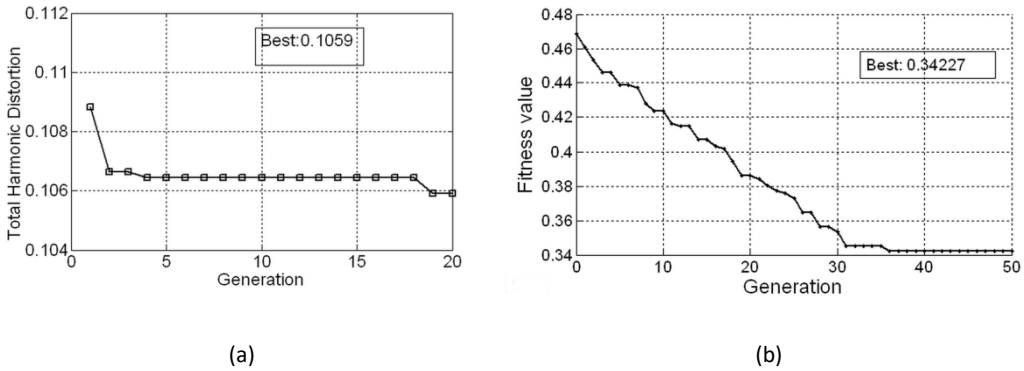


Figure 4.22. Firefly Algorithm THD vs. Generation (a), Genetic Algorithm THD vs. Generation (b).

4.4. Conclusion

We have presented in this chapter the different methods to optimize the THD, Numerical, Algebric and Nature inspired methods.

We have a given to a certain extend most of the ones used specifically to resolve the THD problem.

we have selected the recent firefly algorithm to find the best switching angles in order to minimize the THD on a user defined bandwidth.

The method focuses on optimizing directly the THD and not to resolve the equations or minimize a selected number of harmonics.

The THD over the predefined range was minimized. The best THD found through the simulation is 5% on a bandwidth of 3 kHz.

Under the same conditions (3 kHz bandwidth and 50 Hz fundamental), we have compared the recent FFA to the BBO algorithm developed in [127] and the GA implemented in Matlab. Obtained THD by the BBO algorithm [127] was 12.39% while the obtained THD by using the recent FFA was 11%. In this specific problem, the FFA, compared to the GA, converged faster.

Chapter 4

Practical implementation, experimental tests & Results

5.1. Introduction:

We remember that our first motivation is to make an inverter with the lowest THD. During the progress of the project, we had some other considerations. The MLI will not serve as a UPS only but also can drive AC motors, can convert the frequency, can have multiple applications, and the work can be a good pedagogic support tool , and will definitely help our students understanding the MLI and connecting to the real world.

We have considered the modularity of the design. Number of sources connected now is six (6), but can be easily extended. Can interface the renewable Energy systems.

The power of this MLI can be increased by installing power components instead the ones installed on the prototype.

This MLI is easy to program, modifying the program of the PIC 16F628A will modify the behavior of the MLI.

Getting into the lowest THD has required a thorough survey of the hardware and the software a combination of one of the best existing optimized hardware structures with the recent firefly algorithm, which was used to optimize the THD, are used within this project.

We consider that the main objectives of the project were reached and that this project will be the beginning of having a socioeconomically impact.

5.2. Selecting the best hardware structure

As previously stated on chapter 2, many structures were proposed. The main structures are:

- Diode-clamped inverter (neutral-point clamped).
- Flying capacitor (capacitor-clamped).
- Cascaded H bridge multilevel inverters with separated dc sources.

Since we were aiming to use our inverter within a renewable energy system, the best type which fits in was the cascaded H-bridge that will be naturally feed by different DC sources, like Solar cells.

We will benefit from all the other advantages of the cascaded H-Bridges like:

- Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.
- Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors.
- Easier control strategy than the diode clamping and flying capacitor.

Figure 5.1 is showing the basic cascaded H Bridge seven levels MLI with symmetrical dc sources.

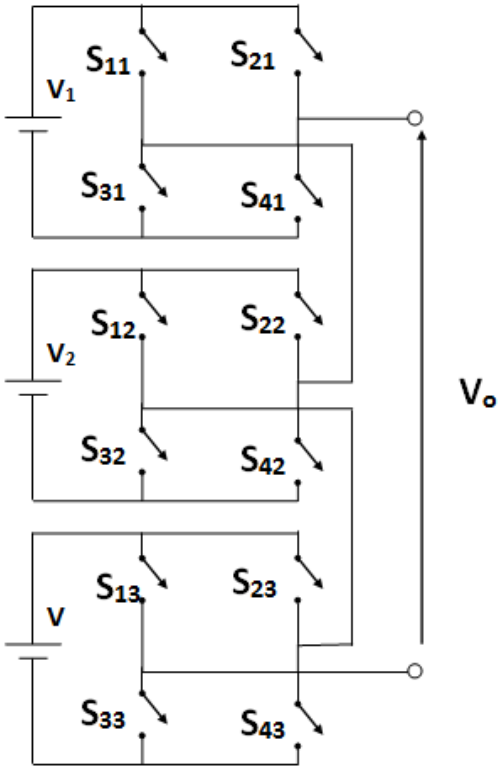
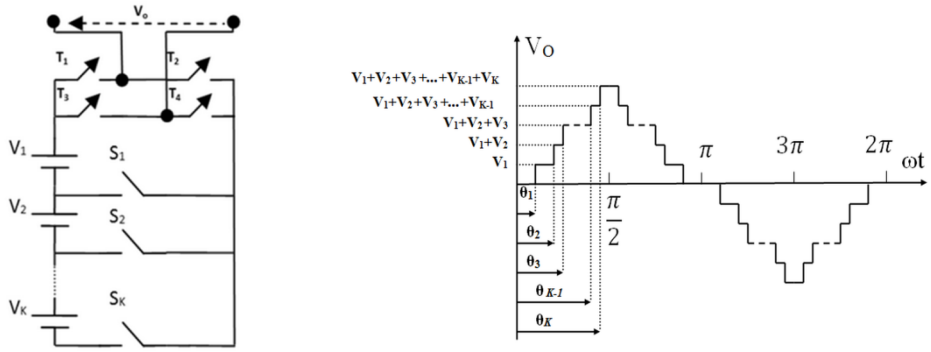


Figure 5.1: Configuration of cascaded H Bridges 7 levels MLI

The variance structure that we have chosen is the one on figure 5.2 (a) presented on [128] has shown a model with reduced number of power components.



(a) (b)

Figure5.2: (a) Sub-multilevel topology [128]; (b) typical output voltage of MLI in [128]

The reference publication [128] was an inspiring paper, looking at its symmetric model, the number of switches proposed is reduced compared to the Cascaded H Bridge configuration. This has allowed dropping the number of switches and therefore the reduction of control complexity and gate driver circuits.

Table 1, shows a quick comparison between the basic structure, cascaded H Bridge, and the proposed design in [128] to be utilized to build the MLI .

Parameter	Basic CHB	Inverter in [128]
$N_{dc\ PWRSP}$	K	K
N_{levels}	2K+1	2K+1
$N_{Switches}$	4K	K+4
Vo,Max	KVdc	Kvdc

Table 5.1: Comparative table between the proposed structure in [128] and the basic CHB MLI.

Where:

$N_{dc\ PWRSP}$ is the number of DC power supplies of the MLI.

N_{levels} is number of output levels of the MLI.

$N_{Switches}$ is number of switches used in the MLI.

$N_{Transistors}$ is number of switches used in the MLI.

Vo,Max The maximum obtainable output voltage of the MLI.

For 13 levels, the basic MLI will need total number of 24 switches (14 Transistors), while the proposed design in [128] uses only 10 switches (10 Transistors).

Considering the symmetric model, this is resulting to a significant reduction of the number of Transistors, with an equivalent output.

5.3. The thirteen level MLI design:

5.3.1. Hardware Design:

The thirteen level inverter was built around a microchip microcontroller type PIC16F628A.

The multilevel inverter consists of 4 major parts:

1) Processor card: this is the brain of the inverter; it generates all the switching angles, to activate the switches to generate the exact angles to minimize the THD.

The best results found through the simulation, by using the FFA have been programmed on the PIC 16F628A, targeting the 5% THD.

2) Switching card: this card contains the switching devices and isolates the control from the power (photo couplers), it takes controls from the processor card and switches power from the batteries pack to the H-Bridge.
3) Batteries pack: directly connected to the switching card and both make the levels generator.
4) H-Bridge card: the input of the H-bridge is half wave, the H Bridge will make the full wave at its output, and feeds the load. The H-bridge is also controlled by the microprocessor.

The block diagram is shown on figure 5.3.

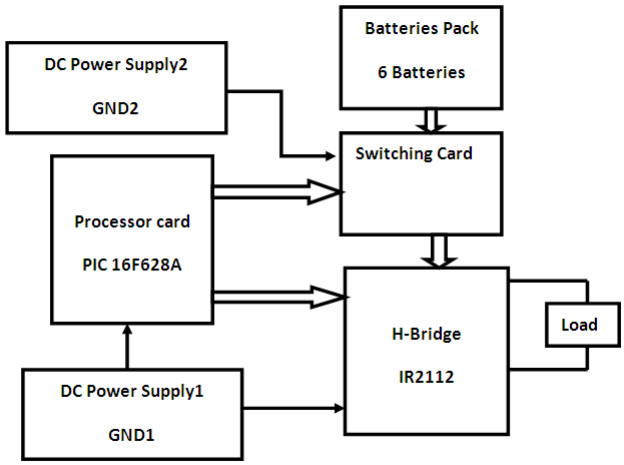


Figure 5.3: Block Diagram of the multilevel inverter

A simplified schematic is presented in figure 5.4. It describes the levels generator and the H-bridge.

1) Levels generators: consists of the switching card and the battery pack, it is a stack of basic level cells, a basic cell consists of a voltage source, a switch and a diode. V_1, S_1 and D_1 is one basic cell. The diode will avoid shorting the power supply if the switches are both on at the same time, in that case the highest voltage will feed the H-Bridge. This design allow the structure to be easily modified to accept more levels, adding another level requires adding another basic cell , which consists of power supply , switch and diode, the control circuit on the micro controller block will also need to be upgraded to control the additional cell.
2) H Bridge, built around IR2112, MOSFET / IGBT driver, will have a rectified signal at its input and alternates the current across the load.

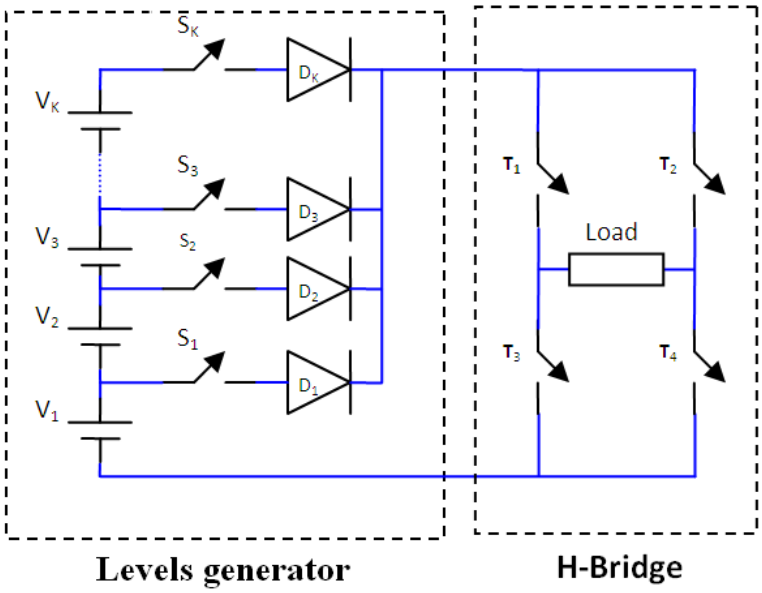


Figure 5.4: Simplified Schematic of the proposed symmetric multilevel inverter.

For the symmetric MLI case, $V_1=V_2=…..V_K$ =Vdc.

S_i switch is connecting power supply V_i to the H-bridge, and will generate iVdc, i varies from 1 to K , K is the total number of DC power supplies.

Diodes D1….DK role is to avoid current flow from higher level to lower level, if accidently two switches are activated, the input at the H-bridge will be the one coming from highest voltage source.

The half wave will be generated through the levels generator, the H-bridge will invert alternatively the wave through the T1 through T4 switches to generate the AC signal.

Si or Ti switches are unidirectional switches, can be Power MOSFETs or Insulated Gate Bipolar Transistors with anti-parallel diode, we have used power MOSFETs IRF620 in our prototype.

As previously stated we have only 2 isolated ground Gate driver power supplies , the first isolated gate driver power supply is 5V and 12V to feed the H bridge, the second power supply to feed the switching card to allow the control of the levels generator. The first Power supply feeds also the Microcontroller card.

Figure 5.5 and figure 5.6 show the 13 status of the inverter, figure 5.5 illustrates different possible states to generate a positive waveform, while figure 5.6 illustrates the negative waveform. Table 2.5 shows the output voltage based on the switches status.

As we see on table 5.2, the control strategy is simple and only 3 switches are controlled at the same time.

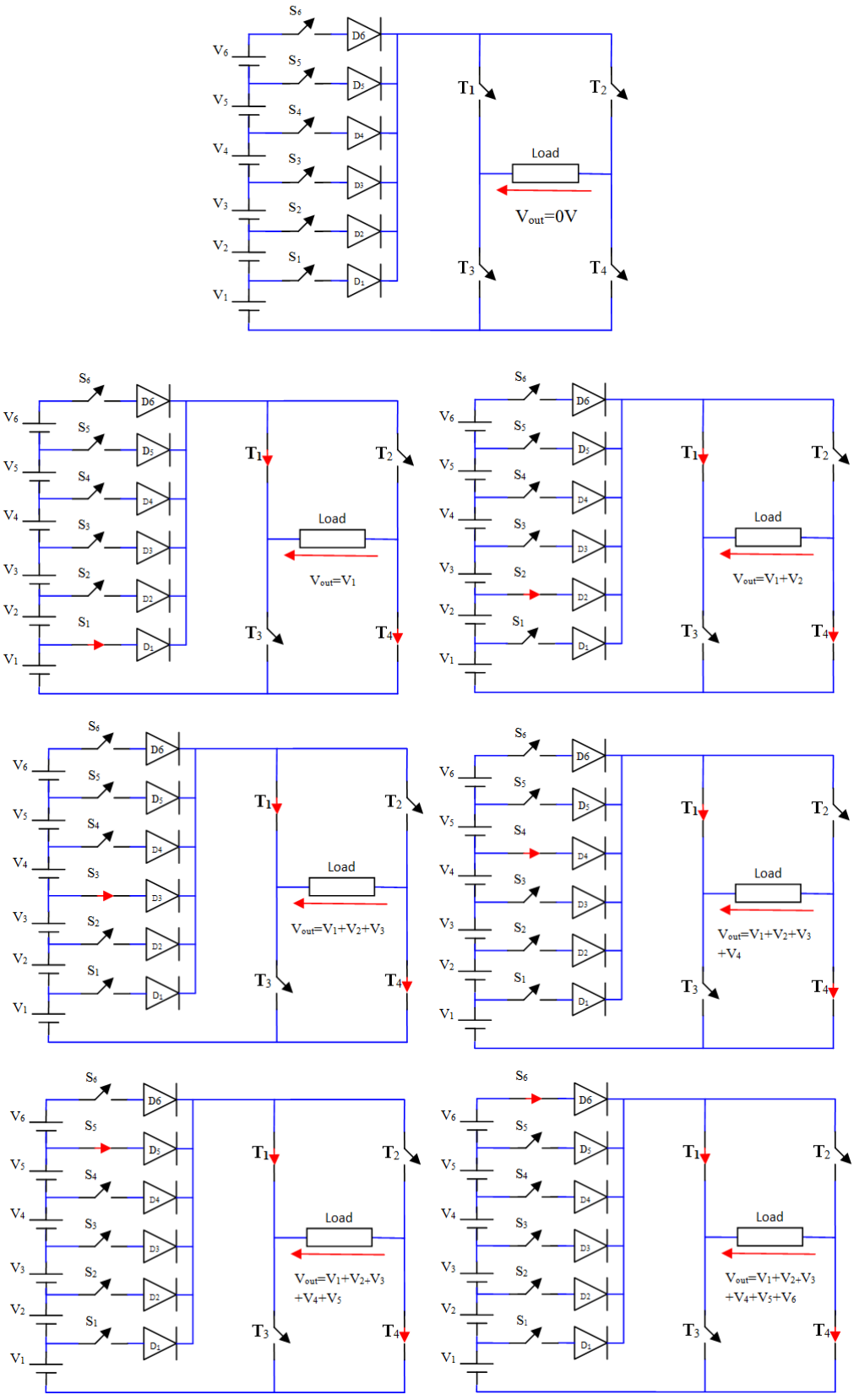


Figure 5.5: Different states of the 13 levels inverter. V_{out} Positive.

1)State 0, $V_{out}=0V$, *2)*Status 1, $V_{out}=V_{dc}$, *3)* Status 2, $V_{out}=2V_{dc}$,*4)* Status 3, $V_{out}=3V_{dc}$.

5)Status 4, $V_{out}=4V_{dc}$, *6)* Status 5, $V_{out}=5V_{dc}$, *7)* Status 6 $V_{out}=6V_{dc}$.

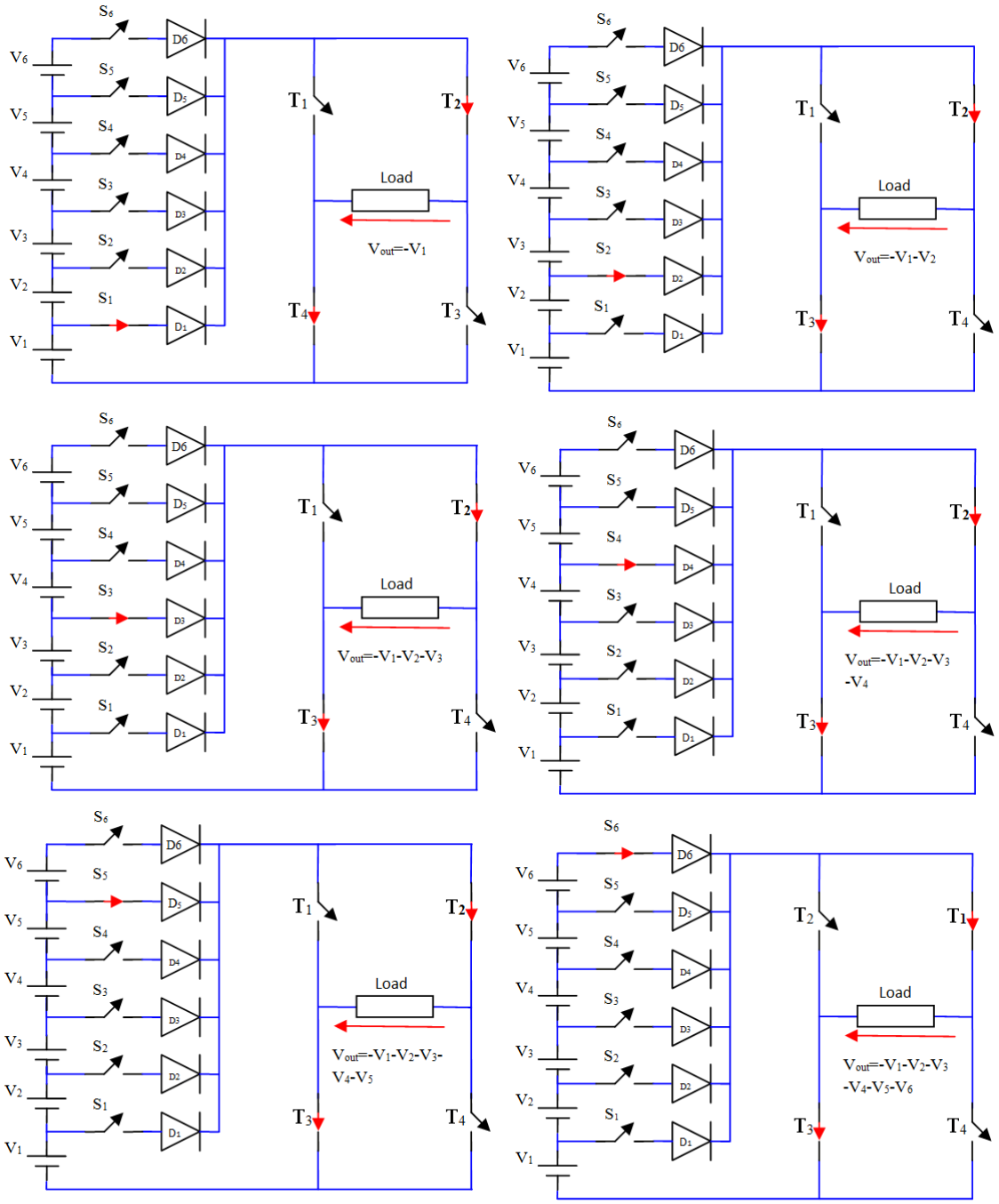


Figure .5.6: Different states of the 13 levels inverter, V_{out} , Negative.

8)State 7, V_{out}=-*Vdc, 9)*Status 8, V_{out} =-$2V_{dc}$, *10)* Status 9, V_{out} =-$3V_{dc}$, *11)* Status 10, V_{out} =-$4V_{dc}$.

12) Status 11, V_{out} =-$5V_{dc}$, *13)* Status 5, V_{out} =-$6V_{dc}$.

State	Switches states										V_L
	S_1	S_2	S_3	S_4	S_5	S_6	T_1	T_2	T_3	T_4	
0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	1	V_1
2	0	1	0	0	0	0	1	0	0	1	V_1+V_2
3	0	0	1	0	0	0	1	0	0	1	$V_1+V_2+V_3$
4	0	0	0	1	0	0	1	0	0	1	$V_1+V_2+V_3+V_4$
5	0	0	0	0	1	0	1	0	0	1	$V_1+V_2+V_3+V_4+V_5$
6	0	0	0	0	0	1	1	0	0	1	$V_1+V_2+V_3+V_4+V_5+V_6$
7	1	0	0	0	0	0	0	1	1	0	$-V_1$
8	0	1	0	0	0	0	0	1	1	0	$-V_1-V_2$
9	0	0	1	0	0	0	0	1	1	0	$-V_1-V_2-V_3$
10	0	0	0	1	0	0	0	1	1	0	$-V_1-V_2-V_3-V_4$
11	0	0	0	0	1	0	0	1	1	0	$-V_1-V_2-V_3-V_4-V_5$
12	0	0	0	0	0	1	0	1	1	0	$-V_1-V_2-V_3-V_4-V_5-V_6$

Table 5.2: Output voltage for different switches status of the 13 levels inverter .

5.3.2. Hardware Simulations

After the design on paper, the next step was to ensure the functionality of the inverter at minimum cost, the simulation has helped us moving faster, without having to physically do all the checks, we have used the available CAD tools, the steps design -simulate, have been repeated , and on every simulation we have checked the performance until we had acceptable results**.**

All different blocks have been simulated individually, and the last step was connecting all the blocks together, the functionality of the end product has been verified.

5.3.1.1. Microcontroller card Simulation:

After identifying the best switching angles through the firefly algorithm in Matlab, these ones were entered into the PIC16F628A; the programs have been checked the first time on Proteus.

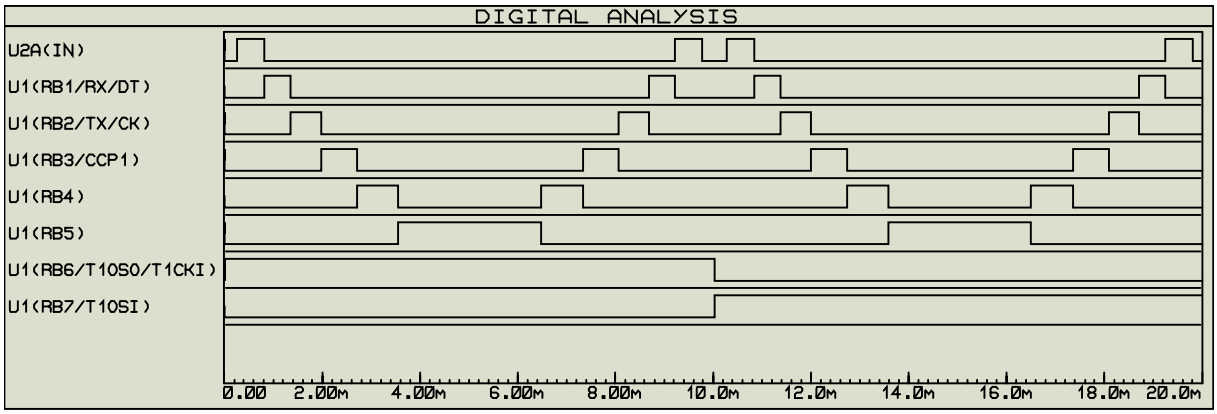


Figure 5.7: 13 level MLI control bits chronogram.

As previously shown, the best switching angles for a 13 levels inverter were found through the firefly algorithm, in Matlab. The first step was to simulate the functionality on a PIC16F628A; these angles were entered and converted to a program were the outputs were checked on Proteus. See figure 5.7

5.3.1.2. Switching card simulation

Many simulations done to ensure that we have the expected signal at the output of the switching card. A rectified signal at the output can be seen as in figure 5.8. The Fourier analyses of the signal is also shown and that is clearly showing 100Hz. See figures 5.9 and 5.10.

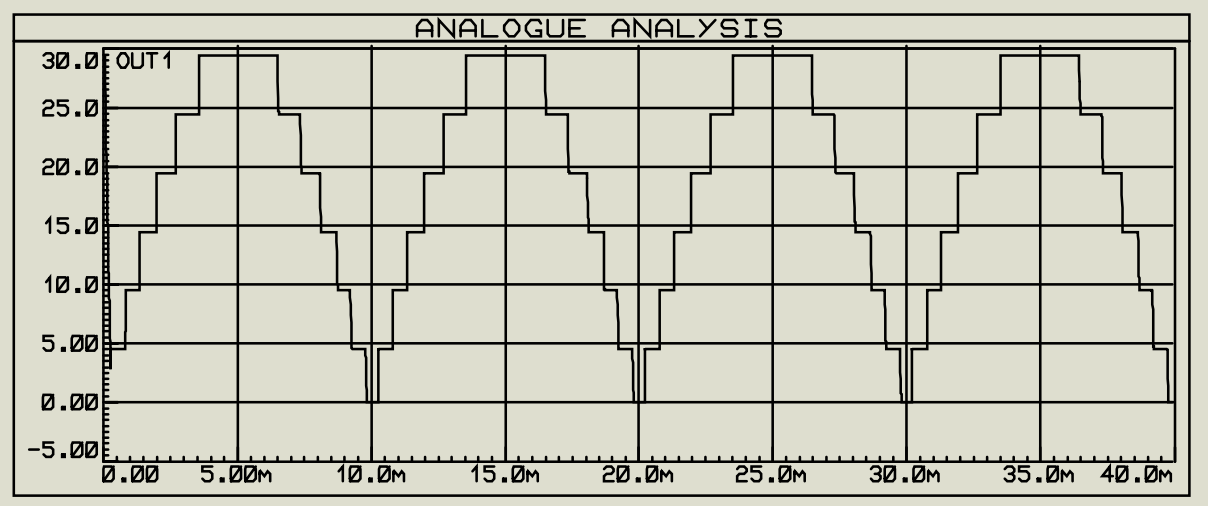


Figure 5.8: Output of the switching card.

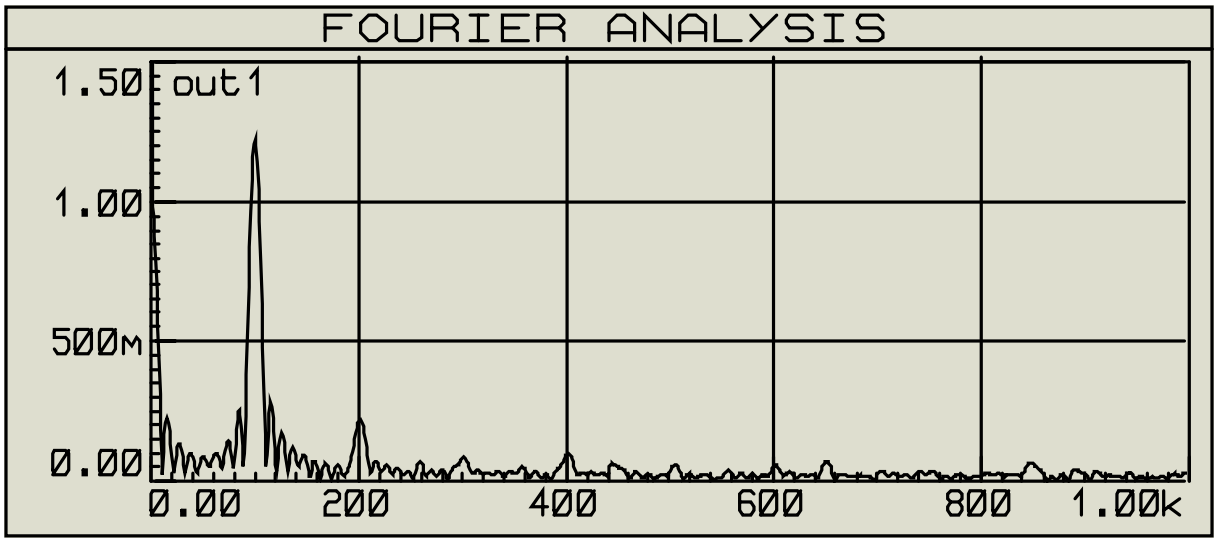


Figure 5.9: Fourier Analyses of the output of the switching card, 1KHz bandwidth.

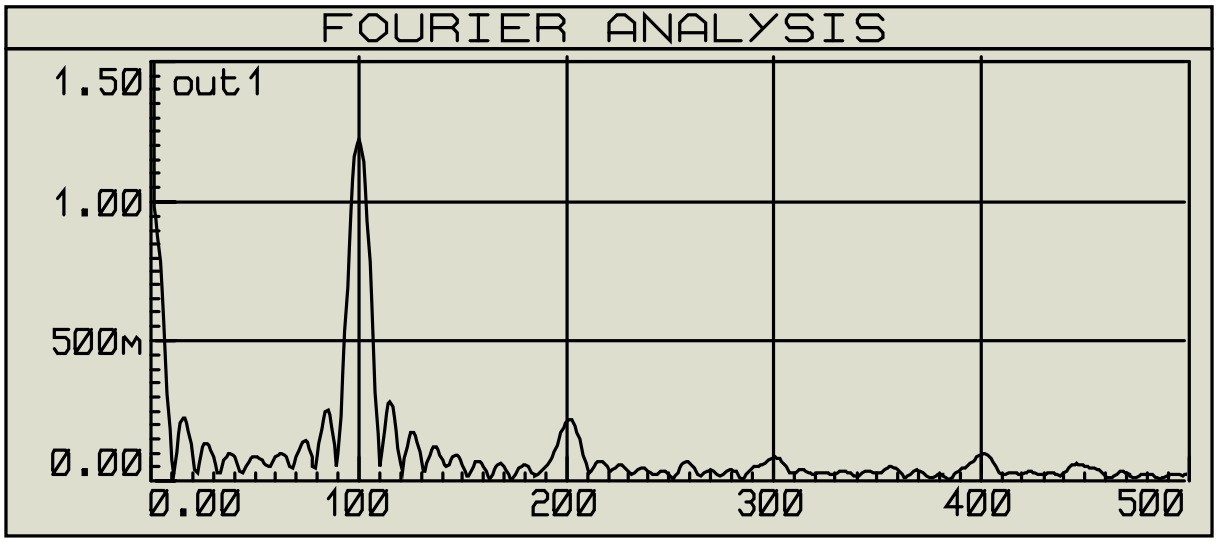


Figure 5.9: Fourier Analyses of the output of the switching card, 600 Hz, bandwidth.

5.3.1.3. H-bridge card simulation

The Hbridge card has been developed around the IR2112, this has been simulated on Proteus and verified timings, and controls. See figure 5.10 where a single level has been tested.

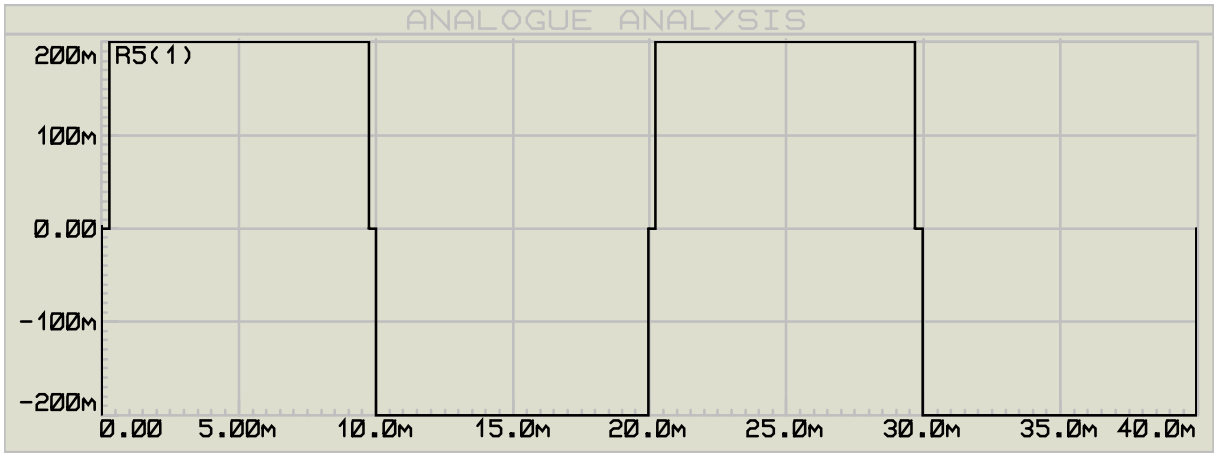


Figure 5.10: Output of the H-Bridge, time domain, one level

5.3.1.4. Connecting the blocs-13 levels MLI simulation

Figure 5.11 shows the output of the 13 levels MLI after connecting all the blocks , , this output is the current through a resistive load , must have the same shape of the output voltage. Figure 5.12, figure 5.13 are showing the spectrum of the same signal in different bandwidths to show the value of the most important harmonic.

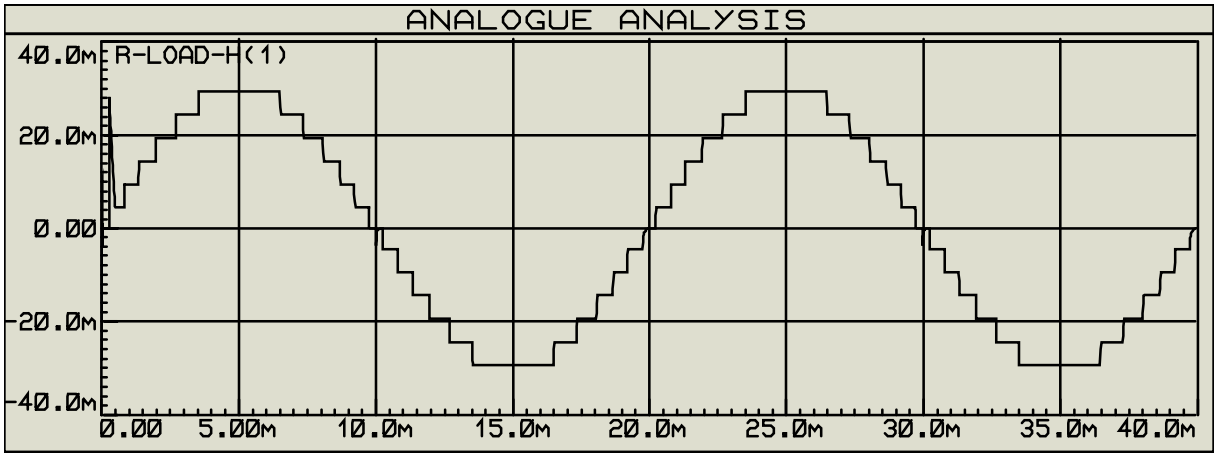


Figure 5.11: output of the simulated 13 levels MLI, time domain

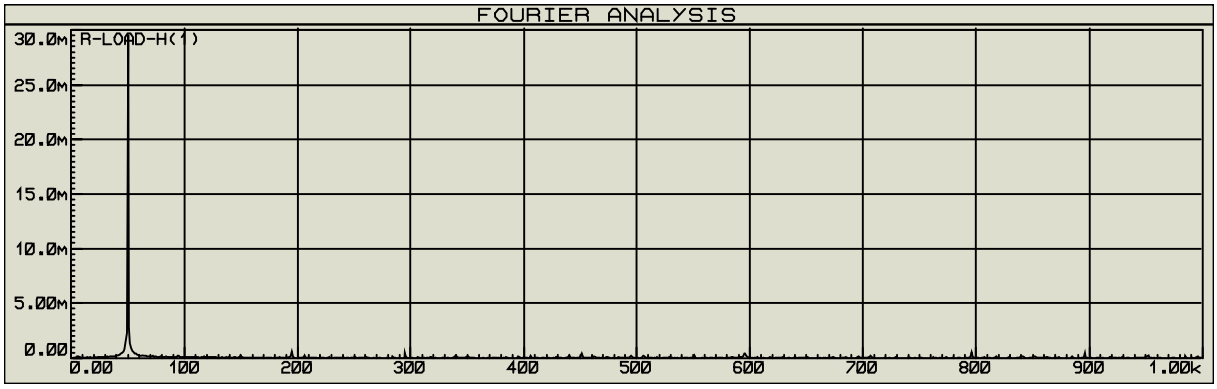


Figure 5.12: output of the simulated 13 levels MLI, frequency domain. 1 KHz bandwidth.

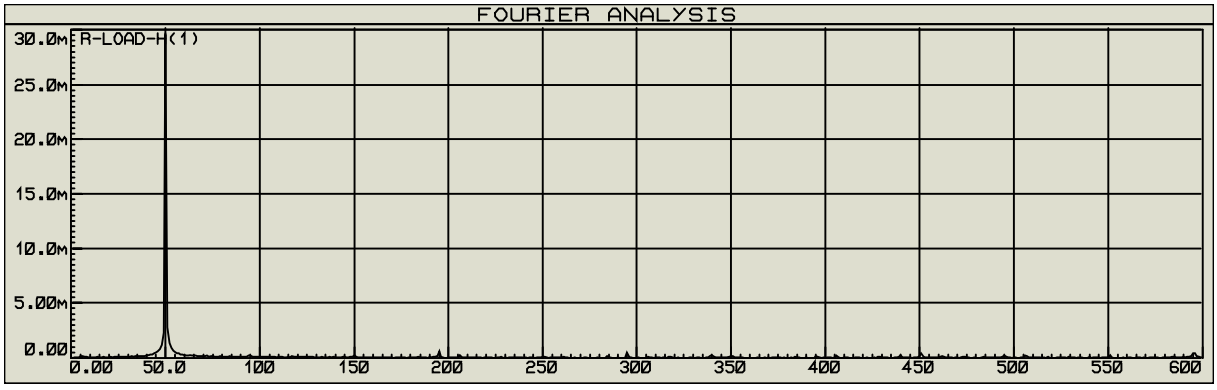


Figure 5.13: output of the simulated 13 levels MLI, frequency domain. 600 Hz bandwidth.

5.4. Experimental tests :

The multilevel inverter has been built and tested, the best values of the angles, corresponding to the lowest THD found during the simulations have been used, the optimum results have been programmed in PIC 16F628A in order to make the desired system.

Three prototype cards have been made, Processor card, levels generator card and the H-Bridge card.

Tests have been conducted with different loads to check the performance of the MLI.

The first set of experiments has been done with a resistive load.

Figure 5.14 shows the thirteen (13) levels inverter running with a resistive load.

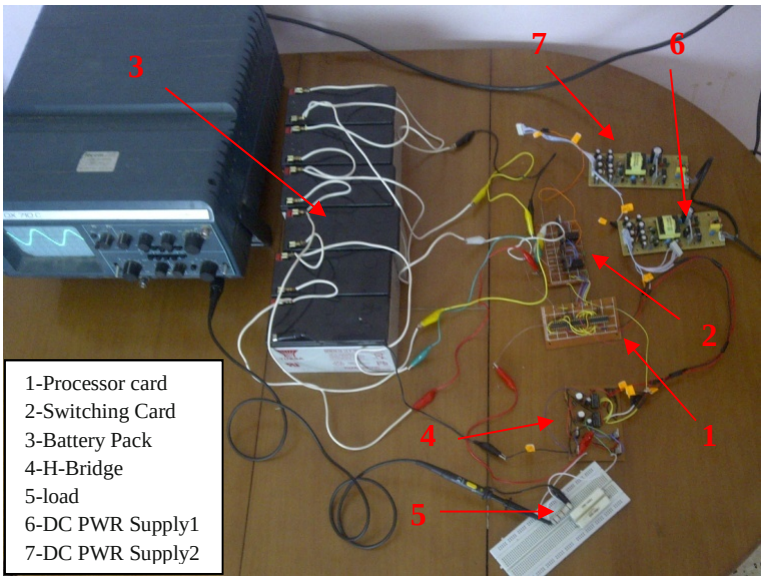


Figure 5.14: The 13 levels multilevel inverter running with Resistive load.

The experimental results have confirmed the theory, with an R load the THD was 4.6 % on a spectrum of 3KHz .

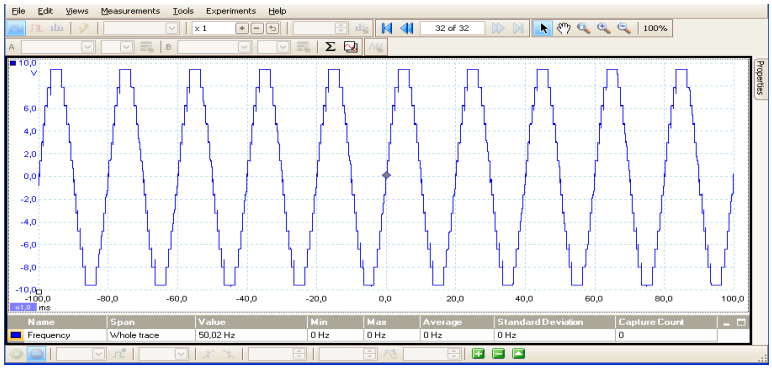
Figure 5.15.a shows the current in a resistive load, on a digital scope, signal frequency 50Hz, while figure 5.15.b Shows the spectrum of the output signal up to 3 KHz**.** The measured value of the THD was 4.6% .This is a satisfactory result as we were targeting 5% THD .

The second set of experiments was done with 100mH induction load. Figure 5.16.a shows the current waveform where the load is a 100mH. More harmonics have been filtered and we see that the resulting THD is 3.2%, this is shown on figure 5.16.b.

Figure 5.17. and figure 5.18 show the output voltage ,from the 13 levels MLI, and the current through a motor load on an analogues scope, current pick is 2.5 Amps.

Figure5.19 shows the conceived MLI running an AC Motor.

a



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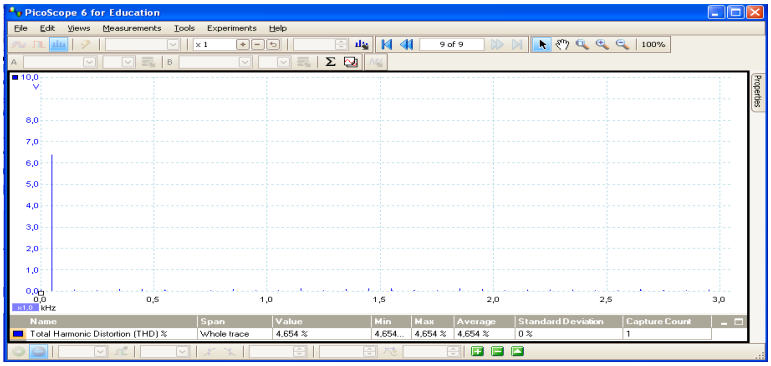
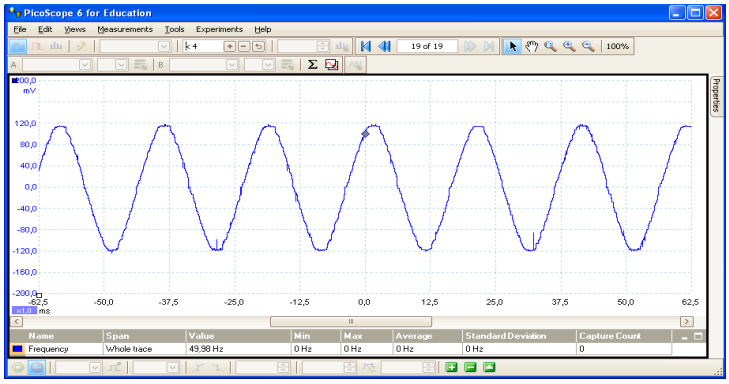


Figure 5.15: The 13 levels inverter with a Resistive load. (a) current waveform.(b) Current FFT 3KHz-THD=4.65%.

a



b

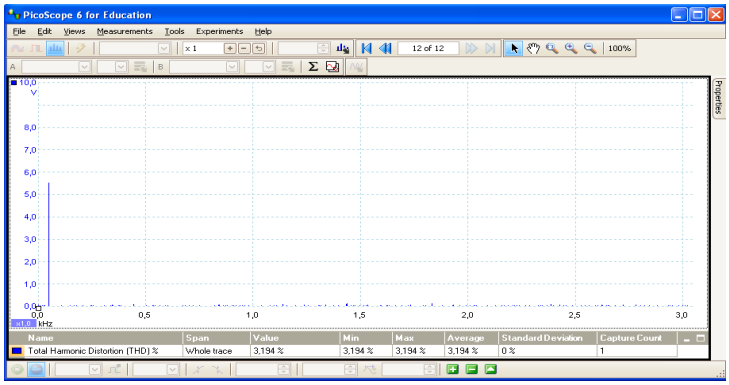


Figure 5.16: the 13 levels inverter with an Inductive load L=100mh. (a) Current waveform. (b) Current FFT 3 KHz-THD=3.2%.

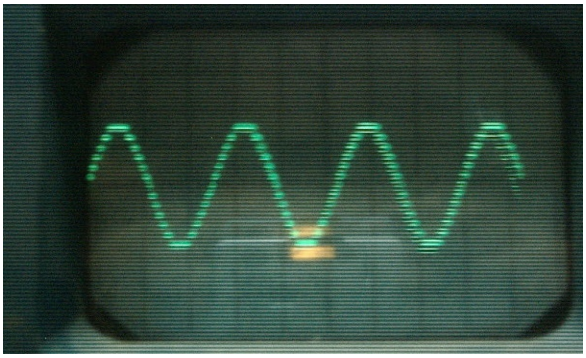


Figure 5.17: 13 levels inverter. -Output Voltage on an Analogue Scope.

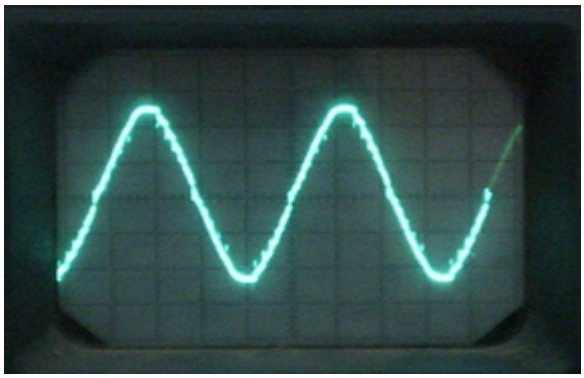


Figure 5.18: 13 level inverter Current through Motor load on an Analogue Scope.(2.5Amps pick).

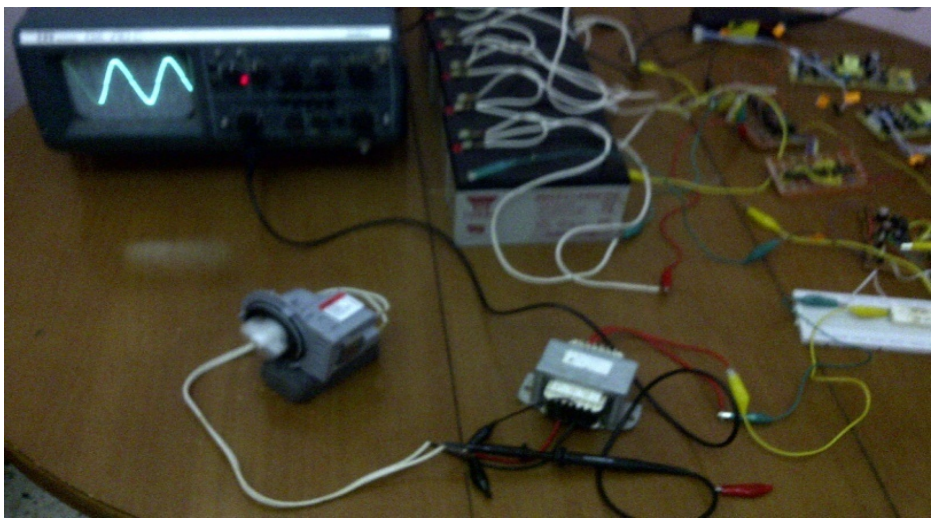


Figure.5.19: The 13 levels inverter with Motor load running.

5.5. Conclusion

The recent firefly algorithm has been used to find the best switching angles in order to minimize the THD on a user defined bandwidth. The method focuses on optimizing directly the THD and not to resolve the equations or minimizes a selected number of harmonics.

The THD over the predefined range was minimized. The best THD found through the simulation is 5% on a bandwidth of 3 kHz.[31]

One of the best optimized hardware structures of MLI has been used [128] to verify and validate the simulation results

The signal generated by 13-level symmetric inverter has a low THD, and the measured THD is 4.8% on a bandwidth of 3 kHz, which is a satisfactory result. Simulation results as well as experimental results have been shared to prove the performance of software solution and the used hardware structure.

One of the additional features is that the proposed design is using only 2 isolated grounds Gate driver power supplies.

The design can be easily extended to higher levels by stacking more basic cells.

Conclusion-Summary and future work

6. Conclusion-Summary and future work

Power electronics involves the study of electronic circuits intended to control the flow of electrical energy, in this thesis we have tried to give a small contribution to the inverters control discipline. It is very difficult to put all the information in one thesis, and we think that we have at least covered the basics, on hardware and control, we have also stressed on the need of treating both problems at once in order to get the best product.

While inverters have different characteristics, such as efficiency, reliability, losses ...etc, we have chosen to challenge one of the most indicative characteristics, which is the THD.

The THD is certainly one of the most important MLI performance, and is one of the essential research axes, many industrial application may allow 5% THD, which was our predefined goal.

In Chapter 2, we have presented the state of the art of the multilevel inverters topologies, presented the 3 main ones , Diode clamped, Flying Capacitors and Cascaded H-Bridges. We have also presented emerging structures through the combinations of one or more basic topologies.

A survey has been done, and we have chosen one of the best-optimized structure, which has reduced the number of power devices and therefore the price of the total product.

In Chapter 3, we have presented the PWM control strategies; presented Sine-Triangle PWM, Selective Harmonic Elimination, space vector modulation, space vector control and one-dimensional modulation.

In our case, we have not used any of these methods, but went to the basic problem, and wanted to minimize the THD on 3 kHz bandwidth.

We had to model the problem in Matlab in order to use its fantastic processing capabilities.

We have also used the recent firefly algorithm, one of the newest metaheuristic algorithms, swarm intelligence methods in order to find the best switching angles.

In chapter 4, we have gone through the most important methods used for optimization, and put more details on the ones used in particular to resolve the THD problem.

The key was to connect the best hardware structure with the best optimization method, in order to get the most effective solution. Through Matlab, the simulations have showed that we can reach 5% THD, on a 13 level MLI.

In Chapter 5 we have shown the way of materialising the experiments, starting from the best structure chosen, the best angles obtained from Matlab simulations through the FFA , we

have implemented the best Angles in the micro controller. First, to ensure the basic functionality, we have simulated the different blocks, and visualized the outputs.

As a last step, we have shown the experimental results, on different loads, resistive and inductive, the results were fascinating, the obtained THD on the spectrum analyser, was less than the expected 5%.

The signal generated by 13-level symmetric inverter has a low THD, and the measured THD is 4.8% on a bandwidth of 3 kHz, which is a satisfactory result. Simulation results as well as experimental results have been shared to prove the performance of software solution and the used hardware structure.

The proposed design is using only 2 isolated grounds gate driver power supplies, is modular and expandable to further levels.

We remember that our first motivation is to make an inverter with the lowest THD, at the end we have realized a product that can fit different needs:

- It can be used as a UPS.
- Can be used as a frequency converter and drive AC motors.
- Will be a good pedagogic tool, and will definitely help our students understanding the MLI and connecting them to the real world.

We consider that the main objectives of the project were reached and that this project will have a socioeconomic impact.

- We have concluded that we have to address the hardware and the control, both at the same time in order to obtain the best results.
- We have reduced the THD down to 5% in accordance to the standard of IEEE 519-1992, amended by IEEE 519-2014.
- We have reduced the number of switches, which reduced the cost of the inverter.

To note one more time, that we did not include a comprehensive study of semiconductor devices, electronic schematics, prototype boards and further hardware details in the thesis. This was not within the main aiming of the subject. It is important to mention that a thorough knowledge and understanding of these disciplines is required to perform practical tests and develop the hardware in a safe and productive manner.

We are open to provide any details if requested. The hardware and all the programs are part of the intellectual property of university of Batna2 (Mostefa Ben Boulaïd), were the work has been performed.

As for future work, on the backbone of our modest contribution through this thesis, it will be beneficial to:

1. Increase the power of the MLI, this can be done by modifying the existing one, the same circuit will be able to drive IGBT, we can easily increase the power by replacing the IRF620 the THD is at an acceptable level, and the control system can drive High Power IGBTs. Note that the actual output power is 5.2 X 72 =374.4 W.

   Just by installing CMOS Transistors IRFP240, the Power can jump to 20X72= 1440W, installing IGBT G4PC40FD, will make the power going up to 27X72=1944W, and can easily cross the 2KW if the temperature of the chip can be maintained less than 100 deg C.
2. Use a different waveform, we have used the basic stair waveform, by changing the waveform, and increasing the switching frequency we can reduce the further the THD, example use the same method to reduce the THD of a 3-level UPS by adding more angles on the 3-levels inverter.
3. Develop and explore other structures as the asymmetrical models, these last ones offers the options of more levels and better performance, therefore more elasticity of the design, possibly reducing more the switches.
4. Explore the model of control in a three-phased system.
5. Interface real renewable energy sources, solar or wind energy.
6. Making smarter inverters, as fault tolerant inverters, as an example, when one component fails, it can be detected, and isolated, can continue running with an acceptable performance, this will avoid drastic shutdowns that can be destructive in many cases. This last application will need to implement the algorithm on a real time system, since the FFA is showing a faster feature than most of the known algorithms.

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