People's Democratic Republic of Algeria
Ministry of Higher Education and Scientific Research

University of Batna 2 – Mostefa Ben Boulaïd
Faculty of Technology
Department of Electronics

Dissertation

Prepared within the Advanced Electronics Laboratory (LEA)

Presented in fulfillment of the requirement of the degree of:

Doctor of Science in Electronics
Option: Microelectronics

Entitled:

Contribution to study and modeling of the nanoscale multi-gate transistor using neural and evolutionary techniques

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April 2018

République Algérienne Démocratique et Populaire
Ministère de l'enseignement supérieur et de la recherche Scientifique

Université de Batna 2 – Mostefa Ben Boulaïd
Faculté de Technologie
Département d'Electronique

Thèse

Préparée au sein du Laboratoire d'Electronique Avancée (LEA)

Présentée pour l'obtention du titre de:

Docteur en Sciences en Électronique
Option : Microélectronique

Sous le Thème:

Contribution à l'étude et la modélisation du transistor nanométrique à multi-grille en utilisant les techniques neuronales et évolutionnaires

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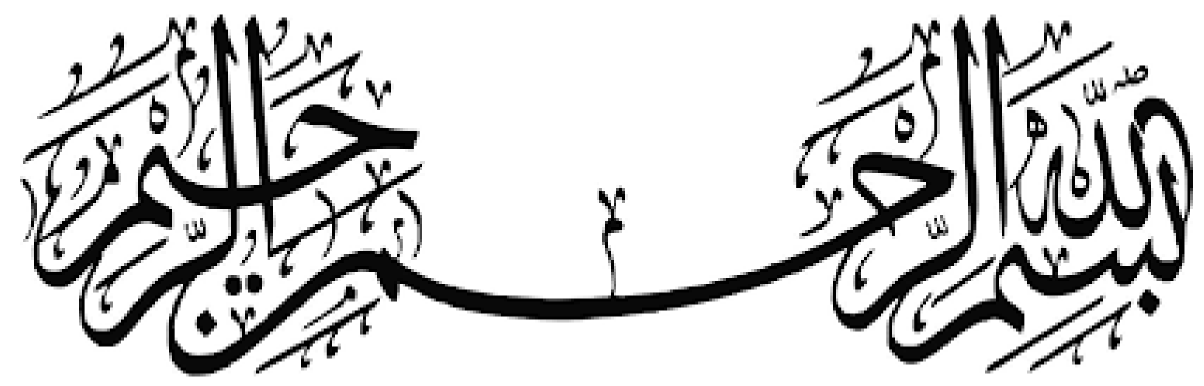
Avril 2018



In The Name Of Allah The Most Beneficent The Most Merciful

Au Nom D'Allah Le Tout Miséricordieux Le Très Miséricordieux

DEDICATION

This dissertation is dedicated to my best friend, my most loyal companion, my beautiful amazing life companion. The one person who knew me, the one person who protected me, the primary reason to any of my achievements, the one person who I loved unconditionally. The true love of my life- my mother-.

Acknowledgments

First of all, I am deeply grateful to **The Almighty Allah (SWT)**, the Most High, the Most Compassionate, and the Most Merciful for all his giving and for the opportunity He gave me to study, to research and to write and finalizing this Ph.D. project. I Thank **Allah,** my utmost thanks, for providing me this opportunity and granting me the capability to proceed successfully.

I cannot express enough thanks to my supervisor ***Professor Fayçal DJEFFAL***, who accepted me as his Ph.D. student at the Department of Electronics, supported my whole graduate life, suggested the topic and provided the platform to complete the project, helped in every step of the way, always believed in me and never hesitate to provide relentless support and motivation at all times throughout all these years. My completion of this work could not have been accomplished without his deepest expertise and the most shrewder insight. Many thanks for his permanent availability and responsiveness to my requests and for giving his time and effort without reservation. I would also like to express my appreciation for his guidance during my study. Without which this research would never have reached this point. And assisting me throughout my thesis-writing period; providing encouragement, good company, and lots of good ideas I'm grateful for all scientific discussion we had and for giving me his inestimable advice and valuable guidance during different cycles of my studies M.Sc and Dr.Sc. I have really learned a lot from his comments and suggestions.

I would like to thank ***Professor Abdelhamid BENHAYA*** from the University of Batna-2- for being president of the examination committee. I thank my oral thesis committee members, ***Professor Ramdane MAHAMDI*** from University of Batna -2- , ***Professor Abdesselam HOCINI*** and ***Dr. Djamel KHEDROUCHE*** from University of M'Sila, and ***Dr. Djamil RECHEM*** from University of Oum El Bouaghi, for accepting, taking time to serve as committee members, to review my dissertation and give valuable comments..

I am really grateful to **all** my lab members and colleagues Dr. T. BENTRCIA, Mr. H. FERHATI and Mr. A. AOUF for their advice and their willingness to share their bright thoughts with me, for shaping up my research.

Finally, I would like to take this opportunity to thank **all** my friends and colleagues and the staff at the Department of Electronics, University of Batna -2- who have given their support and helped **me in completing this work.**

If I did not mention someone's name here, it does not mean that I do not acknowledge your support and help. Again, I would like to thank **everyone** who supported and helped me during my Ph.D. study.

Elasaad CHEBAKI

Abstract

The downscaling of the transistor dimensions was the main and the most important factor leading to improvements in integrated-circuit performance and cost, which contributes to the rapid development of the semiconductor industry. In this dissertation, firstly we propose a new design of Double Gate Junctionless (DGJL) MOSFET based on both gate material engineering and highly doped of drain/source extensions. Analytical models associated to the drain current, analog and radio-frequency (RF) performance parameters are developed incorporating the impact of dual-material gate engineering and two highly doped extension regions on the analog/RF performance of DGJL MOSFET. The transistor performance figures-of-merit (FOM), governing the analog/RF behavior, is also analyzed. The study findings concerning the analog/RF performance are discussed and compared between the proposed design and a conventional DGJL MOSFET of similar dimensions, where the proposed device shows excellent ability in improving the analog/RF performance and provides higher drain current and improved figures-of-merit as compared to the conventional DGJL MOSFET. The obtained results are validated against the data obtained from TCAD software for a wide range of design parameters. Moreover, the developed analytical models are used as a mono-objective function to optimize the device analog/RF performance using Genetic Algorithms (GAs). In comparison with the reported numerical data for Inversion-Mode (IM) DG MOSFET, our optimized performance metrics for JL device exhibits enhancement over the reported data for IM device at the same channel length. This dissertation also focuses on the immunity behavior of the junctionless DG MOSFET device against the hot carrier degradation effect. As a result, we demonstrate that the junctionless DG MOSFET can be a viable option to enhance the immunity performances of nanoscale CMOS-based devices technology for nanoelectronics digital applications.

Keywords: Modeling, Optimization, Multigate, Double Gate, Analog, Radio Frequency, Nanoscale, Dual Material Gate, Genetic algorithm.

Résumé

La miniaturisation des dimensions du transistor était le facteur principal et le plus important menant aux améliorations des performances et du coût du circuit intégré contribuant au développement rapide de l'industrie des semi-conducteurs. Dans cette thèse, nous proposons tout d'abord une nouvelle structure MOSFET à double grille sans jonction (DGJL) basée à la fois sur la grille double matériaux et les extensions fortement dopées liées aux drain et source. Des modèles analytiques associés au courant de drain, aux paramètres de performance analogique et radiofréquence (RF) sont développés en incorporant l'impact d'une grille à deux matériaux et deux régions d'extension fortement dopées sur les performances analogique/RF du MOSFET DGJL. Les facteurs de mérite (FOM) du transistor, qui régissent le comportement analogique/RF, sont également analysées. Les résultats de notre étude concernant les performances analogique/RF pour la structure proposée sont discutés et comparés avec ceux d'un MOSFET DGJL conventionnel de dimensions similaires, où le dispositif proposé présente une excellente capacité à améliorer ces performances, et fournit un courant de drain plus élevé. Les résultats délivrés sont validés par rapport aux données obtenues à partir du logiciel TCAD pour une large gamme de paramètres de conception. De plus, les modèles analytiques développés ont été adoptés comme une fonction objectif pour optimiser les performances analogique/RF du dispositif en utilisant les Algorithmes Génétiques (AGs). En comparaison avec les données numériques rapportées pour la structure MOSFET en mode d'Inversion (IM), nos paramètres de performance optimisés pour le dispositif JL présentent une amélioration en comparaison avec le dispositif en mode d'inversion. Cette thèse s'occupe également de l'immunité du dispositif DG MOSFET sans jonctions envers l'effet de dégradation initié par les porteurs chauds. En conséquence, nous avons démontré que le DG MOSFET sans jonctions peut être un choix fiable pour améliorer les performances relatives aux transistors MOSFET à l'échelle nanométrique pour les applications numériques.

Mots clés : Modélisation, Optimisation, Grilles Multiples, Double Grille, Analogique, Radio Fréquence, Echelle nanométrique, Grille double matériaux, Algorithme génétique.

ملخص

إن محاولة تقليص حجم أبعاد الترانزستور هي العامل الرئيس والأهم الذي يؤدي إلى التحسين في أداء الدوائر المدمجة و تخفيض تكلفتها، الأمر الذي يساهم في التطور السريع لصناعة أشباه الموصلات (أنصاف النواقل) . في هذه الأطروحة، أولا نقترح تصميم ا جديدا لترانزستور ثنائي البوابة بدون وصلات مكون على أساس كل من بوابة ثنائية المعادن و تشويب عالي لكل من امتدادي المنبع و المصب. كما تم تطوير نماذج تحليلية خاصة بتيار منبع الترانزستور، و أيضا تم تحسين معايير أداء الترانزستور في كل من مجالي الترددات اللاسلكية و الإشارات التناظرية مع دمج تأثير كل من البوابة ثنائية المعادن و امتدادي المنبع و المصب ذات التشويب العالي. كما تم تحليل معايير الأداء الأكثر تأثيرا للترانزستور فيما يخص سلوكه تجاه الاستعمالات التناظرية و الترددات اللاسلكية . أيضا النتائج المتحصل عليها في دراستنا في ما يخص الاستعمالات التناظرية و الترددات اللاسلكية نوقشت وتم مقارنتها بين التصميم المقترح و المعدل و بين التصميم الكلاسيكي و ذلك بأبعاد متماثلة (نفس طول القناة)، حيث أعطى الترانزستور المقترح قدرة ممتازة في مجال الاستعمالات التناظرية و الترددات اللاسلكية. تم التحقق من صحة النتائج التي تم الحصول عليها و ذلك بمقارنتها مقابل النتائج المتحصل عليها بواسطة برنامج سيلفللكو لمجموعة واسعة للتصميم و بخصائص مختلفة . وبالإضافة إلى ذلك، تم استخدام النماذج التحليلية المتحصل عليها كدوال هدف في الخوارزميات الوراثية (الجينية) و ذلك لتحسين أمثلية أداء المركب في الترددات اللاسلكية و الإشارات التناظرية بالمقارنة مع البيانات الرقمية التي تم ذكرها من أجل الترانزستور الكلاسيكي، فإن معايير الأداء (الجودة) المحسنة الخاصة بالترانزستور المقترح بدون وصلات JL أعطى نتائج أحسن و تم ذلك بالمقارنة بين النوعين من الترانزستور (الكلاسيكي و المقترح) على نفس طول القناة . ونركز في هذه الأطروحة أيضا على مناعة الترانزستور ثنائي البوابة بدون وصلات ضد تأثير ما يعرف بالشحنات الساخنة. ونتيجة لذلك، بينا أن الترانزستور ثنائي البوابة بدون وصلات المقترح يمكن أن يكون خيارا قابلا للتطبيق لتعزيز أداء الممانعة من تكنولوجيا الأجهزة القائمة و المستعملة في النانو إلكترونيك و التطبيقات الرقمية في السلم النانومتري.

كلمات المفاتيح: النمذجة، الأمثلية، متعدد البوابات، ثنائي البوابة، الإشارات التناظرية (التماثلية)، تردد لاسلكي، سلم نانومتري، بوابة ثنائية المعادن، الخوارزمية الجينية.

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Related publications work

Published Journal Papers

1. E. Chebaki, F. Djeffal, and T. Bentrcia, *'Two-dimensional numerical analysis of nanoscale junctionless and conventional Double Gate MOSFETs including the effect of interfacial traps,'* Phys. Status Solidi C, vol. 9, pp. 2041–2044, 2012.

2. T. Bentrcia, F. Djeffal, E. Chebaki, D. Arar, *'Impact of the drain and source extensions on nanoscale double-gate junctionless MOSFET analog and RF performances,'* Mater. Sci. Semicond. Process. vol.42, pp. 264-267, 2016.

3. E. Chebaki, F. Djeffal, H. Ferhati, and T. Bentrcia, *'Improved analog/RF performance of double gate junctionless MOSFET using both gate material engineering and drain/source extensions,'* Superlattices and Microstructures, vol. 92, pp. 80–91, 2016

4. T. Bentrcia, F. Djeffal, E. Chebaki, *'Approach for designing and modelling of nanoscale DG MOSFET devices using Kriging metamodelling technique,'* IET Circuits, Devices and Systems, vol. 11, no. 6, pp. 618-623, 2017.

5. T. Bentrcia, F. Djeffal, D. Arar, E. Chebaki, *'Improved Reliability Performance of Junctionless Nanoscale DG MOSFET with Graded Channel Doping Engineering,'* Phys. Status Solidi C, Vol. 14, no. 10, October 2017.

Conference Proceedings

1. T. Bentrcia, F. Djeffal, E. Chebaki, '*ANFIS-based approach to study the subthreshold swing behavior for nanoscale DG MOSFETs including the interface trap effect,'* Proceedings of the International Conference on Microelectronics, ICM, 2012.

2. T. Bentrcia, F. Djeffal, E. Chebaki, D. Arar '*A Kriging framework for the efficient exploitation of the nanoscale junctioless DG MOSFETs including source/drain extensions and hot carrier effect,'* Materials Today: Proceedings 4 (2017) 6804–6813.

3. E. Chebaki, F. Djeffal, T. Bentrcia, *'ANFIS-based Approach to Predict the Degradation-related Ageing of Junctionless GAA MOSFET'*, To appear in Materials Today: Proceedings.

Book-chapter

1. T. Bentrcia, F. Djeffal, E. Chebaki, Advenced Materials Series, *"Intelligent Nanomaterials",* 2nd edition, Chapter 12 ***'Multi-objective Design of Nanoscale Double Gate MOSFET Devices Using Surrogate Modeling and Global Optimization',*** pp. 395-425, (Wiley-Scrivener Publishing, 2017).

Introduction:

Introduction and Layout of the Thesis

Introduction

Since the invention of the first transistor in 1947, and that of the integrated circuit in 1958 by Jack Kilby, the progress of microelectronics has been considerable, both in terms of improving performance and increasing the complexity of the circuits leading to the decline in production costs [1]. The integration capacity in microelectronics follows an exponential evolution, with a density of microprocessor transistors doubled every 3 years [2]. This evolution, known as Moore's law [3,4], led to the fabrication of microprocessors of more than 1.9 billion transistors, and the realization of memories, whose density exceeds 1.3 Tb per square inch. Increasing the integration density and improving performance are made possible by decreasing (known also as downscaling or miniaturizing) the size of the transistors. The characteristic quantity of a transistor that distinguishes one generation of transistors from the next is the gate length. The International Technology Roadmap for Semiconductors (ITRS) [5] predicts that the channel length will attend the sub 10 nm region by the year 2018. The miniaturization of semiconductor devices is approaching fundamental physical limits. Indeed, the constant progression of CMOS components (complementary metal-oxide-semiconductor), established by the famous law of Moore, has always been respected, whether in terms of power, speed or size of the components [6]. So far, this approach has been very successful, but it is now reaching its limits. Today, transistors are approaching the ultimate physical limits, and performance is limited by the effects of leaks and those associated with reduced channel length. Three-dimensional devices are being exploited to take over the planar components, thanks to the better control that they allow for effects related to short channels [7].

Several remedy solutions have emerged to deal with the main problem of the miniaturization being the direct dependence of the electrical characteristics with respect to the controllable physical parameters. This causes many parasitic effects that change the performance and power consumption of the systems.

The electrical characterization of a device is of great importance and requires particular attention in the development of advanced Metal Oxide Semiconductor Field Effect Transistor($MOSFET$) based technologies. To do that, there are a huge number of techniques and parameters which can be crucial to develop the MOSFET and alleviate the effects related to short channel. Among these techniques, we can mention: (i) The choice of channel (length, thickness, profile doping, cross section shape, …), (ii) semiconductor (Si, Ge, GaAs,…), (iii) gate (number, shape, metal, polysilicon, gate engineering,

overlap,…), (iv) gate oxide (thickness, SiO_2, High-k, …), (v) substrate doping (uniform, linear, Gaussian, …) and (vi) Source/Drain technology. All these techniques and parameters can largely determine the performance of the device. In designing smaller devices, the impact of the miniaturization on the reliability of the integrated circuits should also be taken into consideration.

However, after almost thirty years of frantic race to reduce the size of electronic components, the problems are not limited to the difficulties of realization. We are now seeing phenomena of a theoretical nature regarding the advantages offered by Complementary MOS ($CMOS$) technology. Among these phenomena, we have in particular the Drain Induced Barrier Lowering ($DIBL$), the short channel effects ($SCEs$), the quantum mechanical confinement, the gate tunneling current, the random fluctuation of the dopants. To overcome these difficulties, one of the solutions consisting in modifying the architecture of the components, in particular the increase of the number of gates in order to have a better control of the current-flow, seems a solution of choice for the future of microelectronics. But these devices, to be used by the designers of integrated circuits, need to be modeled in the form of compact models interpretable by circuit simulators. These compact models must be able to describe as precisely as possible the electrical behavior of the considered devices. The simulation of microelectronic components therefore requires new theories and modeling techniques such as artificial intelligence and soft computing techniques that improve the physical understanding of micro and nano devices.

The field of modeling, optimization, and simulation of microelectronic and nanoelectronic components can be considered as an important field of applications of artificial intelligence and soft computing techniques. Therefore, the study of the possibility of using artificial neural networks and soft computing techniques in the field of microelectronics, especially in the form of predictors and simulators of nanoscale components (Double Gate $MOSFET$, Trigate $MOSFET$, Gate All Around $MOSFET$, ...) is necessary. In this sense, both artificial intelligence and soft computing techniques are seen as an additional tool in the hands of the engineer and the researcher, rather than a substitute for more conventional methods. These tools are likely to provide answers where the analytical procedures show their limits.

Layout of the Thesis

Our dissertation work has twofold essential goals, the first one is to present the principles of soft computing techniques and their applications in the field of modeling, optimization, and simulation of nanoscale electronic components, and the second is to propose new design structures of multigate $MOSFETs$ to study their electrical performances for analog and RF applications. To make the work clear and comprehensible, our dissertation is structured in five chapters: The first chapter presents briefly the bulk MOS transistor and the problems caused by its miniaturization, then discusses the possible technological solutions to resolve these problems, thus exposes the SOI technology with its emerging solutions and details the main electrical characteristics of both multi gate transistors Double Gate DG (MOS transistor), and Gate All Around GAA (MOS transistor). The second chapter is devoted to soft computing techniques: it gives the principles of the four major techniques used in soft computing and in this dissertation namely Fuzzy Logic (FL), Artificial Neural Network (ANN), Genetic Algorithm (GA) and a hybrid soft computing which is Adaptive Neuro-Fuzzy Inference System $(ANFIS)$.

In the third chapter, we propose a new Double Gate Junctionless $(DGJL)$ $MOSFET$ design based on both gate material engineering and highly doped drain/source extensions. Analytical models for the long channel device associated to the drain current, analog and radio-frequency(RF) performance parameters are developed incorporating the impact of dual-material gate engineering and two highly doped extension regions on the $analog/RF$ performance of $DGJL$ $MOSFET$. The transistor performance figures-of-merit (FoM), governing the analog/RF behavior, have also been analyzed. The $analog/RF$ performance is compared for the proposed design and a conventional $DGJL$ $MOSFET$ of similar dimensions, where the proposed device shows excellent ability in improving the $analog/RF$ performance and provides higher drain current and improved figures-of-merit with respect to the conventional $DGJL$ $MOSFET$. Moreover, the developed analytical models are aggregated to form a mono-objective function in order to optimize the device $analog/RF$ performance using Genetic Algorithms (GAs). In comparison with the reported numerical data for Inversion-Mode (IM) DG $MOSFET$, our optimized performance metrics for JL device exhibit enhancement over the reported data for IM device for the same channel length. Chappter IV is divided into two main parts: Part 1 deals with the immunity behavior of the junctionless DG $MOSFET$ device against the hot

carrier degradation effect and we demonstrate that the junctionless $DG\ MOSFET$ can be a viable option to enhance the immunity performances of nanoscale CMOS-based devices technology for nanoelectronics digital applications. In part 2, using the developed model of the Junctionless $DG\ MOSFET$ in chaper III, and in order to analyze the characteristics and circuit performance of the device, we have adopted mixed mode simulation under ATLAS-2D environment for the implementation of the inverter circuit. Based on the numerical outcomes, satisfactory results are recorded in comparison with the conventional junctionless structure. The last chapter covers the applicability and the efficiency of adaptive neuro-fuzzy inference system ($ANFIS$) approach as a predictor of junctionless gate all around (JL-GAA) $MOSFET$ device lifetime. Our predictions are compared versus the numerical results obtained by ATLAS simulator, where a good agreement is obtained.

Finally, we conclude this dissertation and give an overview of perspectives that can be developed to better understand this subject and also can be used in our future research.

Chapter I: MOSFET Transistor: miniaturization limits and solutions

I.1 Introduction

It was in 1960 that Kahng and Attala introduced the first silicon MOS transistor using an insulated gate whose gate dielectric was silicon oxide SiO_2. Silicon was a very wise choice. It is the most abundant element of the earth's crust, after oxygen. In addition, its oxide is not only a very good electrical insulator, but it has also proved perfectly suitable for forming so-called passivation layers protecting the circuits, remarkably increasing their reliability.

MOS transistors on Silicon, simpler and cheaper than their bipolar competitors, but intrinsically less efficient with equivalent technological generation, flourished in the 70s and 80s due to the $CMOS$ technology invented in 1968 which consumes a very small amount of energy. Since then, not only the applications in $CMOS$ logic but also the memories that constitute the other major application of $MOSFETs$ have benefited from a very strong and continuous increase in their speed and their integration density.

In 1967, Dennard invented Dynamic Random Access Memory ($DRAM$) by combining a $MOSFET$ transistor and a storage capacity. The year 1971 was the year of the design of the first microprocessor by Hoof et al of the company Intel. It is a $4-bit$ processor ($Intel$ 4004) $3mm$ by $4mm$ with 2250 transistors and was manufactured with Intel's 10µm PMOS technology [8]. The die map of the Intel 4004 processor and Intel Core i9 − 7980XE processor are illustrated in Figure I.1a and Figure I.1b, respectively.

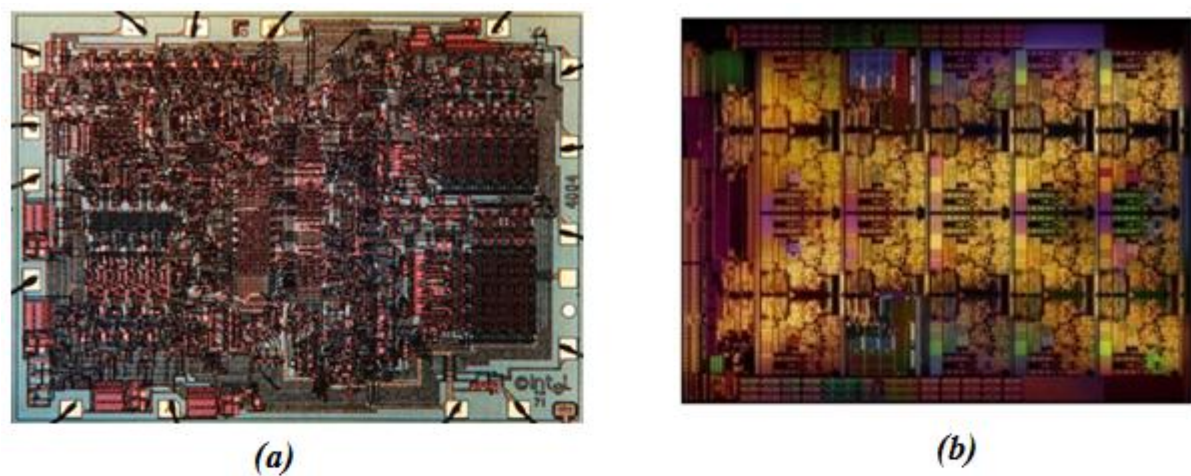

Figure I.1: Illustration of the die map of: (a) Intel 4004 processor (b) Intel Core i9 − 7980XE processor [8].

Since then, many other new technologies have allowed, without really changing the manufacturing methods to reduce the size of the transistors and thus the density of the memories and the power of the microprocessors.

Till 2011, Intel for the first time used a new manufacturing process, which is the 3 dimensions (3D) mixed with multi-gate (tri-gate) designs instead of the planar manufacturing to produce the 22 nm tri-gate 3D transistor. This race for miniaturization using 3D manufacturing allows today to design transistors with 3D tri-gate and a length of 14 nm. This makes it possible to design processors such as the $Core\ i9$, as illustrated in Figure I.1b [8] which shows the $Intel\ Core\ i9-7980XE$ processor die map.

I.2 Description of the MOS transistor

I.2.1 Structure of the MOS transistor

Before presenting the equations allowing the calculation of the drain current of the MOS transistor, it is necessary to define the different used notations [9].

The N-channel MOS transistor ($or\ MOSFET$ for Metal Oxide Semiconductor Field Effect Transistor) is a quadrupole device consisting of a conductive layer (metal or highly doped polysilicon) called a gate electrode (G), a source (S), a drain (D) and a semiconductor substrate (B) on which we locate a thin layer of insulating oxide (SiO_2) of thickness t_{ox}. This is illustrated in Figure I.2.

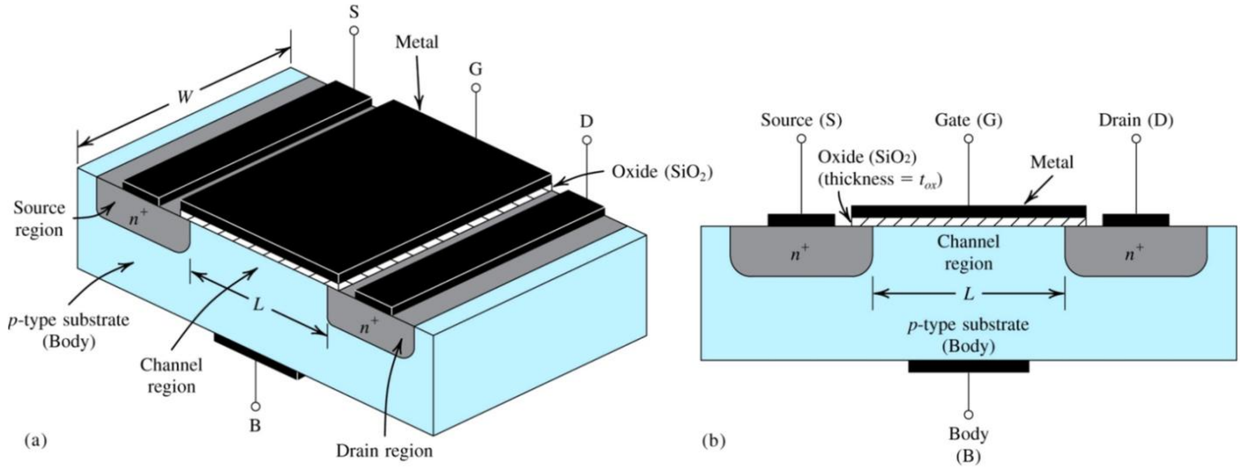

Figure I.2: N-type MOS transistor: (a) perspective view, (b) cross-section.

The length of the transistor, denoted L, corresponds to the length of its gate (slightly overlaps the source and drain regions) and its width is denoted W. The region between the

source and drain junctions is called the channel region and is defined by its length L and its width W. We will consider later a surface channel transistor, that is to say whose conduction is provided by the minority carriers of the substrate (electrons in the case of $nMOSFET$), at the interface between the gate dielectric and the substrate.

Note that the $MOSFET$ has two additional electrodes with respect to the MOS capacitance, which consist of two n^+ doped caissons for an $nMOS$. Thus, many properties of the MOS transistor derive from those of the MOS capacitor.

I.2.2 Principles operating regimes

The operating principle of the MOS transistor ($or\ MOSFET$) is based on the modulation of a carrier density of a semiconductor zone by an electric field perpendicular thereto. This electric field is applied by the control electrode (the gate) through an insulator (gate dielectric). The carriers created are mobile charges: electrons in the case of $nMOS$ transistor, holes in the case of $pMOS$ transistor. When the applied voltage to the gate V_g is greater than a threshold voltage denoted V_t, these mobile charges constitute a conduction channel between the source and the drain. When a potential difference V_{ds} is applied between the source and the drain, the abundant carriers (source side, conventionally) are collected by the drain in the form of a current. We speak of $nMOS$ transistor when the substrate is doped with acceptor type atoms and the minority carriers are the electrons. In this case, the source and drain regions are heavily doped with donor-type atoms (conduction provided by electrons). In contrast, $pMOS$ transistor has a substrate doped with donor atoms and the minority carriers are the holes. Thus, macroscopically, the MOS transistor behaves as a device regulating the current between two electrodes by a voltage control.

Remembering that there are three particular regions namely accumulation, depletion, and inversion and two transition points values of the V_g voltage, which are flat-band voltage V_{fb} and threshold voltage V_t as illustrated in Figure I.3 for the n-type $MOSFET$ device.

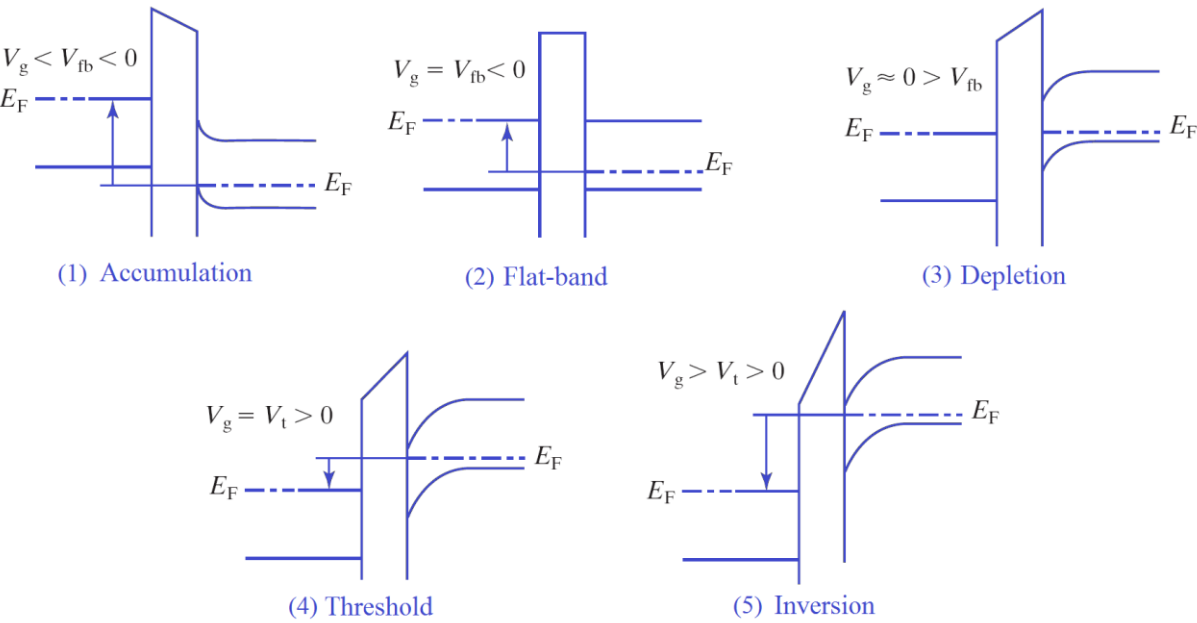

Figure I.3: Energy band diagrams of an n-type MOS transistor [10].

Notice that downward arrows indicate positive V_g whereas upward arrows present negative V_g.

The flat-band voltage is given by:

$$V_{fb} = \psi_g - \psi_S - \left(\frac{Q_{ox}}{C_{ox}}\right) \tag{I.1}$$

where ψ_g and ψ_S are the gate and the substrate work functions respectively and Q_{ox} is the charge at the $Si - SiO_2$ interface. The gate voltage in excess of V_{fb} is divided between the substrate, the oxide and the poly-gate depletion layer.

$$V_g = V_{fb} + \phi_S + V_{ox} + \phi_{poly} \tag{I.2}$$

$$V_g = V_{fb} + \phi_S - \frac{Q_{sub}}{C_{ox}} + \phi_{poly} \tag{I.3}$$

where ϕ_S is the surface potential, or the substrate band bending and V_{ox} is the oxide voltage. The quantity $Q_{sub}\,(C/cm^2)$ is the sum of the accumulation, inversion, and depletion-layer charges.

At the threshold of inversion, ϕ_S and V_t are expressed in terms of ϕ_B and V_{fb} respectively

$$\phi_{St} = \pm 2\phi_B \tag{I.4}$$

$$\phi_B = \frac{kT}{q}\ln\left(\frac{N_{sub}}{n_i}\right) \tag{I.5}$$

$$V_t = V_{fb} + \phi_{St} \pm \frac{\sqrt{q\, N_{sub}\, 2\, \varepsilon_s / \phi_{st}}}{C_{ox}} \quad \text{(I.6)}$$

The important parameters of the transistor are given below:

- The threshold voltage V_t is the gate voltage needed to form a conduction channel (inverting layer) between the source and the drain. The typical threshold voltage of a nano MOSFET is less than 0.4 V.
- The transconductance or gain g_m is defined by:

$$g_m = \left(\frac{\partial I_{ds}}{\partial V_{gs}}\right)_{V_{ds}=cte} \quad \text{(I.7)}$$

and must be as high as possible. The transconductance increases very rapidly when the channel length becomes less than 100 nm.

- The output conductance (g_{ds}) is given by:

$$g_{ds} = \left(\frac{\partial I_{ds}}{\partial V_{ds}}\right)_{V_{gs}=cte} \quad \text{(I.8)}$$

- The subthreshold slope (SS): it represents the gate voltage to be applied (under the threshold voltage value) to increase the drain current by one decade:

$$SS = dV_{gs}/d(log\ I_{ds}) \quad \text{(I.9)}$$

I.2.2.1 Linear operating regime

The total current near the $Si - SiO_2$ interface is the sum of the diffusion and drift currents of the free carriers. In inversion, we consider that the majority concentration is zero in the channel and we can write [11]:

$$\vec{J}(x, y) = q\left(\mu_n n \vec{\xi} + D_n \vec{\nabla} n\right) = \vec{J}_n \quad \text{(I.10)}$$

where μ_n is the mobility of the electrons in a weak field in the inversion layer, D_n the electron diffusion coefficient and $\vec{\nabla}_n$ the concentration gradient. If we consider Shockley's gradual approximation [12], i.e when the transistor is operating in unsaturated mode or when the channel is not pinched, we consider that the field lines are parallel to the interface, (I.10) becomes:

$$J_n = \underbrace{q\mu_n n\xi_x}_{J_1} + \underbrace{qD_n grad_x n}_{J_2} \tag{I.11}$$

with ξ_x being the field along the x axis (Figure I.3), j_1 is the drift component (due to the electric field) and j_2 represents the diffusion current.

Considering the Einstein coefficient $D_n = \mu_n \frac{kT}{q}$ where μ_n is the mobility of the electrons supposed constant, and knowing that ξ_x derives from a scalar potential expressed by:

$\xi_x = -grad(\phi_c)$), the equation (I.11) can be simplified to [11]:

$$J_n = -q\mu_n n \frac{d\phi_c}{dx} \tag{I.12}$$

where the potential relationships are given by:

$$\phi_c(x=0) = -V_{BS}$$
$$\phi_c(x=L_G) = V_{DS} - V_{BS}$$
$$\phi_c(0 < x < L_G) = V(x) - V_{BS}$$

The total current is obtained by integrating the density J_n over the entire thickness of the inverting layer y_i of the transistor of width W_G:

$$I_{DS} = -W_G \int_{y_i}^{0} J_n dy = W_G \int_{y_i}^{0} q\mu_n n \frac{d\phi_c}{dx} dy = W_G \mu_n \frac{d\phi_c}{dx} \int_{y_i}^{0} ndy \tag{I.13}$$

Moreover, since I_{DS} being constant all along the channel, it comes that:

$$\int_{L_G}^{0} I_{DS} dx = I_{DS} L_G = -W_G \mu_n \int_{-V_{BS}}^{V_{DS}-V_{BS}} Q_n d\phi_c \tag{I.14}$$

where $Q_n = \int_{y_i}^{0} ndy$.

On the other hand, the influence of V_{BS} being identical at all points of the channel on the free carrier concentrations, the equation (I.14) can be rewritten:

$$I_{DS} = -\frac{\mu_n W}{L_G} \int_{0}^{V_{DS}} Q_n(V) dV = -\frac{\mu_n W}{L_G} \int_{0}^{V_{DS}} (Q_{SC} - Q_D)(V) dV \tag{I.15}$$

The charge Q_{SC} can be considered as the total charge of the semiconductor to which the Q_D charge of the depleted area under the inversion zone must be subtracted.

$$Q_{SC} = C_{OX}\left(V_{GS} - \phi_c - \phi_{ms} + \frac{Q_{OX}}{C_{OX}} - 2\phi_F\right) \tag{I.16}$$

$$Q_D = -\sqrt{2N_A\varepsilon_{Si}\left(\phi_c - V_{BS} + 2\phi_F\right)} \tag{I.17}$$

To obtain the expression of I_{DS}, it is necessary to substitute equations (I.16) and (I.17) in equation (I.15), the current I_{DS} is then rewritten in the simplified form:

$$I_{DS} = \frac{W_G}{L_G}\mu_n C_{OX} V_{DS}\left[V_{GS} - \underbrace{V_{FB} - 2\phi_F - \gamma\left(-V_{BS} + 2\phi_F\right)^{1/2}}_{V_{th}} - V_{DS}\frac{1}{2}\underbrace{\left(1 + \frac{\gamma}{2}\left(-V_{BS} + 2\phi_F\right)^{-1/2}\right)}_{\alpha}\right] \tag{I.18}$$

which makes it possible to express the drain current of a MOS transistor in linear mode in the following form:

$$I_{DS} = \frac{W_G}{L_G}\mu_n C_{OX}\left[V_{GS} - V_{th} - \frac{\alpha}{2}V_{DS}\right]V_{DS} \tag{I.19}$$

I.2.2.2 Saturation operating regime

As the drain voltage increases, the depletion width expands and reduces the inversion charge at the edge of the drain. The transistor goes into saturation mode when V_{DS} is large enough that Q_{inv} $(x = L_{eff})$ is almost zero. This occurs for V_D equals to V_{Dsat}. Then, we have:

$$V_{Dsat} = \frac{V_{GS} - V_T}{\alpha} \tag{I.20}$$

There is another approach to determine the saturation drain voltage. It is enough to consider that for $V_{DS} > V_{Dsat}$ the drain current does not vary anymore (ideal case), which leads to solve:

$$G_d = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{DS_{sat}}} \tag{I.21}$$

This allows finding the expression of I_{DSsat}:

$$I_{DS_{sat}} = \frac{W_G}{L_G} \mu_n C_{OX} \frac{(V_{GS} - V_T)^2}{2\alpha} \quad \text{(I.22)}$$

Figures I.4a, I.4b, I.5a and I.5b [13] show the calculated $I_{DS}(V_{GS})$ and $I_{DS}(V_{DS})$ characteristics (using equations (I.19) and (I.22)) and measured for a long-channel transistor (W_G / L_G = 10/10µm) and a short-channel transistor (W_G / L_G = 10/0.13µm). There can be a discrepancy between the model and the measurement when the gate and the drain voltages increase. On small geometries, the gap is accentuated, which highlights the need to refine the equations including the effects related to the reduction of the dimensions of the MOSFET transistors. In the next section, we will present these effects, starting from their physical origins, to arrive at a mathematical quantification allowing including their impacts on the electrical behavior of the devices. We will in particular describe the reduction of the carrier mobility in the channel under the influence of the electric field, the modulation of the channel length related to the extension of the depletion width of the Drain-Substrate junction.

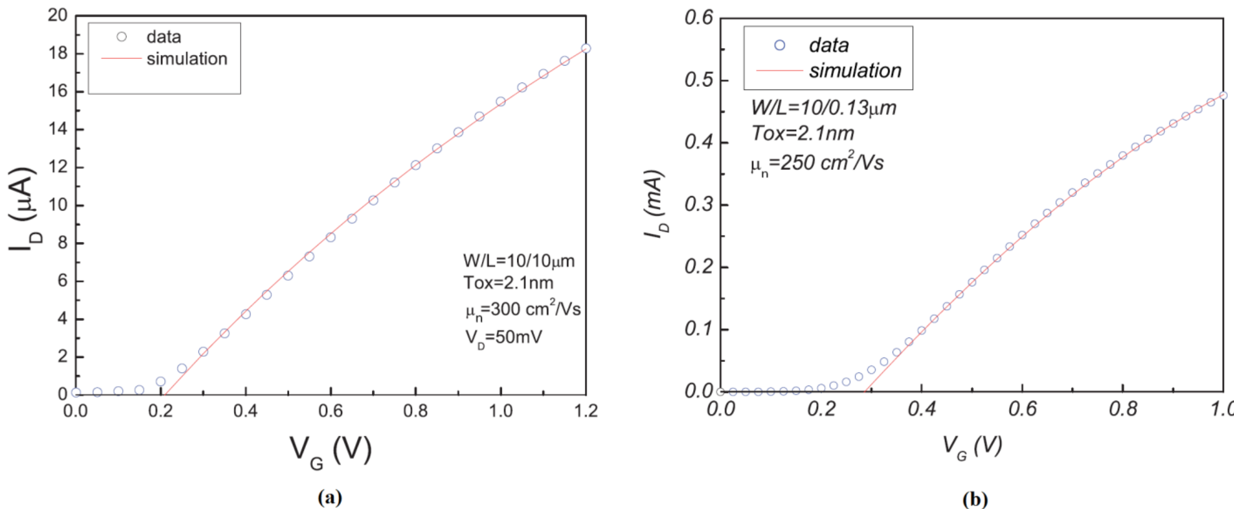

Figure I.4: Comparison between modeling and measurement of linear drain current for a MOS transistor with ultra thin oxide T_{ox} = 2.1nm (a) MOS with long N- type channel (W_{eff}/L_{eff} = 10/10µm) and (b) MOS with short N- type channel (W_{eff}/L_{eff} = 10/0.13µm) [13].

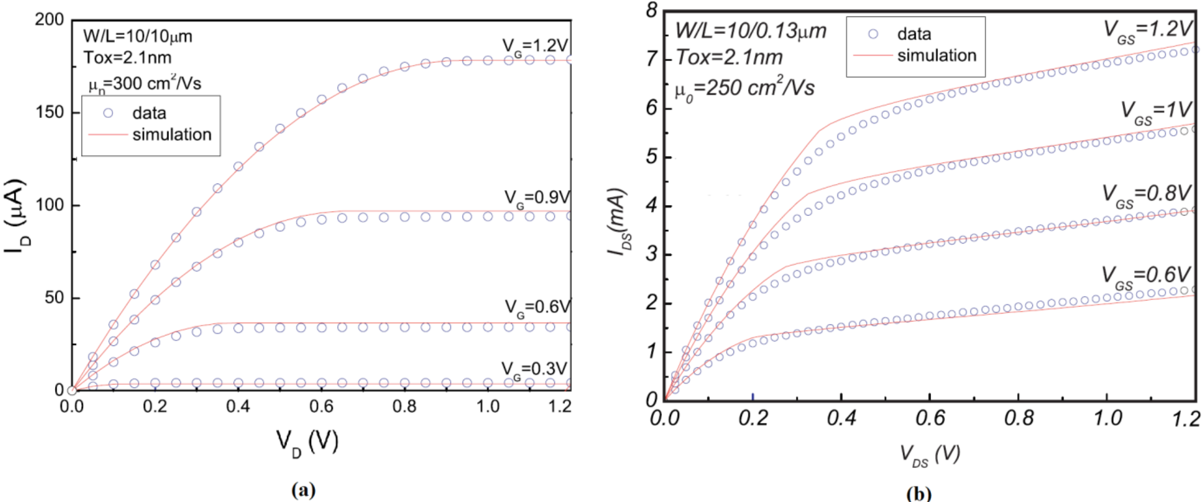

Figure I.5: Comparison between modeling and drain current measurement vs. drain voltage for different gate voltage values for a MOS transistor with ultra thin oxide T_{ox} = 2.1nm (a)MOS with long N- type channel (W_{eff}/L_{eff} = 10/10µm) and (b) MOS with short N- type channel (W_{eff}/L_{eff} = 10/0.13µm) [13]

I.3 Presentation of SOI technology

I.3.1 SOI technology with a single gate

In SOI (*Silicon On Insulator*) technology, unlike the bulk MOSFET (Figure I.6a) where the components are made on a silicon substrate - sometimes called *bulk* - with a thickness of the order of 600 µm of which only the first microns on the surface are really useful, the SOI is realized on a Silicon film previously placed on a buried oxide layer (Figure I.6b) [14]. The silicon film has a thickness noted by t_{Si} .

In an opposite manner of the bulk MOS transistor for which the inversion channel is located at the silicon-oxide interface, the SOI structure gave rise to the concept of volume inversion [15]. The presence of the buried oxide allows a better control of the potential in the channel by the gate compared to the MOS transistor on silicon.

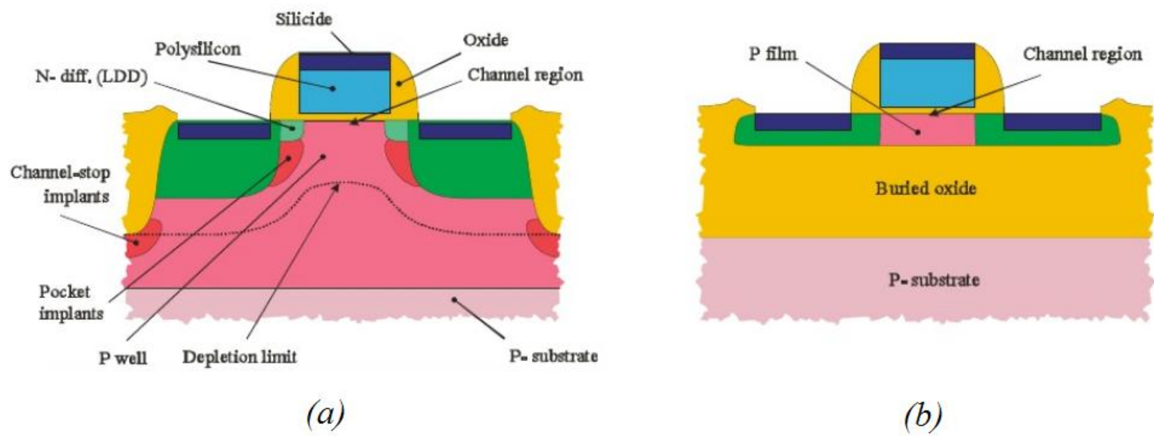

Figure I.6: Cross-section Schematic view of MOS transistors (a) bulk and (b) SOI.

For thick silicon films, the depletion zone in the film does not reach the buried oxide; we then speak of the partially depleted transistor (or PDSOI). When the thickness of the film is reduced and the depletion reaches the buried oxide, the film is completely depleted and the gate improves the control of the potential in the film; we are talking about a fully depleted transistor (or FDSOI). Figure I.7 describes these two structures.

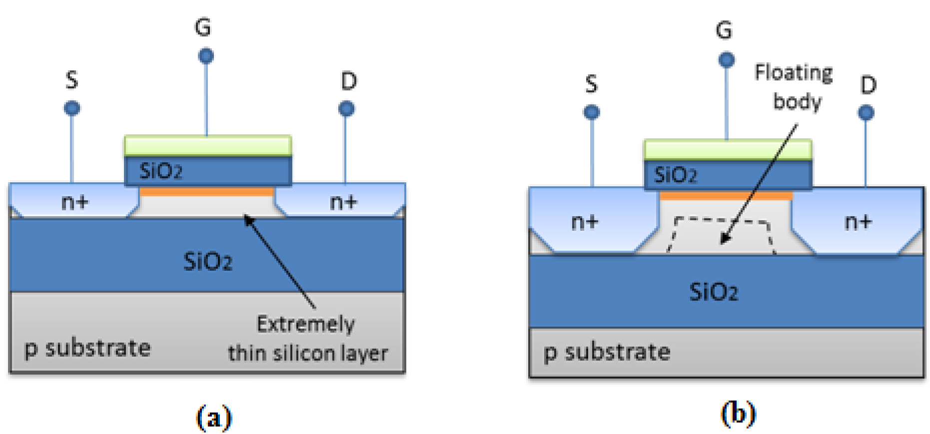

Figure I.7: Schematic representation of a SOI transistor: (a) fully depleted and (b) partially depleted.

The fact that the SOI is partially or fully depleted depends essentially on the extension of the depleted layer in the silicon film. The depth x_{Si} of the depletion zone in the film will depend on the doping of the film [16].

I.3.1.1 Advantages of SOI compared to bulk MOSFET

The electrical properties of this structure, in particular, the completely depleted SOI transistor, are in general much better compared to the bulk MOS transistor [17]. It is also

considered that this component is a potential candidate to successfully integrate devices of longitudinal dimensions less than or equal to 30 nm [17]. We will now see the main properties of the SOI technology compared to the bulk MOSFET.

The advantages of SOI technology are multiple including:

Decrease of parasitic effects

- ✓ Just by the presence of buried oxide, parasitic capacitances are considerably reduced.
- ✓ The source-substrate and drain-substrate junction capacitances, which correspond to the capacity of a reverse-biased junction for the bulk MOSFET, are actually present by a unique oxide capacitor C_{Box} for the SOI MOSFET.
- ✓ The SOI transistor has, still in comparison with the bulk MOS transistor, a thinner and isolated conduction channel [17] besides a simplification of the interconnection levels above the transistors due to the absence of the boxes.
- ✓ When the silicon film is weakly doped, or even undoped, it can be completely depleted at zero gate voltage, which is also advantageous with regard to the surface leakage current.
- ✓ On the SOI (Figure I.7b), these zones are totally isolated and thus the breakdown between these two zones is very difficult.
- ✓ The ability to increase the integration density is a direct consequence of suppressing this parasitic effect [15].
- ✓ Improved gate control over the depletion charge.
- ✓ Charge separation models provide the proportion of the depletion charge controlled by the gate relative to that controlled by the source and drain.
- ✓ The ratio between the depletion charge controlled by the gate and the drain (or the source) is much greater for the SOI transistor, compared to bulk MOS transistor, with identical dimensions (L, W, t_{ox}, X_j).

This phenomenon is more pronounced as the length of the channel decreases as shown in Figure I.8.

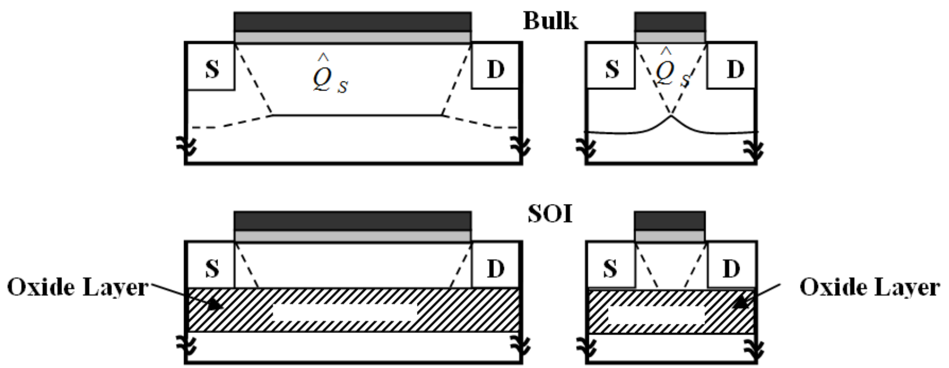

Figure I.8: Distribution of the depletion charge for bulk MOSFET and SOI [18].

Improvement of the subthreshold slope

The subthreshold slope is defined by:

$$SS = n \ln(10) \frac{kT}{q} \tag{I.23}$$

with $n = 1 + (C_{dep}/C_{ox})$ is the substrate factor.

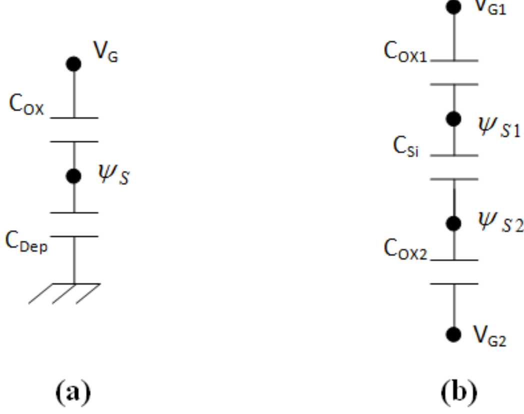

Figure I.9: Capacitive equivalent circuit (a) of a bulk MOSFET and (b) of a SOI [19].

For the bulk MOS transistor (Figure I.9a), since C_{dep} is not negligible, this implies that n> 1. On the other hand, for the SOI transistor on thin film, the entire film is depleted before the voltage reaches the threshold value and therefore C_{Si} is a constant, hence:

$$SS = \frac{nkT}{e} \ln(10) \tag{I.24}$$

where $n = \left(1 + \frac{C_{Si}}{C_{OX1}}\right) - \frac{\frac{C_{Si}}{C_{OX2}} - \frac{C_{Si}}{C_{OX1}}}{1 + \frac{C_{Si}}{C_{OX2}}}$

C_{Si} denotes the capacity of the completely depleted silicon film and C_{ox1} and C_{ox2}, the oxide capacities located respectively in the upper part and the lower part of the silicon film. In Figure I.9b, ψ_{S1} and ψ_{S2} denote the surface potentials in the upper and lower regions of the film respectively and, finally, V_{G1} and V_{G2} correspond to the gate polarizations, always in the upper region and the lower region of the film.

Usually, for thin films we have $C_{ox2} \ll C_{ox1}$ and $C_{ox2} \ll C_{Si}$, we get in this case a value of *n* close to unity and an optimal subthreshold slope. The subthreshold slope at the room temperature is practically minimal (= 60 mV / dec for *n* = 1) in SOI technology (Figure I.10).

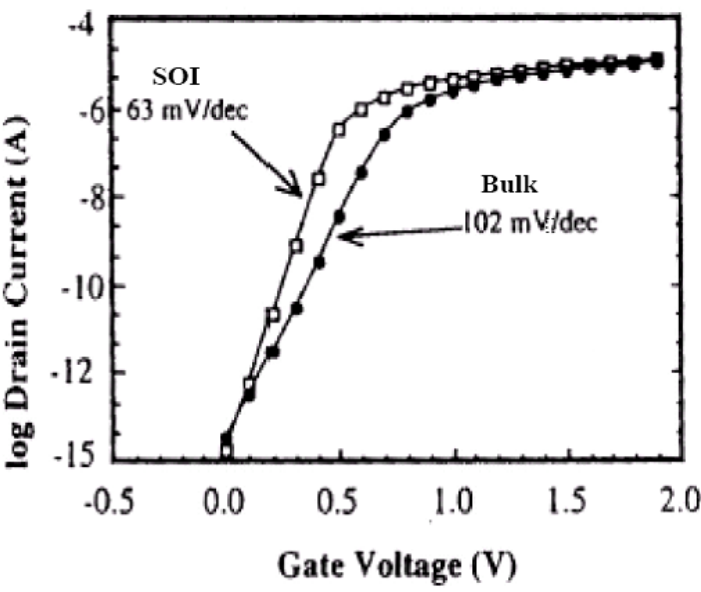

Figure I.10: Comparison of the subthreshold slope of the MOS transistor in bulk and SOI technologies, for a constant geometry [17].

I.3.1.2 Major disadvantage of SOI technology

The advantages of SOI technology are numerous. However, their major disadvantage, especially with regard to PDSOI, is the significance of the short channel effects (Figure I.11). The polarization of the drain can induce short channel effects by electrostatic influence through the buried oxide. This harmful effect becomes significant especially when the thickness of the oxide is important.

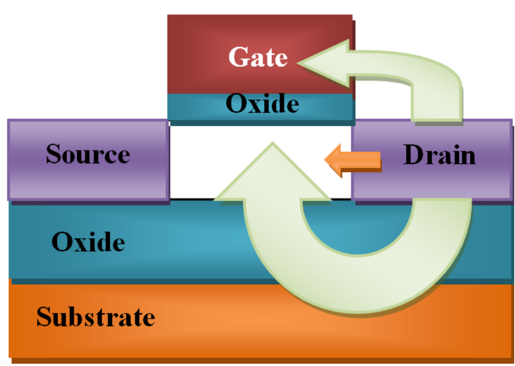

Figure I.11: Electrostatic influence on SOI with single gate [17].

Naturally, reducing the oxide thickness would only reduce the electrostatic influence; however, inserting a gate below the oxide would be a shield that allows completely blocking the field lines. This may directly protect the channel and reduce the short channel effects. Such structure is called Double-Gate (DG) and comes within the framework of multi-Gate structures to be presented in the following section.

I.3.2 Multi-gate transistors

The SOI technology with a single gate does not make it possible to reduce the short-channel effects due in particular to the electrostatic influence. However, the addition of a gate around the silicon layer not only promotes the isolation of the conduction channel and implicitly its protection, but also offers better control over this channel. As a result, SOI structures appear with two, three, or even four gates [17].

The evolution of the SOI devices with the increase of the gates number is illustrated in Figure I.12 and Figure I.13.

Depending on the number of gates controlling the channel and their positioning around the silicon film, the SOI MOSFET denomination differs. So, we find in the literature:

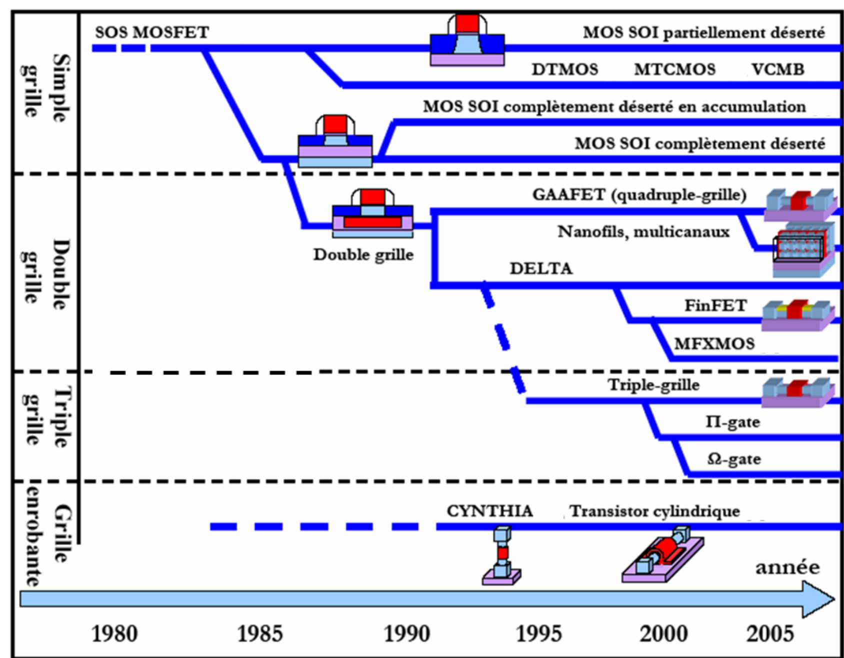

Figure I.12: Evolution of SOI technology over the years [17-18] [20].

Double-Gate structure: The double-gate MOS transistor (DG) consists of two gates placed on the horizontal plane. Figure I.13 shows the architecture in which each gate has control over the channel(s).

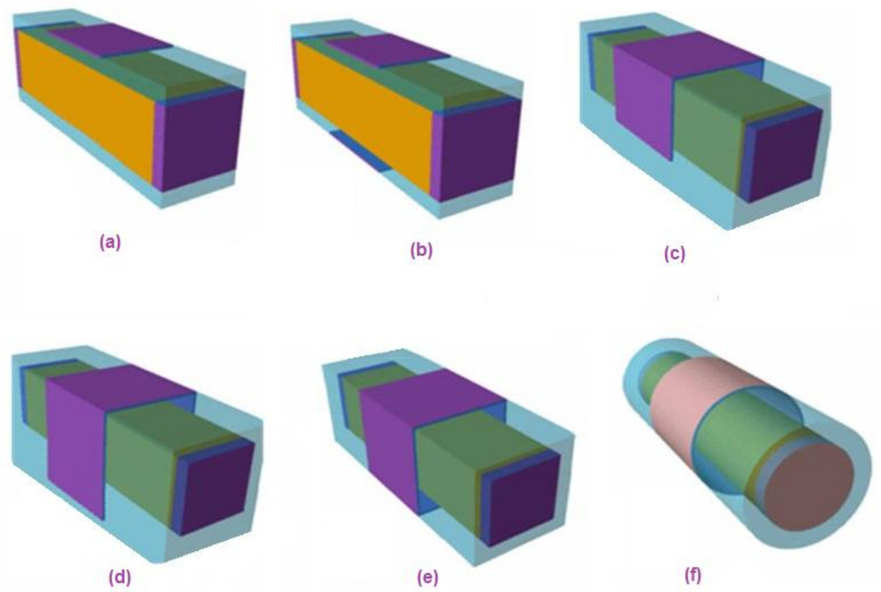

Figure I.13: Single gate versus various multi-gate structures: (a) Single-Gate SOI, (b)Double-Gate SOI, (c) Tri-Gate SOI, (d) Π Gate, (e)Quadruple-Gate SOI, (f) Surrounding-Gate SOI.

There is another structure that belongs to the Double-Gate category although it has three gates; it is often called in the literature, the FinFET. This structure has a "third gate" connecting the two other gates. Compared to a planar double-gate MOSFET device, the advantage of a FinFET transistor is the intrinsic self-alignment of the two gates. The "third gate" is on a thick gate oxide layer. As a result, it does not control the channel. Thus, only the two side gates create and control an inversion layer.

In addition, it is observed that at the level of the planar double-gate MOSFET structure, there are two variants. Depending on how the device is polarized, we can notice different operation modes. We have the dual-gate MOSFET in symmetrical operation mode and the dual-gate MOSFET in asymmetric operation mode.

Tri-Gate structure: This structure has three gates (TG), one above the oxide and one on each side (Figure I.13). The oxide layers in contact with each of the gates have a sufficiently small thickness to allow the formation of three inversion layers inside the silicon film [15].

Tri^{+}-Gate structure: These transistors are represented in Figure I.14. They consist not only of three gates positioned above the gate oxide and on the lateral faces but also of two extra extensions.

Figure I.14: Extension of the gates leading to the structures Π and Ω SOI MOSFETs.

Depending on the shape of these extensions, the architecture differs [17]. If these extensions develop vertically in the buried oxide or following the continuity of the lateral gates, we speak of ΠFET structure. If these extensions grow horizontally or perpendicularly to the side gates, we speak of ΩFET. These extensions are generally obtained by over-etching the oxide in the definition phase of the active zones. Their role is to significantly improve the electrostatic control of the gate.

Quad-Gate structure: This component has four gates (QG). The structure is described in Figure I.13. The silicon film is covered with gate on all four sides, hence they are also

known as "surrounding-gate" structures [17]. We will come back in more details on this type of devices in the following section.

I.3.2.1 Advantages of multi-gate transistors

The idea of adding more and more gates is based on the fact that, if the thickness of the active silicon film between the different gates is sufficiently small, these polarized gates can control the overall silicon volume between the source and the drain. The conduction then taking place volumetrically and not on a surface [17], we expect advantageous effects for the value of the drain current. In addition, taking control of the channel is more important, it gets rid of short channel effects related to the influence of V_{ds}: the drastic decrease in insulation thickness becomes less crucial. Lastly, by their provisions, the gates are shield signs against the lines of fields created by the polarization of the drain influencing the circulation of the electrons. Finally, the performance is significantly improved with such multi-gate architectures. For this purpose, they are currently the subject of intense research in many laboratories.

I.3.2.2 Disadvantage of multi-gate transistors

One of the disadvantages of these structures is the increase of the resistances of the source /drain extensions. In addition, the dimensions of the active zone being reduced to less than a few tens of nanometers in all directions arise many questions regarding the physics of transport in these devices: the importance of ballistic transport [21] or tunnel effect [22] between the source and drain. Finally, the key aspect that remains to be treated resides, of course, in the manufacturing process, which requires the implementation of more complex procedures.

I.4 Double-Gate MOSFET architecture

The first double-gate device was reported in 1984 by Sekigawa et al. [23]. The authors in this paper predicted that short-channel characteristics could be mended by employing a double-gate structure rather than the traditional, single-gate architecture. The fully depleted lean-channel transistor (DELTA), was the first double-gate MOSFET, fabricated in 1989 by Hisamoto et al. and contained a vertically positioned silicon film [24]. Later implementations of vertical-channel double-gate MOSFETs included FinFETs [25]. Double-Gate (DG) MOSFET is the most prevalent studied among Multi-Gate (MG) MOSFETs [26, 27]. According to the current direction and the possible orientations of

the two gates, we can distinguish three different possible topologies of DG MOSFET as illustrated in Figures I.15, which have been adopted from [28]. The planar DG MOSFET presented in Figure I.15(a) resembles the planar bulk MOSFET technology. It has less geometry effects than the other two topologies (vertical and FinFET) such as "Corner effects" [29] and "Narrow width effects" [30]. Moreover, the planar DG is free from "crystal plain orientation uncertainty" problems when directions of the devices vary. Another advantage of planar DG MOSFET is that the two gates are easy to be separately biased as the two gates are formed in different process steps. Actually, these advantages just mentioned are a considerable justification to study DG physical properties and ameliorate their electrical performances for multi-applications such as analog, digital, radio frequency and so forth.

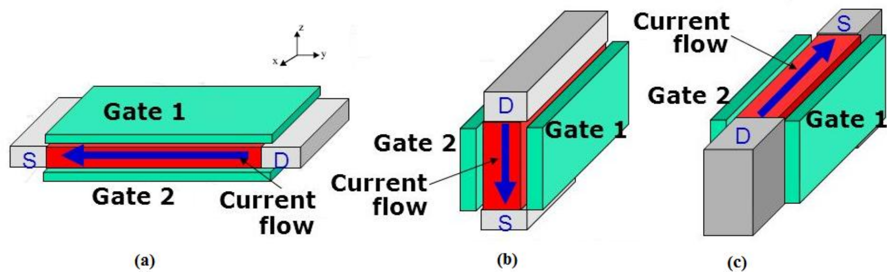

Figure I.15: DG MOSFETs topologies: (a) Planar type; (b) Vertical type; (c) Fin FET type.

It is clearly shown in Figure I.15(b) that the channel of the vertical DG MOSFET is in the vertical direction. It is most compact for DRAM application [31] with low leakage current, however it is topologically difficult for a CMOS logic application [28]. In addition, it is very difficult to fabricate the vertical DG MOSFET, notably due to the high difficulty in controlling the vertical doping profile, and showing no potential advantages compared to the FinFET design.

Currently, the Fin type (Figure I.15(c)) seems to be the most promising structure, which is being studied by many groups [32, 33, 34, 35]. In FinFET DG MOSFET, the current flowing horizontally through the fin channel, has the highest packing density for high-speed logic applications, since the channel width, the longest dimension of a logic FET, is perpendicular to the plane of the wafer [28].

One of the most important device among these three structures is the planar DG MOSFET, which is selected for studying the electrical performances, where the interest

of this dissertation dwells on the device design and basic physical modeling. One of the greatest reason to deal with this kind of MG MOSFETs is the scaling capability to the shortest channel length for a given gate oxide thickness because the bottom gate can effectively screen the field penetration from the drain, which leads hence to the suppression of the short channel effects. We can cite these advantages as: (i) ideal subthreshold slope 60 mV/decade [36]; (ii) scaling by silicon film thickness without high doping; (iii) adjustment of the threshold voltage by gate work functions [37], (iv) easy fabrication because of its planner structure, etc...

In this dissertation, our investigation will focus on the inversion mode planar DG MOSFET and its enhanced behavior versus the accumulation mode junctionless DGJL MOSFET. Our team has worked on analytic surface potential and threshold voltage models for DG MOSFETs several years [38]. One of the contributions of this dissertation is to propose and investigate a new design of the DGJL. Then, the developed device will be used to improve the electrical performances of the DGJL MOSFETs for analog and radio frequency (RF) applications. Efforts will also be concentrated on making the physics-based model more flexible and computationally efficient using soft computing techniques.

I.5 Gate-All-Around MOSFET architecture

The gate-all-around (GAA) MOSFET transistor [39] also known as surround gate MOSFET transistor (SGT) [40] is an innovative MOSFET architecture, where the silicon channel is completely surrounded by the gate. As shown in Figure 1.16, three different cross-section shapes are depicted [06]. GAA transistors will be described in detail in this dissertation because they are the geometry adopted in the context of neural computation and simulation of nanoscale circuits.

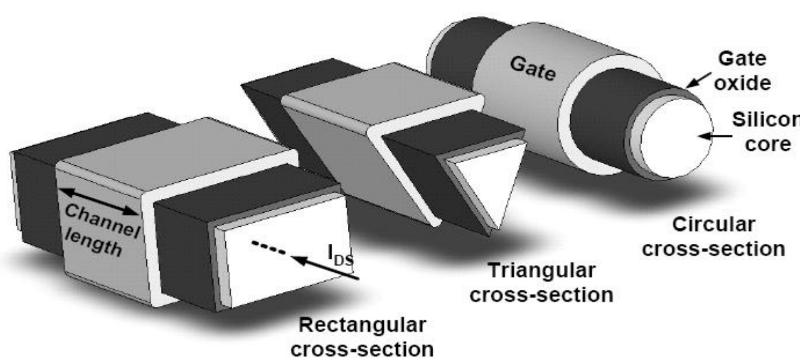

Figure I.16: Three architectures of the GAA MOSFET transistor with different sections [06].

GAA transistors are excellent devices, in terms of SCE, DIBL, subthreshold slope and I_{on}/I_{off} ratio. The main disadvantage of the GAA device is generally for the moment consisting of manufacturing processes that are very difficult. The manufacturing is often based on the realization of silicon nanowires. The channel cross-section is also crucial for the operation of the device. The corners in the channel (in rectangular or triangular shapes) contribute in corner effects and are considered as parasitic (double threshold voltage) or sometimes beneficial effects (low threshold voltage, local volume inversion). GAA silicon nanowire transistors are also very suitable structures in single-electron Transistor (SET) devices [06].

From 1990 to 2000, the efforts were mainly dedicated to the modeling of electronic properties using quantum mechanics, and many publications are still disconnected from all device applications [41]. The calculation of the silicon bandgap in a silicon quantum wire was first proposed in 1993 by Shen [42].

The first GAA transistor on SOI was presented in 1990 by Colinge [43]. Despite these large dimensions (W/L=3µm/3µm) and a thickness of 50 nm of gate oxide, such pioneer devices have correct characteristics. The manufacture of the device is very simple. A thin SOI wire is defined by lithography and etching, which is followed by the formation of buried oxide wire. The gate used is Low Pressure Chemical Vapor Deposition (LPCVD) polysilicon.

Another remarkable GAA MOS transistor was then proposed in 1997 by Leobandung et al. [44]. This is one of the first reports that include a full description of GAA performance. The dimensions of the nanowire are in agreement with the predictions of the ITRS in 1997. The wire has a rectangular cross-section (height × width 50 nm 35-75nm), the minimum wire length is 70 nm and the thickness of the gate oxide is 11 nm. Polysilicon is also used as a gate oxide material. The characteristics extracted are good, with a subthreshold slope 90 mV/dec. A multichannel design has been also proposed.

Since then, many optimized designs have been reported. We can refer to Song et al. [45] and Suk et al. [46] who achieved two excellent reports on GAA CMOS technology. The paper [45] makes a comparison between the two geometries dual-Gate and GAA indicating the GAA increased performance. Secondly, this report also compares a rectangular shape with a circular sectional channel, showing that a cylindrical silicon channel has much lower OFF current and lower SCE and DIBL effects, due to the

nonexistence of corner effects. The results published by [46] are also of great interest and present a process for the integration of silicon double nanowire MOSFETs. They obtained circular GAA devices of 5-10 nm in diameter with a gate length of 30 nm, with a remarkably high ON current for n-type transistors of 2.64 mA/µm.

I.5.1 Different categories of GAA MOSFET technology

Gate All Around (GAA) MOSFET transistors can be classified according to geometrical criteria (the shape of the channel) or electrical criteria (the direction of electronic transport) or also the number of channels they own. So, we can distinguish:

I.5.1.1 Rectangular GAA MOSFET transistor

The architecture of the rectangular GAA MOSFET transistor is based on that of SOI with triple gates (tri-gate) adding a gate from which it draws the name Quadruple-Gate (quad gate [47]). The channel cross-section of such transistor is in the form of a rectangle [48-49]. We note here that it derives from this architecture two other appellations, GAA MOSFET with cubic channel [50] and GAA MOSFET square [51], where such structure is illustrated in figure I.21.

I.5.1.2 Triangular GAA MOSFET transistor

The designation of triangular GAA MOSFET transistor [48] [52-53] is inspired from the cross-section of the device channel, which is in the form of a triangle. The cross-sectional view with dimensions of this architecture is shown in Figures I.17b and I.18a. The steps for producing such architecture are presented in Figure I.19.

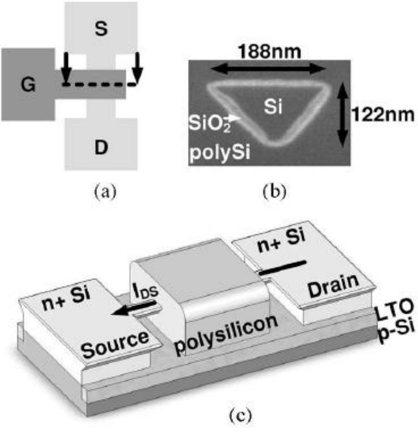

Figure I.17: (a) top view of the layout of a GAA MOSFET. (b) Cross-section view with SEM of triangular GAA MOSFET with dimensions (c) 3D diagram of GAA MOSFET [53].

I.5.1.3 Pentagonal GAA MOSFET transistor

The GAA MOSFET pentagonal transistor carries a channel where its section has a pentagonal shape [53] as shown in Figure I.18b. The steps for producing such a device are presented in Figure I.19.

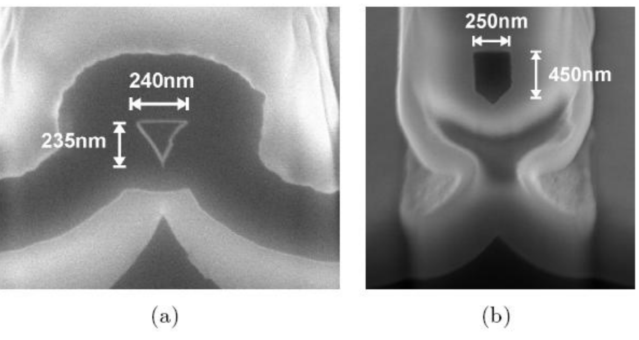

Figure I.18: FIB-SEM cross-section images of (a) triangular GAA MOSFET, and (b) pentagonal GAA MOSFET [7].

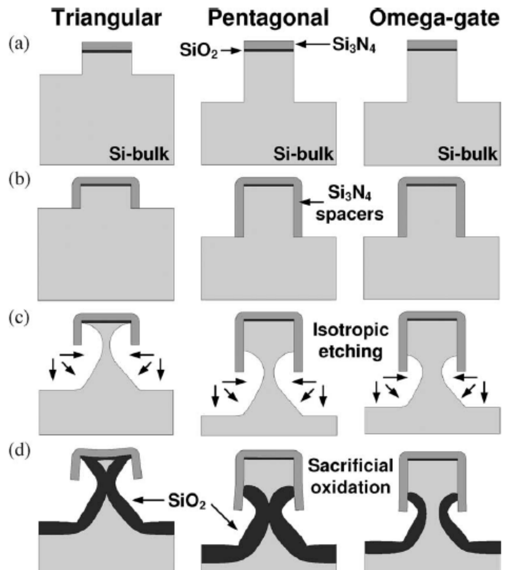

Figure I.19: Simplified steps of realization (cross-sections of the channel) of the triangular, pentagonal, and Ω-gate transistors [53].

I.5.1.4 Cylindrical GAA MOSFET transistor

The name of the cylindrical GAA MOSFET transistor is derived from the shape of its channel, which is in the form of a cylinder [54-60] and it is also called a circular channel transistor. Figure I.20a illustrates this architecture.

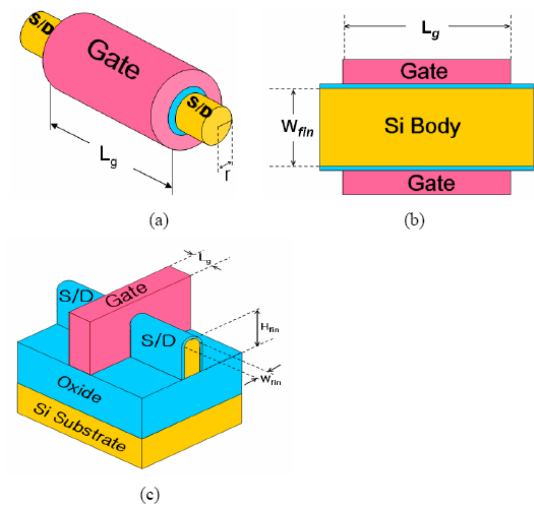

Figure I.20: (a) 3D schematic view of the GAA MOSFET transistor (b) sectional view of the DG MOSFET (c) 3D schematic view of the (SOI) FinFET transistor [61].

I.5.1.5 Single-channel GAA MOSFET transistor

Single-channel GAA MOSFET transistor, as shown in Figure I.21, is the simplest architecture considering the unique channel it has, which leads to simpler design and calculations than those performed for dual channels transistors (TSNWFET) and multichannel (MBCFET).

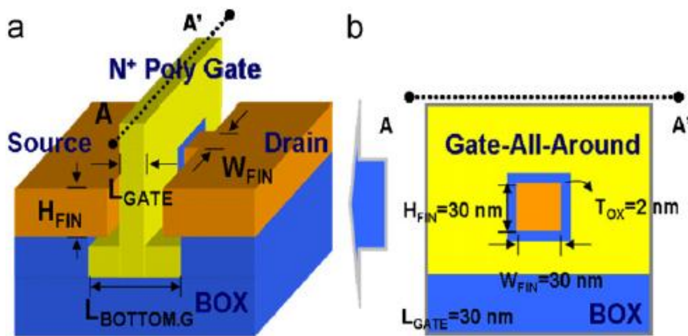

Figure I.21: 3D and Cross-section view of the Square GAA MOSFET with 1-channel [62].

I.5.1.6 Double-channel GAA MOSFET transistor

The double-channel GAA MOSFET transistor is also called Twin Nanowires MOSFET (TSNWFET) [49] [60] [63-64], where the transistor has two channels as shown in Figure I.22.

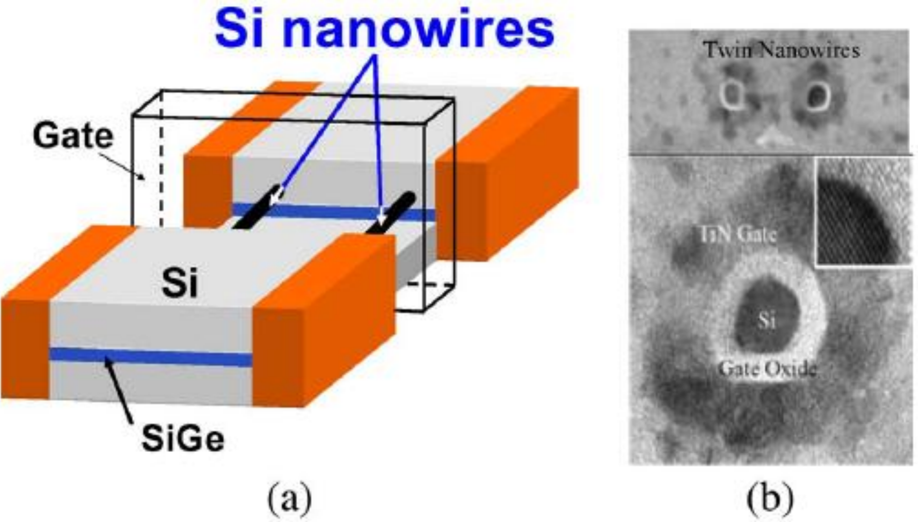

Figure I.22: (a) 3D diagram of TSNWFET GAA transistor (b) TEM cross-section images of TSNWFET [65].

I.5.1.7 Multi-channel GAA MOSFET transistor

The multi-channel GAA MOSFET transistor is also called Multi-bridge channel MOSFET [66] (MBCFET) [67-73]). In this case, the transistor has three or more channels. Figure I.23 shows a GAA Multi-bridge channel with five channels.

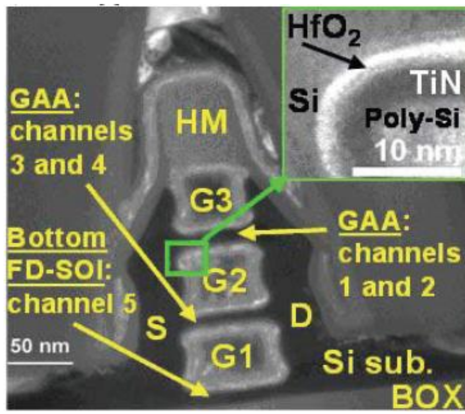

Figure I.23: (a) TEM cross-section image of the n-MCFET transistor with 5 channels [74].

I.5.1.8 Vertical GAA MOSFET transistor

In the case of vertical GAA MOSFET transistor [75-76], the electronic transport is perpendicular to the substrate plane and the gate field is parallel to the substrate.

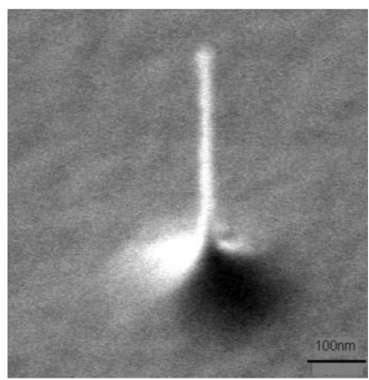

Figure I.24: SEM image of a vertical transistor with a thickness of ~ 20 nm and a height of 1µm [59].

I.5.2 Electrical properties of GAA MOSFET

The GAA MOSFET transistor is considered as one of the most promising devices to reduce the channel length below 50 nm [77-81]. Compared with the bulk MOS transistor and the single gate SOI MOS transistor, completely surrounding the channel (Figure I.25a) allows us to improve the electrostatic control of the channel and thus effectively tackle the short channel effects. Moreover, due to the volume inversion phenomenon, an improvement of the effective mobility of the carriers is expected.

In this section, we will make a comparative study of the electrical properties of GAA MOSFET with those associated to other SOI architectures.

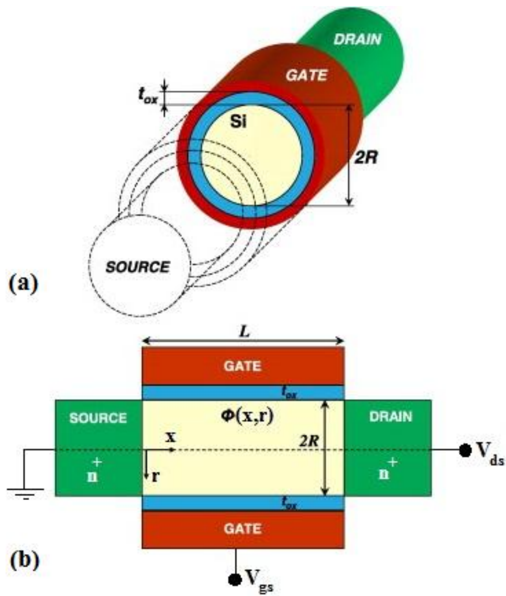

Figure I.25: Cylindrical GAA MOSFET (a) component structure in 3D (b) Cross-section view [58].

I.5.2.1 Threshold voltage definition

An appropriate definition of the threshold voltage of the bulk MOSFET transistors has been expressed as the gate voltage at which the surface potential is twice the Fermi level $2\phi_F$. Nevertheless, this definition is not sufficient for DG and GAA MOSFET transistors, where there is inversion or accumulation in the semiconductor film body, and not only at the surface, which leads to attaining the regime of strong inversion before the surface potential reaches a value of $2\phi_F$.

In the works of Chen et al. [82] and Ma et al. [83] on the DG MOSFET, the threshold voltage was rather defined as the gate voltage at which the minimum density of the charge carriers, Q_{inv} reaches Q_{TH} referring to the value corresponding to the beginning of the inversion mode. The same definition has been applied by Hamdy et al. on the GAA MOSFET [58], where the threshold voltage is given by:

$$V_{TH} = \emptyset_{ms} + \left(V_T \ln\left(\frac{Q_{TH}}{2n_i.r_0}\right)\right) \tag{I.25}$$

where $\emptyset_{ms}$: metal-semiconductor work function.

V_T: Thermal voltage.

n_i: Intrinsic concentration of free carriers.

r_0: Is the radius of the device.

I.5.2.2 **Passing state**

Adding the gate translates an addition inversion channel into a strong inversion channel. Thus, the forward ON current increases as the number of gates increases. This can be seen in Figure I.26 where $I_{DS}(V_{DS})$ characteristics are plotted for different SOI multi-Gate structures with a channel length of $15\ nm$. We note a current augmentation with the increase of the number of gates; as an illustration and for $t_{si} = 10nm$, I_{ON} reaches $1623\ A/m$ on the single gate SOI MOSFET, $2138\ A/m$ on the double-gate MOSFET, $2420\ A/m$ on the tri-gate MOSFET, and finally $2815\ A/m$ on the quadruple-Gate MOSFET.

However, this increase in I_{ON} is not proportional to the number of gates. The characteristics normalized by the number of gates represented in dashes are decreased when the number of gates increases. Hence, two parallel double-gate MOSFETs deliver

more current than a quadruple-gate MOSFET. In general, it should be noted that, in all these SOI devices, the current is greater than the current recommended by the ITRS [5], which has a magnitude of 1020 A/m. The decrease in t_{Si} reduces the I_{ON} current quasi-proportionally, so that the current of the double-gate MOSFET varies from 2420 to 1280 A/m for t_{Si} ranging from 10 to 5 nm.

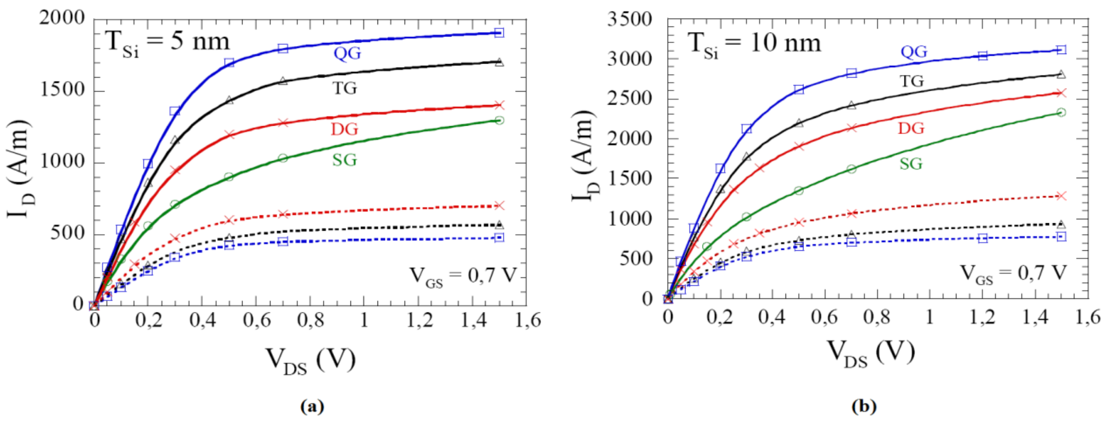

Figure I.26: $I_{DS}(V_{DS})$ characteristics of multi-gates for $L = 15\ nm$, (a) $t_{si} = 5\ nm$ and (b) $t_{si} = 10\ nm$. In dashes, the current is divided by the number of gates; 1 for the Single Gate SOI MOSFET (SG), 2 for the double-gate (DG) MOSFET, 3 for the tri-gate (TG) MOSFET and 4 for the quadruple-Gate (QG) MOSFET [1].

The transconductance g_m is also improved with the number of gates (Figure I.27). For $t_{si} = 10\ nm$, g_m reaches 41701 S/m on the double-gate MOSFET, 5700 S/m on the tri-gate MOSFET and 7070 S/m on the quadruple-gate MOSFET. This increase is not proportional to the number of gates. Decreasing the thickness of the device reduces the transconductance.

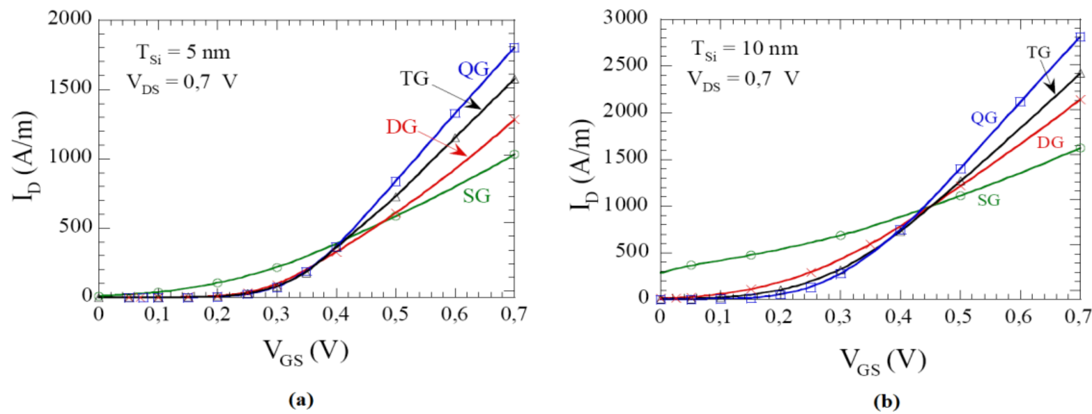

Figure. I.27: $I_{DS}(V_{GS})$ characteristics of multi-gates for $L = 15nm$, (a) $t_{si} = 5nm$ and (b) $t_{si} = 10nm$ [1].

I.5.2.3 Blocked state

In Figure I.28, we find that the characteristics of the single-gate SOI MOSFET device are severely degraded due to the short channel effects (SCEs) that are almost uncontrolled. The structures simulated in this figure correspond to MOS transistors with a channel length of 15 nm. The value of the subthreshold slope SS is greater than 100 mV/dec . It appears from this figure that the behavior under the threshold improves clearly with the increasing number of gates, and this is due to an improvement of the electrostatic control. For instance, for a film thickness of 10 nm, SS is 110 mV/dec on the double-gate MOSFET, 96 mV/dec on the tri-gate MOSFET and finally 83 mV/dec on the quadruple-gate MOSFET. The reduction of t_{si} also has a beneficial effect on SS: when t_{si} is varied from 10 nm to 5 nm, SS passes from 110 to 80 mV/dec in the double-gate MOSFET.

The explanation of this effect always comes from the control of the channel, which is much better when the two gates are close, that is when t_{si} is small.

Finally, we can conclude that the blocking power of the transistors is improved by reducing the thickness of the active area t_{si}. At $t_{si} = 10\ nm$, four gates would be required to keep SS values acceptable ($SS < 80\ mV/dec$ for $L = 15nm$), whereas at $t_{si} = 5\ nm$, only two would be sufficient.

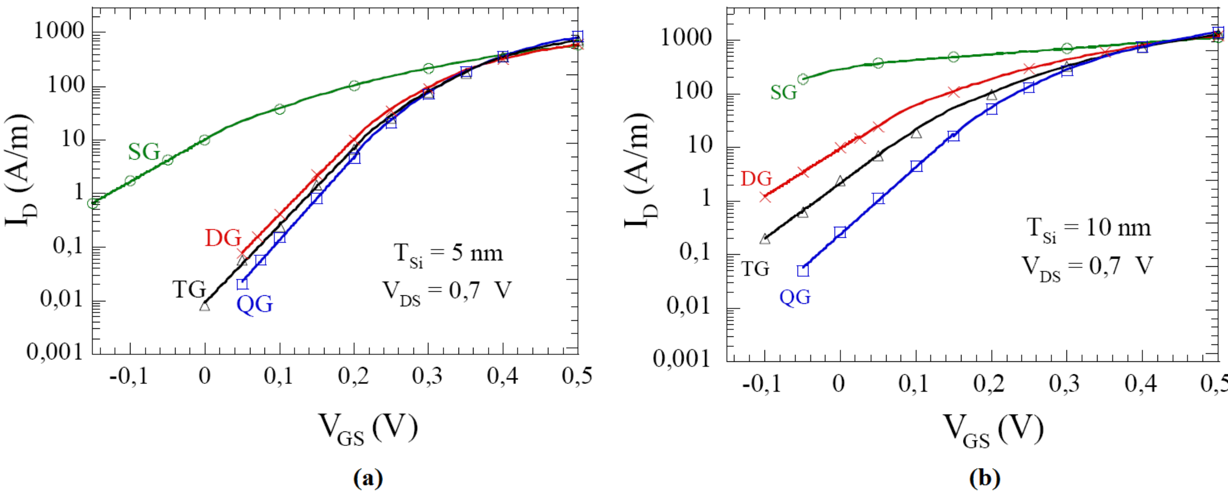

Figure I.28: $I_{DS}(V_{GS})$ characteristics in logarithmic scale of multi-gates for $L = 15nm$, (a) $t_{si} = 5nm$ and (b) $t_{si} = 10nm$ [1].

I.6 Conclusion

In this chapter, we have introduced various concepts of the long channel and nanoscale MOSFET design. We have also presented a summary of the existing literature review of Multi-Gate transistor devices and various technologies. This literature survey has helped to identify various harmful effects related to the short channel. To conclude, we can emphasize that both double gate (DG) and Gate All Around (GAA) MOSFET transistors are interesting given their offered electrical performances. The major difficulty in their development is at the technological level.

Chapter II: Soft Computing based methods

II.1 What is Soft Computing ?

To begin, first "*soft computing*" is a widely-used term in most of the scientific fields, and especially in the engineering ones. In order to better understand the real meaning of this term, it could be quite useful to mention and refer to the first who has produced this term. The term "*soft computing*" was initiated in the early 1990s, when Lotfi A. Zadeh, the father of fuzzy logic and one of the leaders in the soft computing community, published his first paper on soft data analysis, where he has defined "soft computing" [84]. He also established the Berkeley Initiative in Soft Computing. This group includes students, professors, employees of private and government organizations, and other individuals interested in soft computing. Since that time, many researchers have tried to define it considering different approaches such as: in terms of its main constituents, its use, properties, abilities, etc. This means that several definitions from different viewpoints and many others could be taken into consideration. From this understanding, in what follow we mention several definitions that have been revealed in literature, where each one uses a different approach and emphasizes different aspects. These include definitions and characterizations of "*soft computing*" as:

- a family of several computing techniques,
- an antithesis of hard computing,
- a tool for coping with imprecision and uncertainty, and
- by essential characteristics.

II.1.1 Soft Computing as the fusion of several preexisting techniques

Soft Computing techniques can either be deployed as separate tools or be integrated in unified and hybrid architectures. The fusion of Soft Computing techniques causes a paradigm shift (breakthrough) in engineering and science fields by solving problems, which could not be solved with the conventional and the stand-alone computational tools.

II.1.1.1 Soft Computing as the mixture of separate tools

As mentioned previously, the term "*Soft Computing"* was coined by Lotfi A. Zadeh to refer to one multidisciplinary computing techniques particularly adapted to cope with a class of problems for which other techniques were not quite well suited. Zadeh established the definition of soft computing in the following terms [85]:

"Basically, soft computing is not a homogeneous body of concepts and techniques. Rather, it is a partnership of distinct methods that in one way or another conform to its guiding principle. At this juncture, the dominant aim of soft computing is to exploit the tolerance for imprecision and uncertainty to achieve tractability, robustness and low solutions cost. The principal constituents of soft computing are fuzzy logic, neurocomputing, and probabilistic reasoning, with the latter subsuming genetic algorithms, belief networks, chaotic systems, and parts of learning theory. In the partnership of fuzzy logic, neurocomputing, and probabilistic reasoning, fuzzy logic is mainly concerned with imprecision and approximate reasoning; neurocomputing with learning and curve-fitting; and probabilistic reasoning with uncertainty and belief propagation."

Therefore, it is clear from this definition that rather than to provide a precise definition for "Soft Computing", it is easily defined by enumeration of the available techniques and concepts which attempt to surmount the difficulties that take place in real problems whichever occur in an imprecise, an uncertain and a difficult to categorize world. Figure II.1 illustrates the development history of the Soft Computing as the mixture of several preexisting techniques.

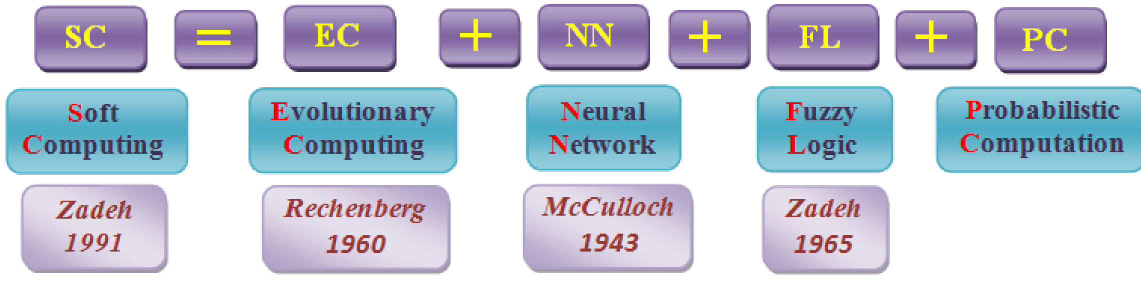

Figure II.1: Development history of the Soft Computing.

Another concept we can extract from this enumeration of techniques is the fact that Soft Computing is an evolving concept. In this early definition, genetic algorithms are considered as a part of probabilistic reasoning, but, as the presence of genetic algorithms techniques has gained importance in the field, more recent enumerations have included Evolutionary Computation (EC, a family of search and optimization techniques that among others include genetic algorithms) as an independent constituent of Soft Computing. In that sense, most enumerations of Soft Computing components contained

Fuzzy Logic, Neural Network, Probabilistic Computation, and Evolutionary Computation as the four basic and essential components.

II.1.1.2 Soft Computing as unified and hybrid tools

Fuzzy logic, genetic algorithms, and artificial neural networks are not competing with each other, but instead, they may be mixed on the basis of integrated frameworks to outperform conventional design approaches. Furthermore, each individual Soft Computing technique has certain strengths and weaknesses and they cannot be applied commonly to every problem. It is also interesting to mix at least two techniques or more to obtain what we call a hybrid technique. For instance, combining a neural network with a fuzzy system results in a hybrid neuro-fuzzy system.

In this sense, and using the combination of the fourth based techniques which are probabilistic reasoning, fuzzy logic, neural networks, and evolutionary computation forms the core of soft computing (SC). This essential role of hybridization and according to Cordon et al. [86] can be represented by Figure II.2, using the idea of different hybrid techniques appearing as the intersecting areas of the main components of Soft Computing.

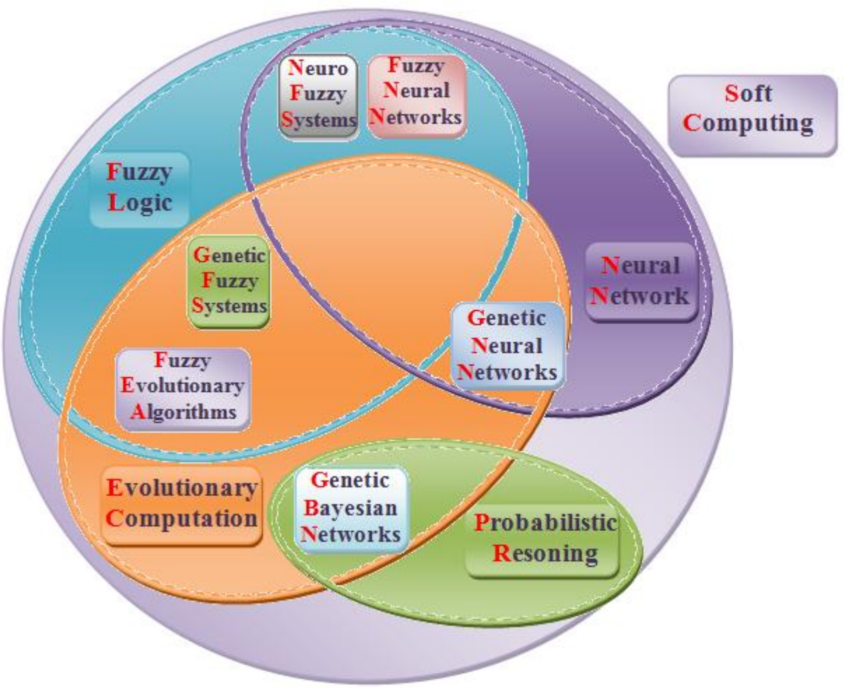

Figure II.2: New design using hybridization according to Cordon et al.[86].

In this extent, one of the main characteristics of Soft Computing is that of hybridization. With independence to the techniques considered as a part of SC, hybridization is surely one of the central aspects of the field of Soft Computing.

II.1.2 Soft Computing as an antithesis of Hard Computing

Another way of defining soft computing, that we will take into account here is whereby it is considered to be the opposite of what we might call traditional computing or also as it is well-known hard computing. Lotfi A. Zadeh formulated this new scientific concept in [84]. “In traditional -hard- computing, the prime desiderata are precision, certainty, and rigor. By contrast, the point of departure in soft computing is the thesis that precision and certainty carry a cost and that computation, reasoning, and decision making should exploit -wherever possible- the tolerance for imprecision and uncertainty”. The term soft computing distinguishes those previously enumerated techniques from hard computing (conventional approaches) considered as less flexible and more computationally demanding. Soft computing could, therefore, be considered as a series of methods and techniques of computation so that real practical situations could be dealt with in the same way as humans deal with them, which means on the basis of intelligence, common sense, consideration of analogies, approaches, and so forth. In this sense, we can consider soft computing as a family of problem-resolution techniques headed by approximate reasoning and functional and optimization approximation methods, including search methods.

In this context, we can say that the main principle of the Soft Computing is to elaborate methods of computation that lead to the desired solution with low cost and more robustness by seeking for an approximate solution to the inaccurate or precisely formulated problem. Soft Computing differs from conventional (hard) computing in term of tolerance of imprecision, uncertainty, partial truth and approximation. Therefore, the role model for SC is the human mind. SC is basically an optimization technique which is applied to find solution to problems that are very hard to answer.

II.1.3 Soft Computing as a tool for outfacing with imprecision and uncertainty

In 1992 Lotfi A. Zadeh has also described the term “*soft computing*” by the following definition [87]: ”Soft computing is an emerging approach to computing which parallels the remarkable ability of the human mind to reason and learn in an environment of uncertainty and imprecision”. The main target to deal with which is Soft Computing

techniques is designed to operate in an environment that is subject to uncertainty and imprecision. According to Zadeh [87], the guiding principle of soft computing is:

"exploit the tolerance for imprecision, uncertainty, partial truth, and approximation to achieve tractability, robustness, low solution cost and better rapport with reality."

It is well-known that imprecision is the result of our bounded capability to resolve detail and encompasses the notions of noisy, vague, partial and incomplete data about the real world. In other words, Soft Computing techniques are designed to outfacing with all those unwanted properties that real-world uses to add to the problems under consideration. This means, it is not only difficult or even impossible but also unsuitable to use traditional computing techniques when dealing with circumstances in which the required data is not available and/or the measures of the considering variables are noisy and/or the behavior of the considered system is not totally known. The point of view described here in this section is the most common approach when talking about Soft Computing as a tool to outfacing with imprecision and uncertainty, but we can go deeper and analyze those situations where imprecision is not a drawback of the data we are managing but an intrinsic characteristic of that data. In that sense, it is quite important to distinguish between measurements and perceptions, and to differentiate those situations where we work on the basis of imprecise measurements from those where we calculate with perceptions. Calculating with perceptions is obviously an approach to approximate reasoning.

In the sense of soft computing as a tool to outfacing with imprecision and uncertainty should obviously incorporate computing with perceptions and words as one of its essential components. Computing using words is inspired by the amazing human capability to carry out a large diversity of physical and mental tasks without any need to use measurements. As a methodology, computing with words provides a foundation for a computational theory of perceptions.

It is clear that the fundamental difference between measurements and perceptions is that, in general, measurements are crisp but perceptions are fuzzy. One of the potential achievements of soft computing will be to return to perceptions in order to take profit of its qualities as a carrier for intrinsically imprecise data. It is reasonably important to understand that the existence of uncertainty or imprecision is not an objective for Soft

Computing but it derives from the properties or circumstances of the problem under consideration, or they are added as a need to surmount the complexity of the problem.

II.1.4 Soft Computing defined by essential characteristics

Defining "Soft computing" taking into consideration the most important characteristics or properties was proposed by Li et al. [88] in their article, where they defined soft computing as "Every computing process that purposely includes imprecision into the calculation on one or more levels and allows this imprecision either to change (decrease) the granularity of the problem, or to ''soften'' the goal of optimisation at some stage, is defined as to belonging to the field of SC". From this definition, we can clearly see that it includes all those approaches and techniques of computing that have been previously mentioned and defined as the components of soft computing.

The main and essential characteristic, which is taken into consideration behind this point of view, is that computing process in soft computing techniques purposely includes imprecision into the calculation changing (relaxing) the level of description of the problem or the level of achievement of the goal. However, the imprecision is not a target, but it is considered as a need to achieve a higher order objective that could be summarized as "solvability" of the problem. Furthermore, it is possible to say that, soft computing encompasses two main conceptual components, namely approximate reasoning and function approximation and optimization.

From this viewpoint, we can consider any computing technique as belonging to the Soft Computing technique all those reasoning and optimization techniques that suppose and incorporate imprecision when solving a problem either as a consequence of the presence of that imprecision in the available information or as a mean to overcome complexity and achieve feasibility and solvability.

II.2 Introduction to Fuzzy logic

Before to dive in the subject of fuzzy logic, we should begin with this basic and essential statement: fuzzy logic is not logic that is fuzzy, but the logic that is used to describe fuzziness, and also it is a better approximation to reality.

In 1937, a paper called '*Vagueness: an exercise in logical analysis*' was published by Max Black, a philosopher [89]. The most important contribution of Black in this paper

was in its appendix. Where he defined the first simple fuzzy set and outlined the basic ideas of fuzzy set operations.

Later, in 1965, a Professor and Head of the Electrical Engineering Department at the University of California, Berkeley named Lotfi Askar Zadeh, published his famous paper 'Fuzzy sets'[90]. In this paper, he developed the theory of fuzzy sets, which is a generalization of the classical set theory. He is being an expert in control engineering realized that control theory was unable to solve many complex real system problems.

In short term, fuzzy logic may be considered as a logical system that goals at a formalization of approximate reasoning. In long-term, fuzzy logic is used as a synonym for a fuzzy set theory which has several branches such as fuzzy arithmetic, fuzzy mathematical programming, fuzzy topology, fuzzy graph theory, fuzzy data analysis, and fuzzy logic, among others [84].

The contribution of fuzzy logic to the area of soft computing is to introduce flexibility in classification, querying and problem-solving, and to capture imprecision when there is a lack of information [91]. In this context, fuzzy logic brings an effective way of compressing and representing knowledge through the use of linguistic variables, linguistic values, and fuzzy if-then-rules.

II.2.1 Basic concept

A linguistic variable is the principal concept underlying fuzzy logic, which is a variable whose values are words instead of numbers (such as tall, very tall, short, fast, and smart). A linguistic variable is a fuzzy variable. For example, the statement *'Mohamed is tall'* implies that *Mohamed* is the linguistic variable and it takes the linguistic value *tall*.

The universe of discourse of the linguistic variable is presented by the range of possible values of that variable. For example, the linguistic variable *height* might have the universe of discourse with a range between 100 and 210 cm and may include such fuzzy subsets as *very short, short, medium, tall*, and *very tall*.

II.2.2 Fuzzy sets

We use fuzzy sets in fuzzy logic to relate classes of objects with unclearly (fuzzy) defined boundaries in which membership is a matter of degree.

In the theory of conventional sets as an example, an element totally belongs or totally does not belong to a set. Let us consider X is the universe of discourse and its elements are denoted as *x*. In conventional set theory, crisp set *A* of *X* is defined as a function $f_A(x)$ called the characteristic function of A

$$f_A(x): X \rightarrow \{0,1\} \tag{II.1}$$

where

$$f_A(x) = \begin{cases} 1, & if\ x \in A \\ 0, & if\ x \notin A \end{cases}$$

so the degree of membership of an element in a set can only take the value zero or unity. On the contrary, in the theory of fuzzy sets, fuzzy set A of universe X is defined by a function $\mu_A(x)$ called the membership function of set A

$$\mu_A\ (x): X \rightarrow [0\ ,1] \tag{II.2}$$

where

$$\mu_A(x) = 1\ \ if\ x\ is\ totally\ in\ A$$

$$\mu_A(x) = 0\ \ if\ x\ is\ not\ in\ A$$

$$0 < \mu_A(x) < 1\ \ if\ x\ is\ partially\ in\ A$$

An element can belong more or less to a set. This set allows a continuum of possible choices. Thus, the degree of membership of an element in a fuzzy set can take any value in the range of [0, 1]. What differentiates the two theories arises from limitations of defined sets. In classical theory the contours of the sets are “net”, although for the fuzzy sets contours are gradual, or fuzzy as shown in Figure II.3.

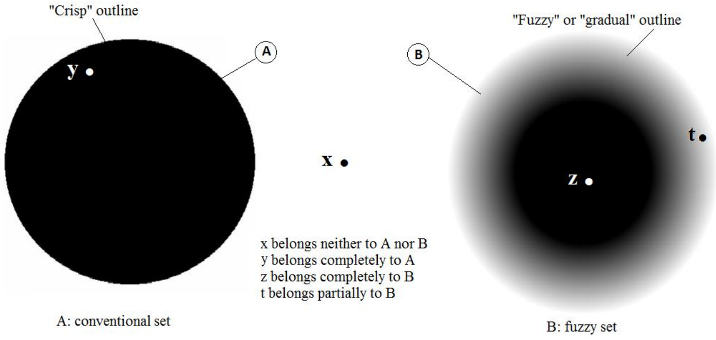

Figure II.3: Comparison between classical and fuzzy sets.

II.2.3 Membership functions

A fuzzy set as mentioned previously is an extension of a crisp set where (in a crisp set) an element can only belong to a set (full membership) or not belong at all (no membership). Fuzzy sets allow partial membership, in other words, an element may partially belong to one or more than one set. The membership function is the solution of the representation of a fuzzy set. A fuzzy set A is characterized by a membership function μ_A that assigns to each object *x* in a given class a degree of membership to the set. The degree of membership ranges from 0 (no membership) to 1 (full membership) written as,

$$\mu_A(x) : X \rightarrow [0\,,1] \qquad \text{(II.3)}$$

which means that the fuzzy set A belongs to the universal set X (called the universe of discourse) defined in a specific problem. A membership function defines how each point in the input space is mapped to a degree of membership.

For example, consider the set of membership functions for a set of tall people shown in Figure II.4. If the set is given the crisp boundary of a classical set, it can be considered that all people taller than 170 cm, while those less than 170 cm are short. But, such a distinction is not fully realistic. If one would, however, consider a smooth curve from "short" to "tall", then the transition would make more sense. A person may be both tall and short to some degree. The output axis would be a number between 0 and 1, known as the degree of membership in a fuzzy set of height.

The value $\mu_A(x)$ in equation (II.3) measures the membership or the membership degree to which an element *x* belongs to the set A. Then, each fuzzy set can be represented by its membership function. The membership functions may be symmetrical, consistently distributed or have a non-uniform distribution. In general, the shape of membership functions depending on the application and the quantity to be modeled may have different shapes: triangular, Gaussian or trapezoidal function, etc. [90, 92, 93].

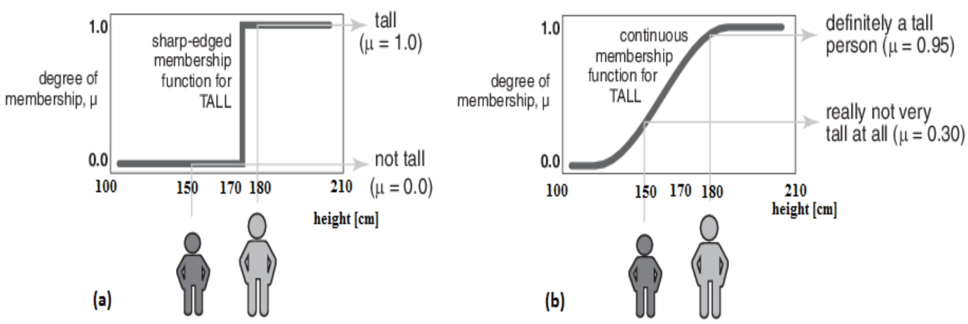

Figure II.4: Illustration of membership functions for a set of tall people (a) crisp set (b) fuzzy set.

II.2.3.1 Triangular membership function

A triangular membership function is defined by three parameters $\{a, b, m\}$ as follows:

$$T(x;a,m,b) = \begin{cases} 0 & if\ x \leq a \\ (x-a)/(m-a) & if\ a \leq x \leq m \\ (b-x)/(b-m) & if\ m \leq x \leq b \\ 0 & if\ x \geq b \end{cases}$$

where the parameter a presents its lower limit, b its upper limit, and m the modal value, so that $a < m < b$. We call the value $b - m$ margin when it is equal to the value $m - a$ as depicted in Figure II.5.

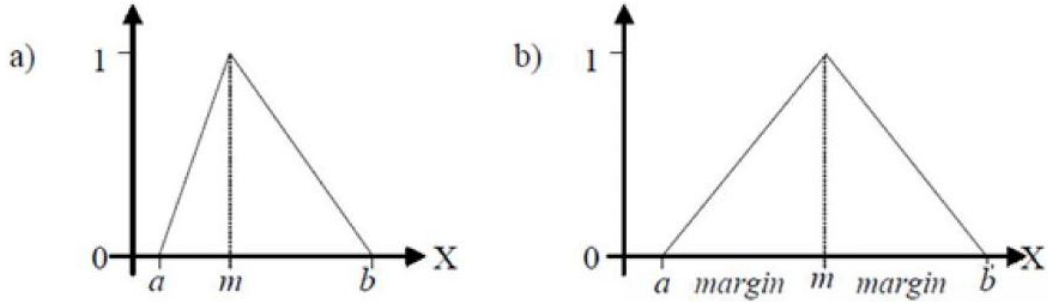

Figure II.5: Triangular membership function (a) general (b) symmetrical.

II.2.3.2 Singleton membership function

The Singleton membership function takes the value 0 in all the universe of discourse except in the point *m*, where it takes the value 1. It is the representation of a crisp value.

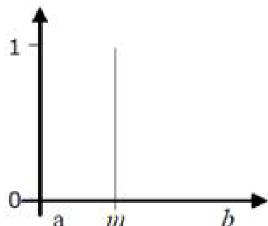

Figure II.6: Singleton membership function.

$$SG(x) = \begin{cases} 0, & if\ x \neq m \\ 1, & if\ x = m \end{cases}$$

II.2.3.3 L membership function

This function is defined by two parameters *a* and *b*, in the following way:

$$L(x; a, b) = \begin{cases} 1, & if\ x \leq a \\ \frac{b-x}{b-a}, & if\ a < x \leq b \\ 0, & if\ x > b \end{cases}$$

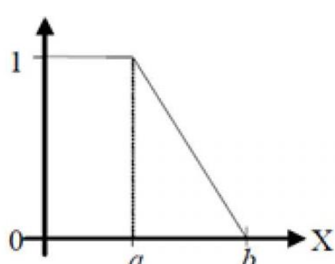

Figure II.7: L membership function.

II.2.3.4 Gamma membership function

It is defined by its lower limit *a* and the value *k*>0.

$$\Gamma(\mathrm{x}; \mathrm{a}) = \begin{cases} 0 & if\ x \leq a \\ \frac{k(x-a)^2}{1+k(x-a)^2} & if\ x > a \end{cases}$$

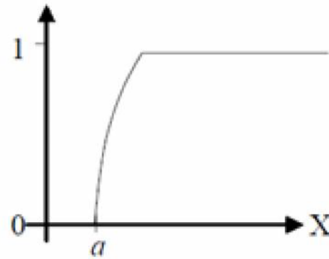

Figure II.8: A generic form of Gamma membership function.

• This function is characterized by a rapid growth starting from a.

• k determines the rate of growth.

• It has an horizontal asymptote in 1.

The function can also be expressed in a linear way as illustrated in Figure II.9.

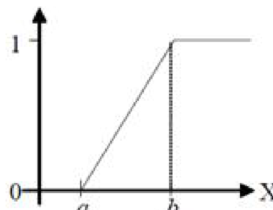

Figure II.9: Gamma membership function in its linear form.

$$\Gamma(\mathrm{x};\mathrm{a},\mathrm{b}) = \begin{cases} 0, & if\ x \leq a \\ \dfrac{x-a}{b-a}, & if\ a < x \leq b \\ 1, & if\ x > b \end{cases}$$

II.2.3.5 Trapezoid membership function

A trapezoidal membership function is specified by four parameters $\{a, b, c, d\}$ as follows:

$$T(x; a, b, c, d) = \begin{cases} 0 & if\ \ x \leq a \\ \dfrac{x-a}{b-a} & if\ a \leq x \leq b \\ 1 & if\ b \leq x \leq c \\ \dfrac{d-x}{d-c} & if\ c \leq x \leq d \\ 0 & if\ x \geq d \end{cases}$$

where the parameter a presents its lower limit, d its upper limit, whereas b and c present the lower and the upper limits of its nucleus respectively as depicted in Figure II.10.

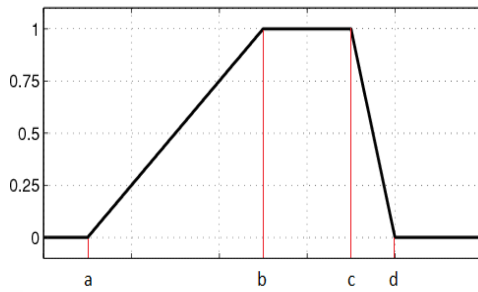

Figure II.10: Trapezoidal membership function.

II.2.3.6 S membership function

Defined by its lower limit *a*, its upper limit *b*, and the value *m* standing for the point of inflection, so that $a < m < b$. A typical value is $m = \frac{a+b}{2}$. Growth is slower when the distance $a - b$ increases.

$$S(x; a, m, b) = \begin{cases} 0, & x \leq a \\ 2\{(x-a)|(b-a)\}^2, & a \leq x \leq m \\ 1 - 2\{(x-a)|(b-a)\}^2, & m \leq x \leq b \\ 1, & x \geq b \end{cases}$$

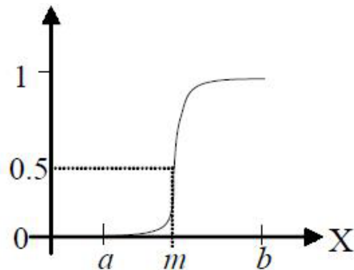

Figure II.11: S membership function.

II.2.3.7 Gaussian membership function

A Gaussian membership function is specified by two parameters $\{\sigma, \mathrm{m}\}$ as follows:

$$\mathrm{G}(\mathrm{x}; \sigma, \mathrm{m}) = \mathrm{e}^{\frac{-(\mathrm{x}-\mathrm{m})^2}{2\sigma^2}}$$

where the parameter *m* represents the membership function center and σ determines the membership function width. The smaller σ is, the narrower the bell.

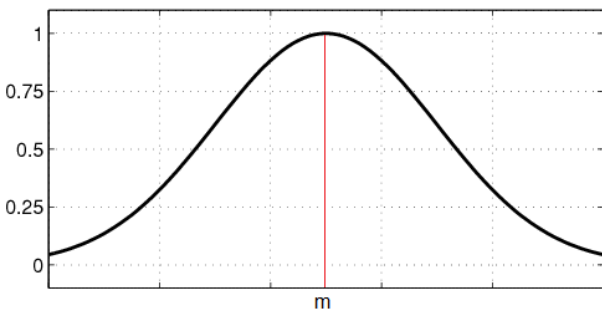

Figure II.12: Gaussian membership function.

II.2.3.8 Pseudo-Exponential membership function

Defined by its mid-value *m* and the value $k > 1$. As the value of *k* increases, the rate of growth increases, and the bell becomes narrower.

$$P(x,k,m) = \frac{1}{1 + k(x-m)^2}$$

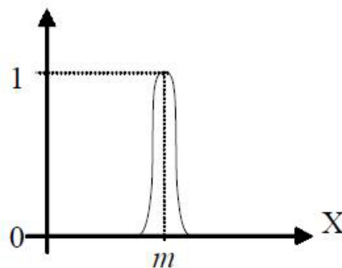

Figure II.13: Pseudo-Exponential membership function.

II.2.4 Fuzzy set operations

We can use operations using fuzzy sets as with traditional sets. The most common fuzzy set operations extend union, intersection, and complement. We should note that using the interval [0, 1], instead of the set {0,1}, gives us infinite possibilities for operations. Mostly, we will be interested in aggregation operations, for example to average out different expert opinions.

II.2.4.1 Fuzzy complement (negation)

The complement (negation) of a fuzzy set A, denoted by $\bar{A}$ or $\neg A$, or $NOT\ A$ which contains all elements that belong to the universal set but do not belong to A and it is defined by

$$\mu_{\bar{A}}\ (x) = 1 - \mu_A\ (x)$$

as illustrated in Figure II.14.

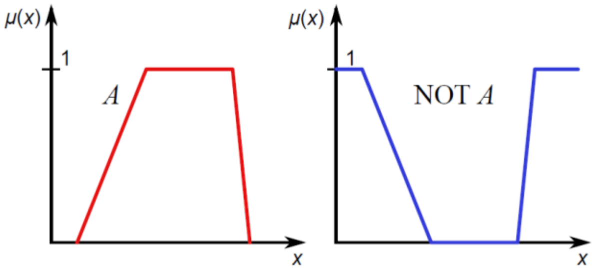

Figure II.14: Illustration of the complement (negation) of a fuzzy set.

II.2.4.2 Fuzzy union (disjunction)

The union of two fuzzy sets A and B is a fuzzy set C, written as $C = A \cup B$ or as $C = A\ OR\ B$, the membership function of which is related to those *of A and B by*

$$\mu_C(x) = max(\mu_A(x), \mu_B(x)) = \mu_A(x) \vee \mu_B(x)$$

Such case is depicted in Figure II.15.

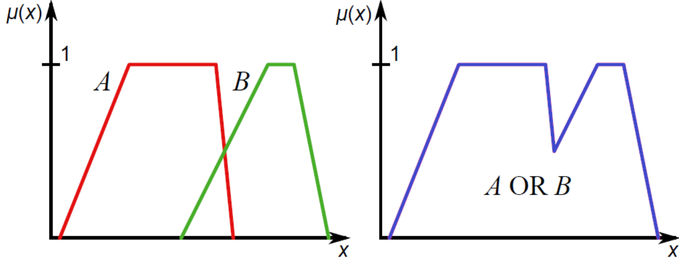

Figure II.15: Illustration of the union (disjunction) of two fuzzy sets.

II.2.4.3 Fuzzy intersection (conjunction)

The intersection of two fuzzy sets A and B is a fuzzy set C, written as $C = A \cap B$ or $C = A\ AND\ B$, the membership function of which is related to those of A and B by

$$\mu_C(x) = \min(\mu_A(x), \mu_B(x)) = \mu_A(x) \wedge \mu_B(x)$$

Figure II.16. gives an example of the fuzzy intersection of the two fuzzy sets A and B.

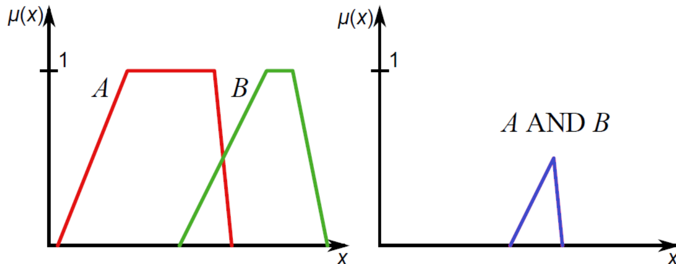

Figure II.16: Illustration of the intersection (conjunction) of two fuzzy sets.

II.2.4.4 Containment (subset)

A is a subset of B (or Fuzzy set A is contained in fuzzy set B), if $\mu_A(x) \leq \mu_B(x)$ for all *x*:

$$A \subseteq B \Leftrightarrow \mu_A(x) \leq \mu_B(x)$$

As can be seen from Figure II.17, for all value of x the relation $\mu_A(x) \leq \mu_B(x)$ is always true.

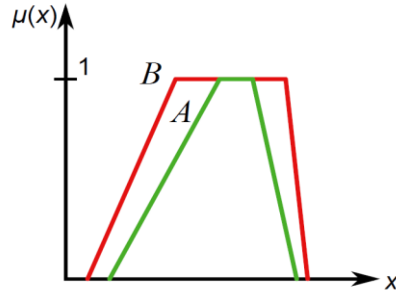

Figure II.17: Illustration of the containment (subset) between two fuzzy sets.

II.2.5 Fuzzy logic rules

Lotfi Zadeh, in 1973 published his second most influential paper [94]. He outlined in this paper a new approach to the analysis of complex systems, in which he suggested capturing human knowledge in fuzzy rules.

The use of fuzzy sets allows the characterization of the system behavior through fuzzy rules between linguistic variables. A fuzzy rule, also known as a fuzzy if-then rule, fuzzy conditional statement, or fuzzy implication, is a conditional statement R_i based on expert knowledge assumes the form:

$$R_i : \text{IF } x \text{ is small THEN } y \text{ is large} \quad \text{(II.4)}$$

where *x* and *y* are fuzzy variables whereas *small* and *large* are linguistic values defined by fuzzy sets on universes of discourse X and Y, respectively. The expression "*x is small"* is called the antecedent or premise, while "*y is large"* is called the consequence or conclusion.

Expression (II.4), which is abbreviated as $A \to B$, can be defined as a binary fuzzy relation R on the product space $X \times Y : R = A \to B$. R can be viewed as a fuzzy set of two-dimensional MF

$$\mu_R(x, y) = f(\mu_A(x), \mu_B(y))$$

where the function f is called the fuzzy implication function, that transforms the membership degrees of *x* in A and *y* in B into those of (*x*, *y*) in $A \to$B.

If there are *n* rules, the rule set R is represented by the union of all these *n* rules i.e.,

$$R = R_1 \; else \; R_2 \; else \ldots else \; R_n \quad \text{(II.5)}$$

A fuzzy controller is based on a collection of R control rules. The execution of these rules is governed by the compositional rule of inference [95]. The relationship between the

premise and the consequence of the rule is determined by a fuzzy inference. Then, the degree of truth is defined by a membership function which depends on the degree of truth μ_A and μ_B of the two elementary propositions.

The most common inferences for the determination of the membership functions resulting from the fuzzy scheme are given by:

The inference of Mamdani:

$$\mu_R(x, y) = min(\mu_A(x), \mu_B(y)) \tag{II.6}$$

The inference of Larsen:

$$\mu_R(x, y) = \mu_A(x) . \mu_B(y) \tag{II.7}$$

II.2.6 Fuzzy logic model

The process of fuzzy logic model unlike conventional techniques does not use specific mathematical relationships or accurate formulas [96]. However, it controls the inferences with several fuzzy rules based on fuzzy operators such as AND, OR, THEN.

Figure II.18 illustrates the general structure of a fuzzy logic model and depicts its four principal components.

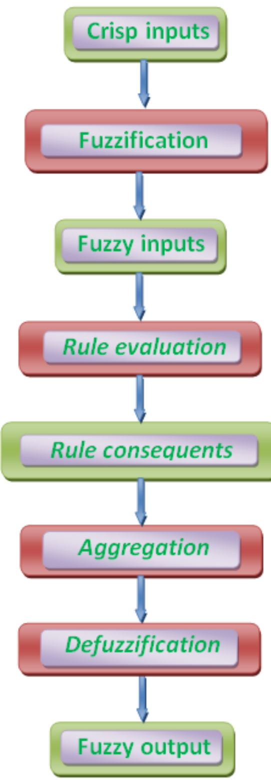

Figure II.18: Block diagram of the fuzzy logic model.

Figure II.18 introduces the global block diagram of the fuzzy logic model and in what follows we present in a detailed manner the associated elementary steps.

II.2.6.1 Fuzzification

The first step in the fuzzy logic model is fuzzification, which allows defining membership functions for the linguistic variables. It converts crisp inputs data into suitable linguistic values (degree of membership) using a membership function. Some of these inputs can be measured directly (voltage, current, temperature, pressure, speed, distance etc.) while others can be based only on the expert estimate. The conversion of crisp inputs into linguistic values is a projection as illustrated in Figure II.19 of the physical variable to the fuzzy sets by characterizing the variable. In addition, fuzzification allows an accurate measurement of the degree of membership of the input variable for each fuzzy set [97].

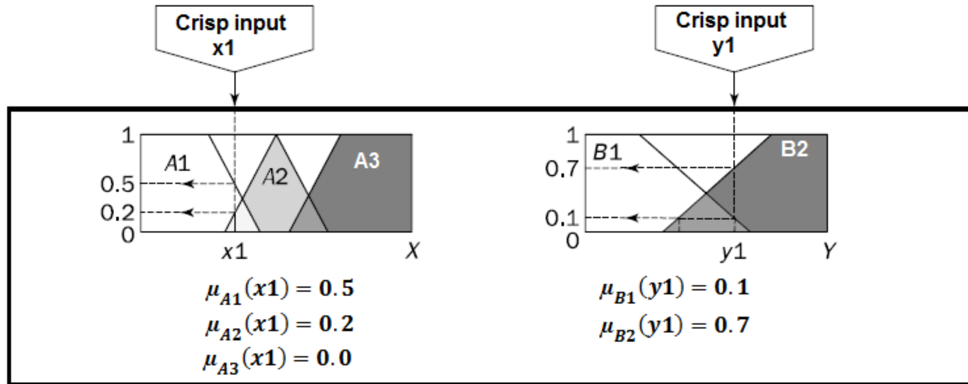

Figure II.19: Fuzzification step diagram.

Furthermore, the membership functions defined over the so-called universe of discourse of the input variables are applied to their actual values with the aim of obtaining the grade of truth for each rule as explained in the next step.

II.2.6.2 Rule evaluation

After fuzzification, rule evaluation is the second step applied in the fuzzy logic model. In this step, we take the fuzzified inputs and apply them to the antecedents of the fuzzy rules. As depicted in Figure II.20 for the two rules Rule 1 and Rule 2, a fuzzy operator (AND or OR) is used. If a given fuzzy rule has multiple (two or more) antecedents in order to obtain a single number that represents the result of the antecedent evaluation. This number (the truth value) is then applied to the consequent membership function.

As can be seen from Figure II.20 (Rule 1), to evaluate the disjunction of the rule antecedents, we use the OR fuzzy operation:

$$\mu_C(x) = \mu_{A\cup B}(x) = \max(\mu_A(x), \mu_B(x)) = \mu_A(x) \vee \mu_B(x)$$

Similarly as also shown in Figure II.20 (Rule 2), in order to evaluate the conjunction of the rule antecedents, we apply the AND fuzzy operation intersection:

$$\mu_C(x) = \mu_{A\cap B}(x) = \min(\mu_A(x), \mu_B(x)) = \mu_A(x) \wedge \mu_B(x)$$

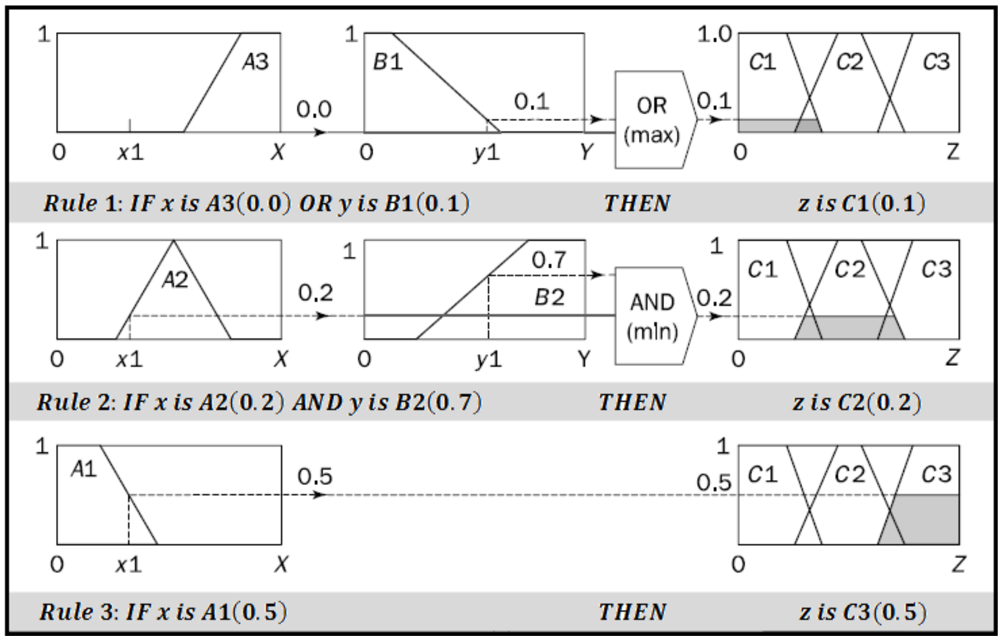

Figure II.20: Diagram of the rule evaluation step.

The interface inference consists of three blocks:

• The knowledge base consists of a database with the necessary linguistic definitions and the control rule set.

• The rule base consists of a set of relations linking the input variables to the output variables of the system to be adjusted. The truth-value for the premise of each rule is computed and applied to the consequence part of each rule. This results in one fuzzy set to be assigned to each output variable for each rule.

• The inference engine performs the digital processing of inference rules, described by fuzzy operators for linguistic or fuzzy output. It simulates a human decision-making process in order to infer the fuzzy control action from the knowledge of the control rules and the linguistic variable definitions. Thus, all of the fuzzy sets assigned to each output

variable are combined together to form a single fuzzy set for each output variable. This operation is made by different methods that are cited as the inference method max-min, max-product and sum-product. Each of these methods uses a special digital processing operator of fuzzy logic [97].

II.2.6.3 Aggregation of the rule outputs

The third step in the fuzzy logic model is the aggregation, which is the process of unification of the outputs of all rules. In other words, we combine the membership functions of all rule consequents into a single fuzzy set. Thus, the input of the aggregation process is the list of consequent membership functions, and the output is one fuzzy set for each output variable. Figure II.21 illustrates how the output of each rule is aggregated into a single fuzzy set for the overall fuzzy output.

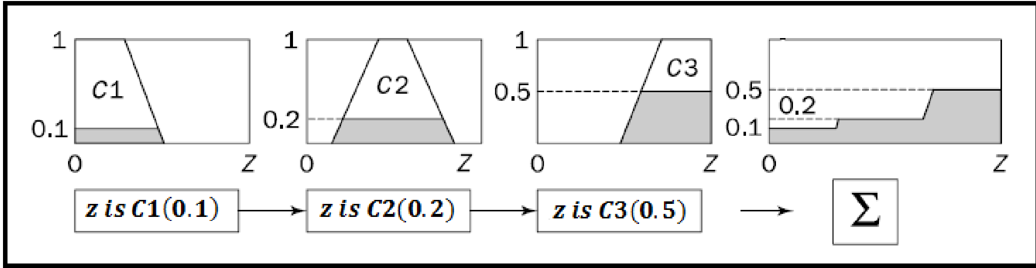

Figure II.21: Aggregation of rule consequents step diagram.

II.2.6.4 Defuzzification

Defuzzification, also known as fuzzy decoding, is the last step in the fuzzy logic model, which involves the process of transposing the inferred fuzzy output set into a crisp (non-fuzzy) number as shown in Figure II.22.

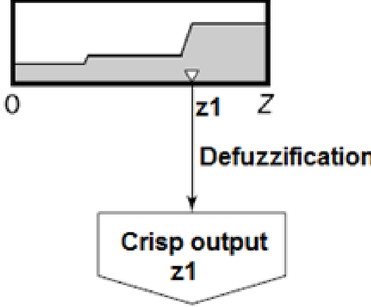

Figure II.22: Diagram of the defuzzification step.

In other words, the input for the defuzzification process is the aggregate output fuzzy set and the output is a single number. All through this step, the deduction of the digital

output data is obtained from the fuzzy inference in order to calculate the value of a digital output variable using a set of rules according to the degrees of membership in all fuzzy sets of the input variables and the fuzzy sets of the output variable.

There are many defuzzification strategies used to defuzzify the aggregate fuzzy set, such as:

- ✓ Center of gravity or (centroid principle).
- ✓ Maximum value method (height method).
- ✓ Average maximums method (mean-max membership) [98, 99].
- ✓ First (or last) maxima.
- ✓ Center of sums.
- ✓ Center of largest area.
- ✓ Weighted average method.

II.3 Artificial Neural Networks

The human brain gives proof of the existence of massive neural networks that can be successful at those cognitive, perceptual, and control tasks in which humans are unbeaten. The human brain is also capable of computationally demanding perceptual acts for example recognition of faces, speech, in addition of its capability to control activities such as body movements and body functions. The human brain includes more than 10 billion interconnected neurons and nearly 60 trillion connections, called synapses, between them [100]. The brain can perform its functions in a very fast manner by its effective use of massive parallelism which means by using multiple neurons simultaneously, the highly parallel computing structure, and the imprecise information-processing capability.

An artificial neural network can be defined as a model of reasoning based on the human brain.

II.3.1 Biological Neuron

Each neuron is a cell which has a very simple structure, as illustrated in Figure II.23. This cell uses biochemical reactions to receive, process, and transmit information.

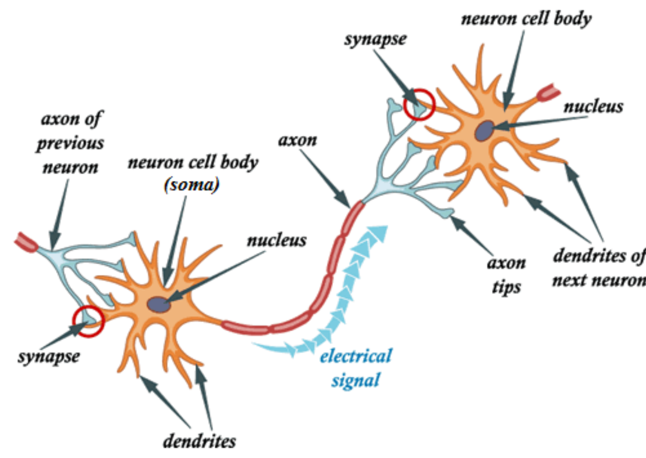

Figure II.23: Biological nervous cell (the neuron).

A huge number of such elements constitutes a terrific processing power. Treelike receptive networks of nerve fibers called *dendrites* that carry electrical signals into the *neuron cell body* or *soma*, where the *cell nucleus* is located. The *soma* effectively sums and thresholds these incoming signals. A single long fiber extending from the *cell body* is called the *axon* that carries the signal from the cell body out to other neurons, which eventually branches into strands and substrands, and is connected to other neurons through synaptic terminals or *synapses.* The biological nervous cell is illustrated in Figure II.23.

II.3.2 Artificial Neuron (The Perceptron)

The basic processing element of the neural network is called artificial neuron, which is also simply named neuron, node, and perceptron. Invented in 1957 by Frank Rosenblatt at the Cornell Aeronautical Laboratory, an Artificial Neuron is the simplest neural network possible which is a computational model of a single neuron. A perceptron consists of one or more inputs, a processor, and a single output. Figure II.24 represents the perceptron.

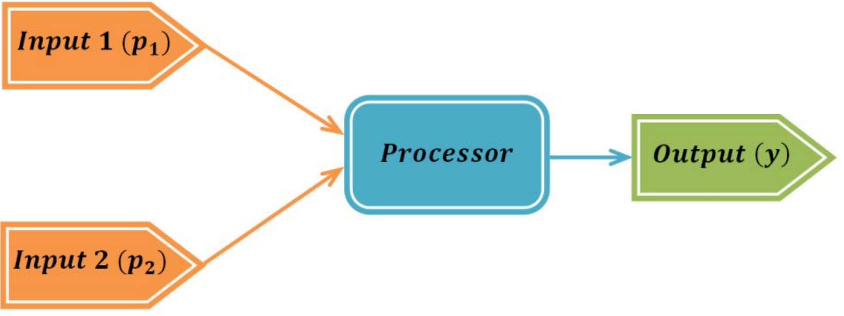

Figure II.24: Artificial Neuron (Perceptron).

An Artificial Neuron follows the "feed-forward" model, which means that inputs (p_1, p_2) are sent into the neuron, where they are processed, and result in an output (y). In *Figure II.24* this means the network (in our case it posses' only one neuron) reads from left (inputs side) to right (output side): inputs come in, output goes out.

These steps can be presented in the following Algorithm.

Algorithm of Artificial Neuron

1. Multiply every input by its corresponding weight.

2. Sum all of the weighted inputs.

3. Compute the output of the perceptron based on that sum passed through an activation function.

In what follow we explain each of these steps in more detail using a simple example.

1-First Step: Receive inputs

Considering that our artificial neuron has two inputs: p_1 and p_2

Let us say: $p_1 = 8$ and $p_2 = 6$

2-Second Step: Weight inputs

Each input that is sent into the neuron must first be weighted, in other words, multiplied by some value. When creating an Artificial Neuron, we will typically begin by affecting random weights. For instance, let us give the inputs (p_1, p_2) the following weights:

$w_1 = -0.25$

$w_2 = +1$

In this simple model, each of the scalar input is multiplied by its own scalar weight to form, one of the terms that are sent to the summer.

$p_1 \times w_1 = 8 \times (-0.25) = -2$

$p_2 \times w_2 = 6 \times 1 = 6$

3-Third Step: Sum inputs

In this step, we simply add together the weighted inputs.

$sum = -2 + 6 = 4$

4- Forth Step: Generate the output

Generating the output is the last step in the algorithm. In this step the summer output, often referred to as the net input, goes into a “transfer function” or “activation function”, which produces the scalar neuron output y. Let us choose the hard limit transfer function as our activation function which is a simple transfer function, if the sum is a positive number, the output is 1; if it is negative, then the output is 0.

$$y = Hardlim(4) = 1$$

In literature, we distinguish two types of artificial neurons namely Single-Input Perceptron and Multi-Input Perceptron.

II.3.2.1 Single-Input Perceptron Model

Figure II.25 illustrates a single-input perceptron. In this simple model, the perceptron has only one input.

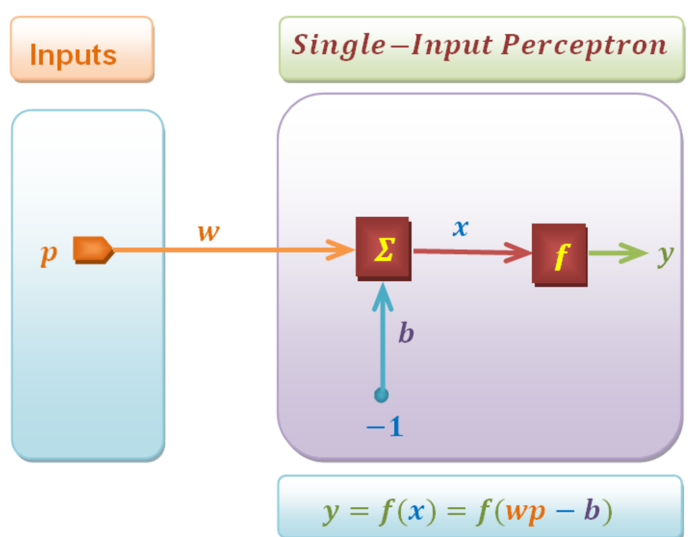

Figure II.25: Single-Input Perceptron Model.

The *perceptron* output y is calculated as

$$y = f(wp - b) \tag{II.8}$$

The value of y which is the actual output depends on the transfer function used.

II.3.2.2 Multiple-Input Perceptron Model

Typically, a perceptron has more than one input. A neuron with n inputs is shown in Figure II.26. The individual inputs $p_1, p_2, \dots p_n$ are each weighted by corresponding elements $w_{1,1}, w_{1,2}, \dots w_{1,n}$ of the weight matrix W.

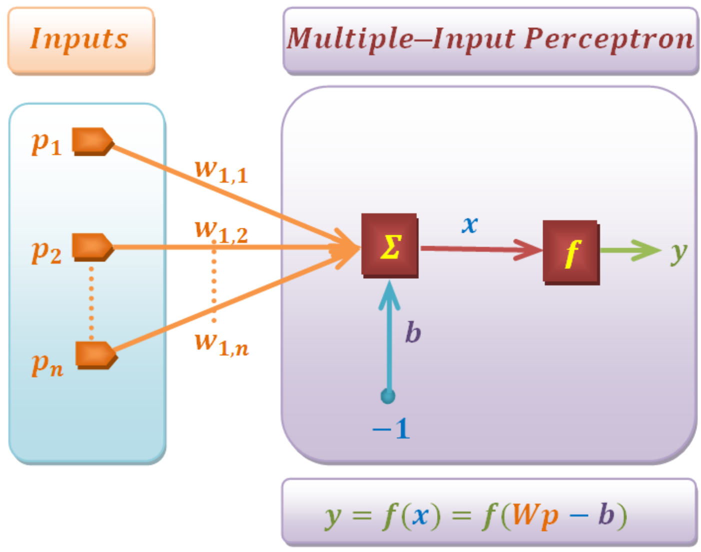

Figure II.26: Multiple-Input Perceptron Model.

The neuron has a bias, which is multiplied by -1 then summed with the weighted inputs to form the net input :

$$x = w_{1,1}p_1 + w_{1,2}p_2 + \cdots + w_{1,n}p_n - b \tag{II.9}$$

The matrix form of this expression can be written as

$$x = Wp - b \tag{II.10}$$

note that for the single neuron case the matrix W has only one row.

finally, the output y of the perceptron can be written as

$$y = f(x) = f(Wp - b) \tag{II.11}$$

Note that W and b are both adjustable parameters of the perceptron. Typically the transfer function is chosen by the designer and then the parameters W and b will be adjusted by some learning rule so that the relationship between the inputs and the output of the perceptron meets a very specific goal. As described in the following section, we have different transfer functions for different purposes.

II.3.3 Transfer Functions

In Figure II.26 the activation function could be a linear or a nonlinear function of x. A particular activation function is chosen to satisfy some specification of the problem that the perceptron is attempting to resolve.

In Table II.1 most of the activation functions used in the literature are summarized. Of course, we can find other activation functions in addition to those shown in Table II.1.

Table II.1: Common Activation Functions for Perceptrons y = f(x).

The name of the function	Input/Output Relation	Icon
Hard Limit	$y=0$ if $x<0$ $y=1$ if $x\geq 0$	
Symmetrical Hard Limit	$y=-1$ if $x<0$ $y=1$ if $x\geq 0$	
Linear	$y=x$	
Saturating Linear	$y=0$ if $x<0$ $y=x$ if $0\leq x\leq 1$ $y=1$ if $x>1$	
Symmetric Saturating Linear	$y=-1$ if $x<-1$ $y=x$ if $-1\leq x\leq 1$ $y=1$ if $x>1$	
Positive Linear	$y=0$ if $x<0$ $y=x$ if $x\geq 0$	
Log-Sigmoid	$y=\frac{1}{1+e^{-x}}$	
Hyperbolic Tangent Sigmoid	$y=\frac{e^{x}-e^{x}}{e^{-x}+e^{x}}$	
Competitive	$y=1$ if neuron with max x $y=0$ all other neurons	C

A variety of transfer functions have been included in literature. Three of the most commonly used functions namely hard limit, linear, and log-sigmoid activation function are discussed in this section.

Figure II.27a illustrates the input/output characteristic of a single-input perceptron that uses a hard limit transfer function. Here we can see the effect of the weight and the bias. In this case, the input/output relationship is determined according to the expression

$$y = hardlim\ (w^T p - b) \quad \text{(II.12)}$$

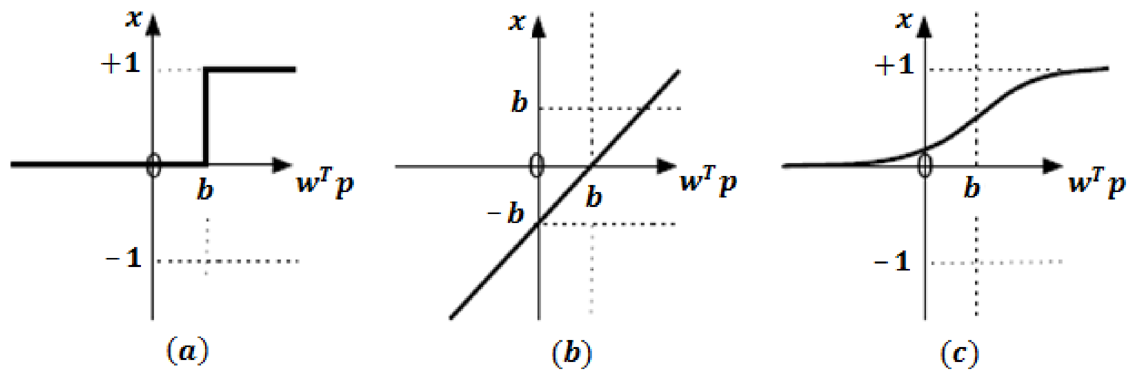

Figure II.27: Transfer function: (a) hard limit; (b) linear, and (c) log-sigmoid.

The linear function is very simple, it directly affects its input to its output:

$$y = x \quad \text{(II.13)}$$

Applied in the context of a neuron, this function is illustrated in Figure II.27b. In this case, the output of the neuron corresponds to its activation level whose transition to zero occurs when $w^T p = b$.

The log-sigmoid transfer function is illustrated in Figure II.27c. It resembles either the hard limit or the linear function, depending on whether we are far or near b, respectively. This transfer function takes the input (which may have any value between plus and minus infinity) and squashes the output into the range 0 to 1, according to the expression:

$$y = \frac{1}{1+e^{-x}} \quad \text{(II.14)}$$

II.3.4 Network Architectures

It is well known that only one neuron, even with many inputs, may possibly not be good enough. We might need a sufficient number of neurons, operating in parallel, in what we call a “layer.” This concept of a layer is discussed in the next section. The architecture of

an artificial neural network defines how its various perceptrons are organized, or placed, in relation to each other. These arrangements are structured essentially by directing the synaptic connections of the perceptrons.

II.3.4.1 A Layer of Neurons

A number of neurons or perceptrons that are classed together are considered as a Layer. Note that rarely a layer can contain only one neuron. A single-layer network of neurons is shown in Figure II.28. From this figure, it can be seen that each of the inputs is connected to each of the neurons and that the weight matrix now has rows.

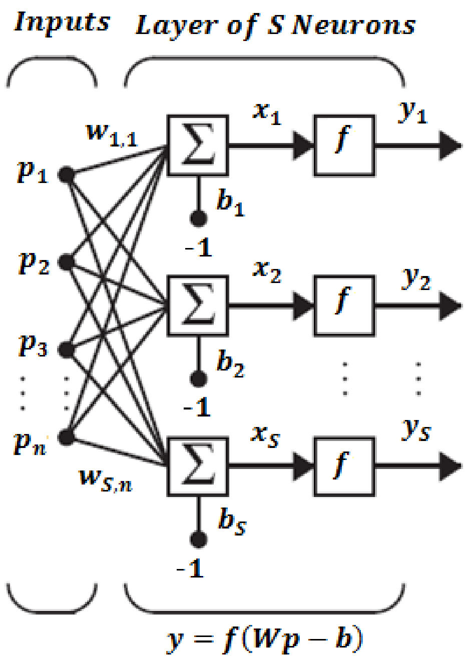

Figure II.28: A Layer of Neurons.

It is clearly shown that each element of the input vector $[p_1, p_2, p_3, \dots p_n]$ is connected to each neuron through the weight matrix W. Each neuron has his own bias, summer, transfer function and his own output.

As mentioned before taken together, the layers form an artificial neural network, each layer should be one of the following types of layers: (i) Input layer, (ii) Hidden layer, or (ii) Output layer.

1. Input layer

This layer is the first layer in the architecture of any Artificial Neural Networks and it is responsible for receiving data (information), signals, features, or measurements. These

inputs data are usually normalized within the limit values produced by activation functions. This normalization results in better numerical precision for the mathematical operations performed by the network.

2. Hidden Layers

Hidden layers, also known as intermediate, invisible, or middle layers, are composed of neurons which are responsible for extracting patterns associated with the processor system being analyzed. These layers perform most of the internal processing from a network.

3. Output layer

This layer is also composed of neurons and thus is responsible for producing and presenting the final network outputs, which result from the processing performed by the neurons in the previous layers.

The main architectures of artificial neural networks, considering the neuron disposition, as well as how they are interconnected and how its layers are composed, can be divided as follows: (a) single-layer feedforward network, (b) *non-deep neural network*, (c) d*eep neural network*, (d) recurrent network, and (e) mesh network. In what follow we explain each of these types of networks in more detail.

II.3.4.2 Single-Layer Feed-forward Architecture

We can find no hidden layer in this type of artificial neural network architecture; it has just one input layer and a single neural layer, which is also the output layer. Figure II.29 outlines a single-layer feed-forward network composed of n inputs $[p_1, p_2, \dots p_n]$ and m outputs $[y_1, y_2, \dots y_m]$.

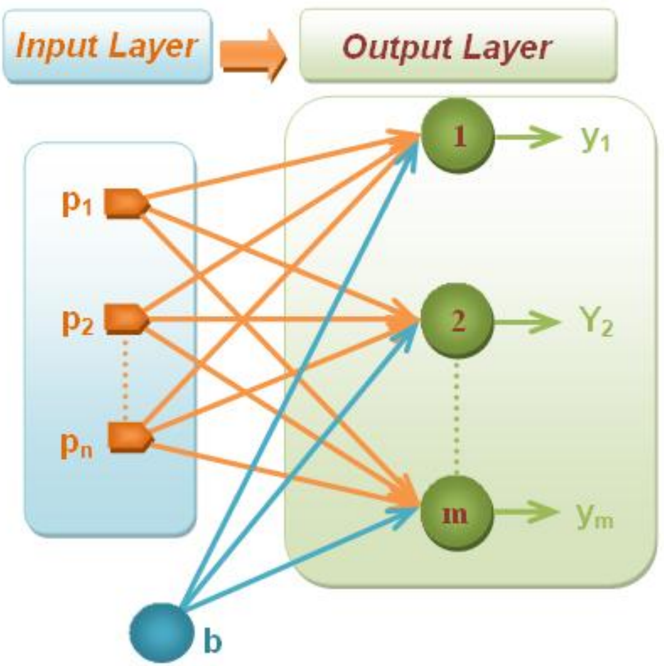

Figure II.29: Single-Layer Neural Network Architecture.

In this neural network architecture information always flows in a single direction (thus, unidirectional), which is from the input layer to the output layer.

II.3.4.3 Multiple-Layer Feed-forward Architectures

Conversely to the networks belonging to the precedent architecture, Multiple-layer feed-forward architectures are composed of one or more hidden neural layers. The number of hidden layers determines two well-known types of neural network architectures namely non-deep neural network (one hidden layer) and deep neural network (more than one hidden layer).

II.3.4.3.1 Non-deep Neural Network Architecture

Non-deep neural network architecture, also known as simple neural network architecture is an architecture which contains only one hidden layer in addition to the input and output layer. Such architecture is depicted in the following figure.

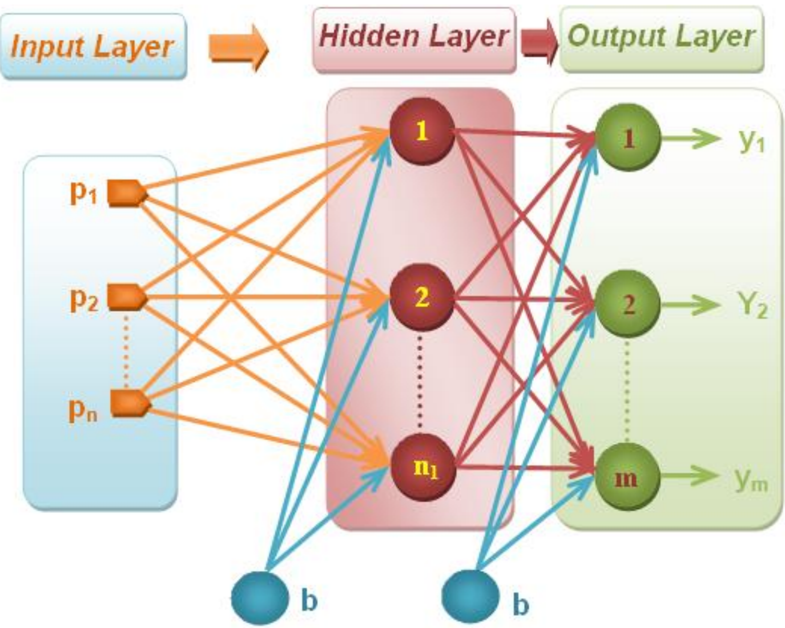

Figure II.30: Non-deep (simple) Neural Network Architecture.

II.3.4.3.2 Deep Neural Network Architecture

By contrast, deep neural network architecture is an architecture which contains at least two hidden layers. *Figure II.31* gives an example of deep neural network architecture with three hidden layers.

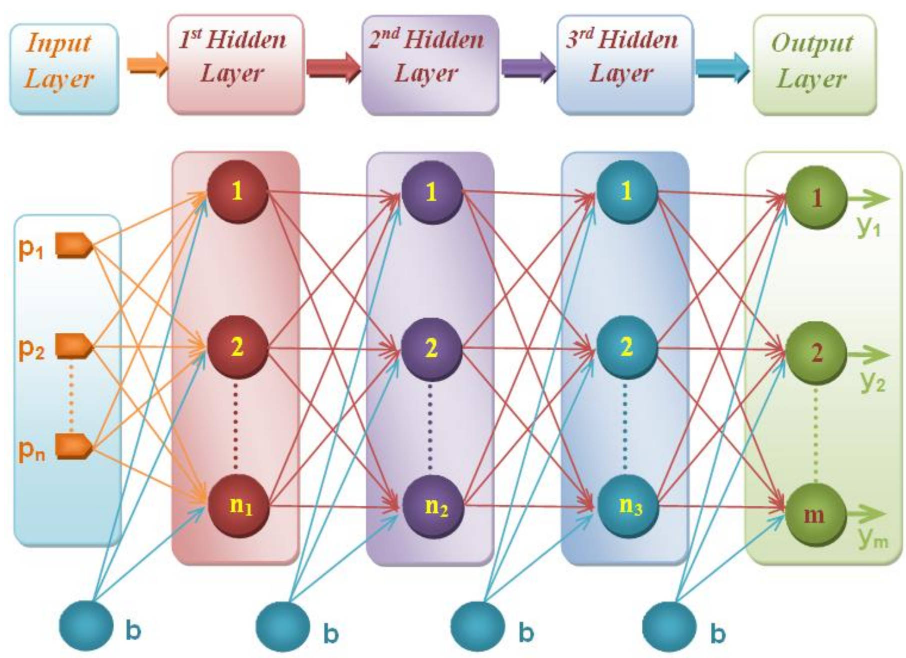

Figure II.31: Deep Neural Network Architecture.

As shown in Figure II.31 and as an example, this d*eep neural network architecture is formed from three* hidden layers, also it can contain only two hidden layers or more than three layers.

II.3.4.4 Recurrent or Feedback Architecture

Contrary to feed-forward networks, recurrent networks contain feedback connections. As illustrated in figure II.32 the outputs of the neurons in this class of network architecture, are used as feedback inputs for other neurons belonging to the hidden layers. The feedback characteristic qualifies these networks architectures for dynamic information processing, which means that they can be utilized on time-variant systems, for instance, process control, system identification and optimization, time series prediction, and so on.

Figure II.32 depicts an example of network architecture with feedback, where one of its output signals is fed back to the hidden layer.

Thus, using the feedback process, the networks with this architecture produce current outputs also taking into consideration the previous output values.

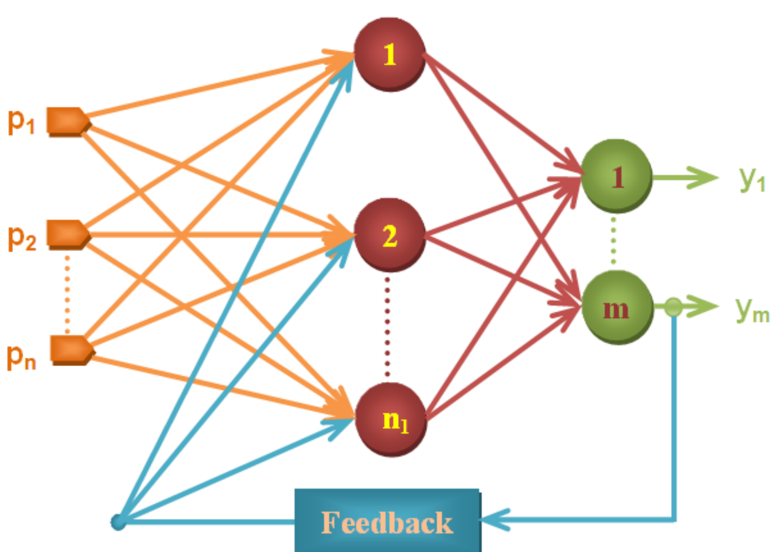

Figure II.32: Example of a Recurrent Network.

II.3.4.5 Mesh Architecture

Figure II.33 outlines an example of mesh network architecture. From this figure, it is conceivable to check that in this network class, the several input signals are perused by all neurons inside the network.

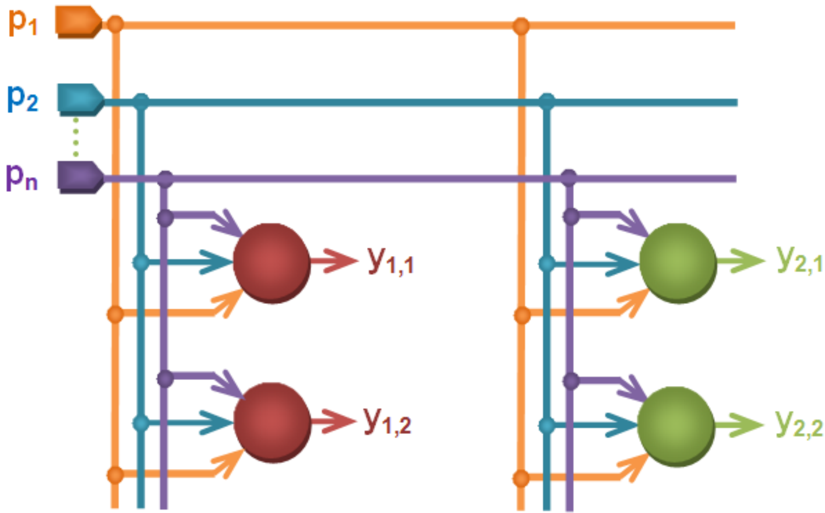

Figure II.33: Example of a mesh network.

The fundamental highlights of networks with mesh structures reside in considering the spatial arrangement of neurons for pattern extraction purposes, that is, the spatial localization of the neurons is directly related to the process of adjusting their synaptic weights and thresholds. These networks serve a wide range of applications and are used in problems involving data clustering, pattern recognition, system optimization, graphs, and so on.

There are several other neural network architectures which are mentioned in literature, for instance, competitive networks, adaptive resonance theory maps, Elman network, and so forth, depending on the properties and requirement of the application.

II.3.5 Training Processes and Properties of Learning

It is well known that artificial neural networks are able to learn from the presentation of samples (patterns), which expresses the behavior of the system. This ability of learning is one of the most relevant of its features. Therefore, after the network has learned the relationship between inputs and outputs, it can generalize solutions, which means that for any given input values the network can generate the desired (expected) set of outputs. Several methods to set the strengths of the connections exist. One way is to set the weights explicitly, using a priori knowledge. Another way is to train the neural network by feeding it teaching patterns and letting it change its weights according to some learning rule. The learning situations in neural networks may be classified into three distinct sorts. These are supervised learning, unsupervised learning, and reinforcement learning.

II.3.5.1 Supervised Learning

The training data consist of a set of training examples. In supervised learning strategy, each training sample is a pair composed of the input signals and their corresponding responses, in other words, at the inputs an input vector is presented at the same time with a set of desired outputs, one for each node, at the output layer. Therefore, it requires a table with input/output data, also called attribute/value table, which describes the process and its behavior. It is from using this information that the neural structures will formulate "hypothesis" about the system being learned.

In this case, the efficiency of supervised learning depends only on the availability of that input/output data, and it behaves as if a "teacher" is training the artificial network what is the right answer for each sample offered for its input. The term supervised originates from the fact that the desired signals on individual output nodes are provided by an external teacher.

A forward pass is done, and the errors or discrepancies between the desired and actual response for each node in the output layer are found. These are then used to determine weight changes in the net according to the prevailing learning rule.

In fact, the supervised learning is a typical case of pure inductive inference, where the free variables of the network are adjusted by knowing a priori the desired outputs for the investigated system.

II.3.5.2 Unsupervised Learning

Unlike the supervised learning paradigm, the utilization of an algorithm based on unsupervised learning (or self-organization) does not necessitate any knowledge of the respective desired outputs.

Thereby, the network needs to organize itself when there are existing particularities between the elements that compose the entire sample set, identifying subsets (or clusters) presenting similarities. The learning algorithm adjusts the synaptic weights and thresholds of the network in order to reflect these clusters within the network itself.

Otherwise, the network designer can specify (a priori) the maximum quantity of these possible clusters, using his knowledge about the problem.

II.3.5.3 Reinforcement Learning

Reinforcement learning is learning what to do – how to map situations to actions – so as to maximize a numerical reward signal. The learner is not told which actions to take, as in most forms of machine learning, but instead must discover which actions yield the most reward by trying them. In the most interesting and challenging cases, actions may affect not only the immediate reward, but also the next situation and, through that, all subsequent rewards. These two characteristics, trial-and-error search, and delayed reward are the two most important distinguishing features of reinforcement learning.

II.4 Genetic algorithm (introduction)

Evolutionary Computing (EC) is considered one of the four typical components of soft computing as we have seen in section II.1 and also as it is illustrated in Figure II.1 and perhaps the newest yet possibly most up-to-date is that of Evolutionary Algorithms. Genetic algorithm and as we can see from Figure II.34 is a part of evolutionary computing, which is a rapidly growing area of soft computing. The concept of evolutionary computing was invented by I. Rechenberg in his work “Evolution strategies (ES)” in the 1960s. Alternatively, Fogel in 1962 offered a new method for simulating evolution as a phenotypic process, this method is known as Evolutionary programming (EP). Genetic Algorithm was invented to imitate some of the processes observed in natural evolution. The father of the original Genetic Algorithm (GA) was John Holland who invented it in the early 1970's and developed by him and his students and colleagues in 1970. In 1992 John Koza has used a genetic algorithm to develop programs to accomplish particular tasks. He named his method genetic programming (GP). All these techniques GP, ES, and EP share the same underlying principles with GAs [101]. The development history of evolutionary computing and genetic algorithm just described is summarized in Figure II.34.

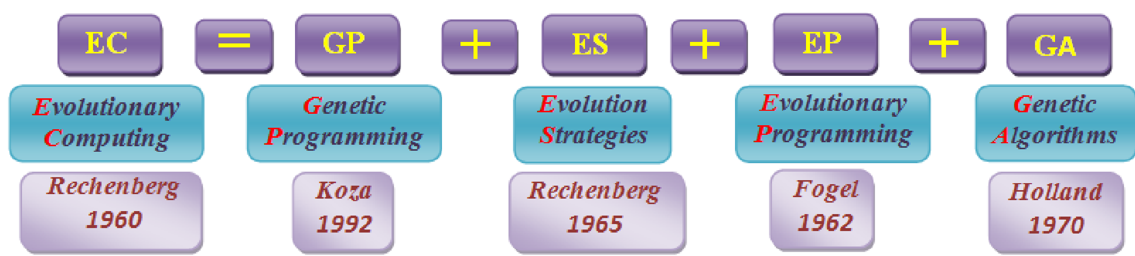

Figure II.34: Development history of Evolutionary Computing.

Genetic algorithms (GAs) are powerful techniques for solving optimization problems, furthermore, they provide to soft computing an efficient mechanism for solving difficult problems through a systematic stochastic search based on the principles of natural selection.

A genetic algorithm has been applied to a variety of problems, many of which conventional methods have failed to solve when the Genetic algorithm can effectively solve these and other hard problems.

II.4.1 Biological Background and notation

Genetic algorithms (GAs) very closely resemble the biological model of *chromosomes* and *genes*. All living organisms consist of cells. In every single cell, there is the same *set of chromosomes*. *Chromosomes* are strings of deoxyribonucleic acid (DNA), which serve as a model for the whole organism. A *chromosome* consists of *genes*. Each *gene* encodes a particular protein that represents a *trait*, for example, color of eyes. Possible settings for a trait (e.g. blue, brown) are called *alleles*. Each *gene* has its own position in the chromosome. This position is called *locus*. Complete *set of all chromosomes* is called *genome* and a particular set of genes in the genome is called *genotype*.

During reproduction, first occurs *recombination* (or *crossover*). *Genes* from parents form in some way the whole new *chromosome*. The newly created *offspring* can then be *mutated*. *Mutation* means, that the elements of DNA are a bit changed. These changes are mainly caused by errors in copying genes from parents.

The *fitness* of an organism is measured by the success of the organism in its life.

II.4.2 Basic concept

Genetic algorithms (GAs) are inspired by Darwin's theory of evolution and genetic. As genetic algorithms are modeled after these processes we found that the building blocks of the algorithms are named after genetic elements. That’s why Genetic algorithms contain a chromosome, a gene, a set of population, fitness, fitness function, mutation, and selection.

As can be seen from Figure II.35 genes are the binary encoding of each problem variable, and all of the genes as a string (8 genes) are referred to a chromosome or individual. A set of chromosomes is called a population which contains the necessary information about the individuals in our case n chromosomes (n individuals).

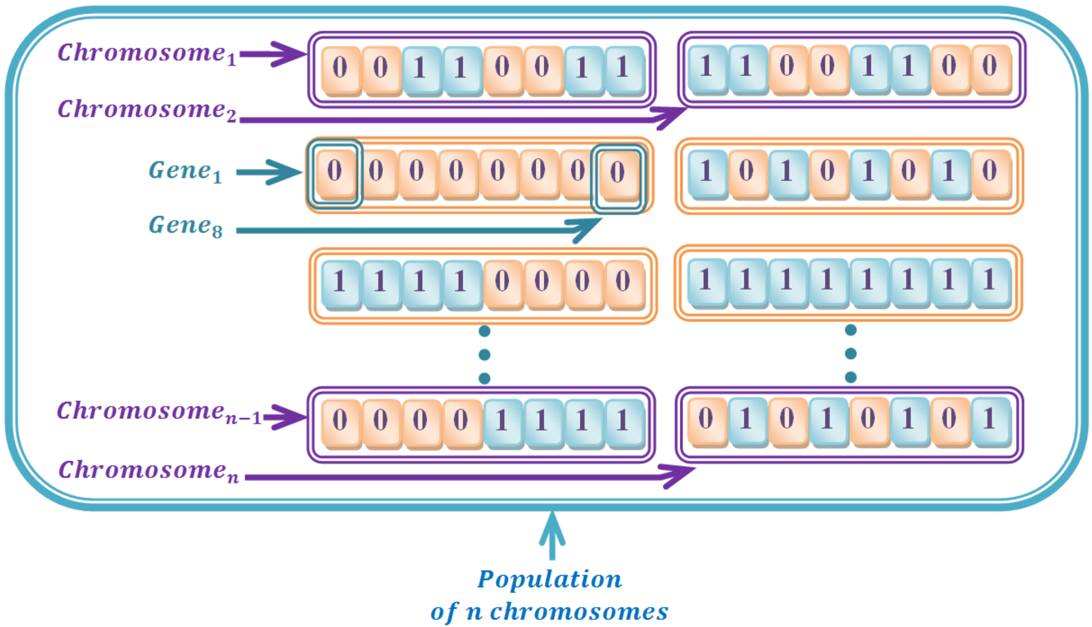

Figure II.35: Representation of the basic elements of GA.

Genetic algorithms (GAs) start with a randomly generated set of solutions represented by chromosomes, named population. Solutions from one population are selected and used to generate a new population, which is motivated by the hope that the new population will be better than the old one. Further, solutions are selected according to their fitness to form new solutions, that is, offspring (or individuals). This process is repeated until some condition is satisfied. Algorithmically, a canonical genetic algorithm (also called simple or standard GA) [102] is an algorithm which utilizes binary representation, one-point crossover, and bit-flipping mutation. A simple genetic algorithm is outlined as below:

Algorithm II.41 Simple genetic algorithm

1. Randomly initialize a population of n chromosomes $(x_1, x_2, \dots, x_n)$;

2. Determine the fitness of each individual chromosome: $f(x_1), f(x_2), \dots, f(x_n)$

3. Create a new population by repeating the following steps;

a. Select two parent chromosomes from a population according to their fitness using fitness function;

b. Crossover the parents to form a new offspring. If no crossover was performed with a crossover probability (P_c), offspring is an exact copy of parents (clone);

c. Mutate new offspring at a locus (position in cthe hromosome) with a mutation probability (P_m);

d. Place the new created offspring chromosomes in the new population

4. Until the new population is complete (rich n chromosomes);

5. Use newly generated population for a further run of the algorithm;

6. Until the termination criterion is satisfied.

7. Stop, and return the best solution in current population

From this Simple genetic algorithm, it can be seen that there are many things that can be implemented differently in various issues, for instance how to create chromosomes and choose the type of encoding.

The genetic algorithm is started with a randomly generating of an initial **set of solutions** which is also known as individuals who are represented by **chromosomes,** this set of solutions is called **population**. Solutions from one population are selected and used to generate a new population. Solutions which are chosen to form new solutions (**offspring**) are chosen according to their fitness which is calculated through a fitness function. This process is repeated until one condition is satisfied (for instance number of populations or improvement of the best solution).

Figure II.36 outlines the flowchart of a basic genetic algorithm.

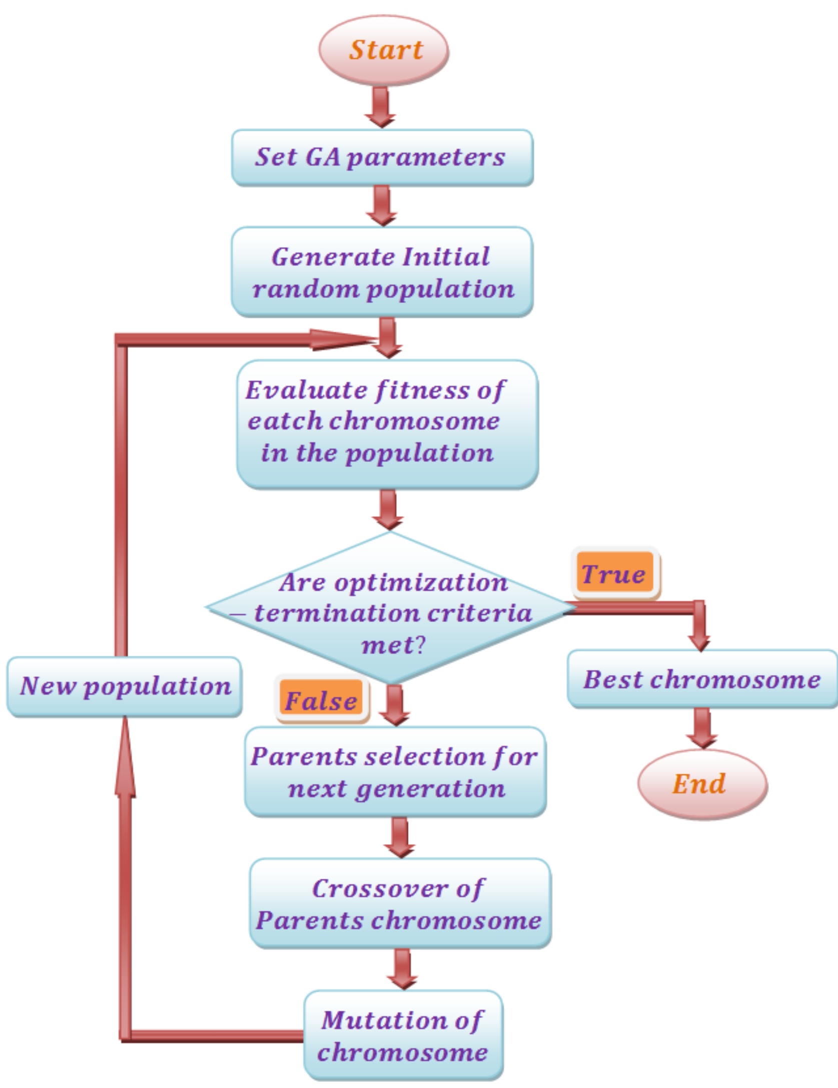

Figure II.36: Simple genetic algorithm flowchart.

II.4.3 Encoding technique

In some way, the chromosome should contain information about a solution which it represents. Since the most used way of encoding is a binary string, there must be a process of converting continuous values into binary, and vice versa. In this context, each variable in the optimization problem must be coded as a gene, and all variables concatenated together to form a chromosome. For example, the sample chromosome illustrated in Figure II.37 is composed of S parameters and each parameter is composed of three binary digits.

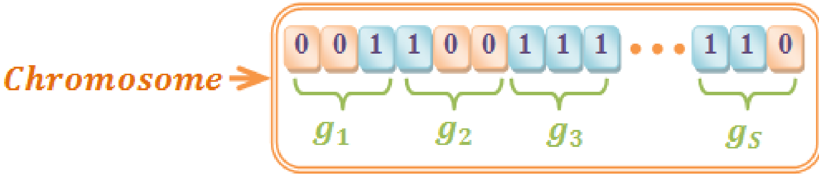

Figure II.37: Chromosome representation with S parameters composed of three binary digits each.

In this figure, it is clearly shown that each gene g_i has a mapping from the chromosome space to the parameter space. In the encoding technique t,he chromosome must first be decoded in order to be evaluated by the fitness function since the GA works with the binary encodings but the fitness function often requires continuous variables.

II.4.4 Evaluating fitness

Evaluating the fitness of each chromosome in the genetic algorithm is the most important step, and the fitness is calculated through a fitness function. The fitness function measures the quality of the solutions that the Genetic Algorithm has generated. The fitness function must assign a number to each solution that is a measure of the goodness of the present individual in relation to the optimization goals. The success of the algorithm is dependent on how well the fitness function evaluates each chromosome in relation to the overall objectives of the optimization problem. The fitness function is generally the most time-intensive part of a genetic algorithm, so it is also important when considering the time efficiency of the optimization algorithm, in other words, the performance of a Genetic Algorithm in solving a problem is usually measured in terms of the number of required fitness function evaluations until the optimum is found or approximated with the desired accuracy. Minimizing the number of fitness function calls is very important. To summarize, the choice of the fitness function in Genetic Algorithm is a crucial design objective.

II.4.5 Selection operators

The key idea in selection operator also known as selection technique or selection scheme is to give priority to better individuals, allowing them to pass on their genes to the next generation by crossover and mutation. Many selection algorithms are based on randomness. In order to search for increasingly better individuals, fitter individuals should have higher probabilities of being selected on the contrary unfit individuals should

have less probability to be selected. Several methods of calculating selection probability exist. The commonly used techniques for selection of chromosomes are roulette wheel selection, rank-based selection, and tournament selection.

II.4.5.1 Roulette wheel selection

Roulette wheel selection is also known as fitness proportional selection selects parental solutions randomly with uniform distribution, this algorithm uses the fitness value of each individual to determine its selection probability and assigns it to the corresponding individual in the population based on relative fitness values [103]. Figure II.38 illustrates roulette wheel for six solutions having different fitness values. And also shows how solutions are assigned a space on the wheel that is directly related to their relative fitness. For example the fourth individual (x_4) has a higher fitness than any other, it is expected that the Roulette wheel selection will choose the fourth solution (x_4) more than any other solution. On the other hand, it can be seen that there is still a small probability for the sixth solution (x_6) with the smallest fitness value will be selected for the mating process, thus maintaining its genetic information and preserving a higher level of diversity.

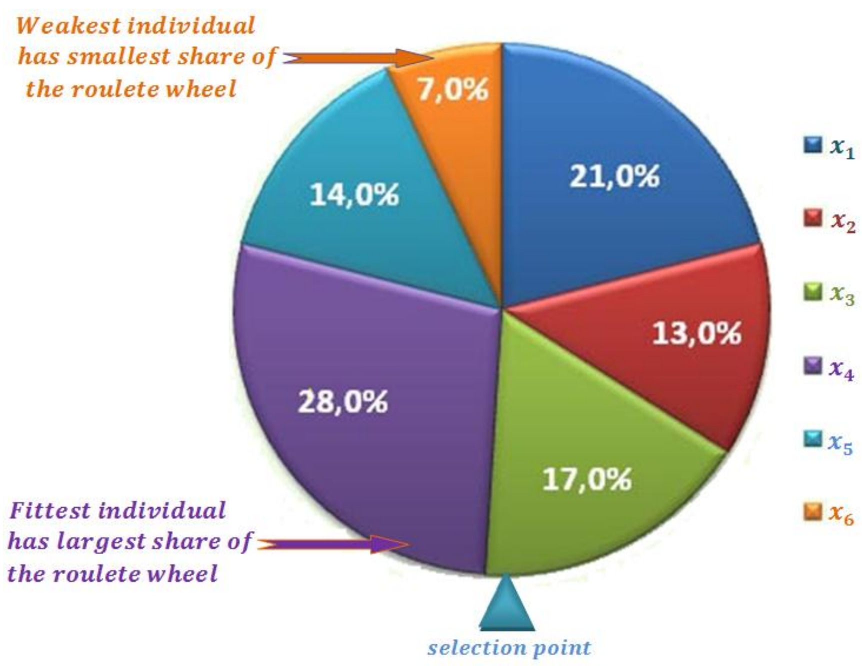

Figure II.38: Roulette wheel technique.

II.4.5.2 Rank-based selection

In this method, we select the chromosomes which are ranked from highest to lowest based on their fitness [103]. The rank selection first ranks the population according to their fitness and then every chromosome receives a ranking. The worst will have fitness 1, the second worst will have a fitness of 2, and the best one will have a fitness value n, where n is the number of chromosomes in the population. The remaining individuals are randomly paired to produce offspring and create the next generation.

II.4.5.3 Tournament selection

Tournament selection is another famous selection operator, where a set of solutions (sub-population of n chromosomes) is selected randomly and within this competition subset, the chromosome with the highest fitness value wins the tournament and is chosen as a parent in the mating pool. All the sub-population individuals are returned to the general population and the process repeats until the mating pool is full. Tournament selection scheme acts much as roulette wheel selection, with the more fit individuals having a higher probability of selection while still maintaining the diversity of the population. The advantages of the tournament selection technique are the non-existence of fitness ranking, which makes it a faster process than roulette wheel selection and offers a positive probability for each solution to survive, even if it has worse fitness values than other solutions.

II.4.6 Crossover operators

Crossover in a GA with crossover probability P_c selects genes from parent chromosomes and creates a new offspring. The crossover operator depends on the crossover probability P_c. For instance, if we assume that the crossover probability value is $P_c = 0.8$ which means that the probability that the crossover occurs is 80%, i.e. 80% of the new individuals are generated from two selected parents through the crossover process and 20% percent for them are clones of their parents. As shown in Figure II.39 the offspring C_i is a clone of the parent P_i i.e. both are identical.

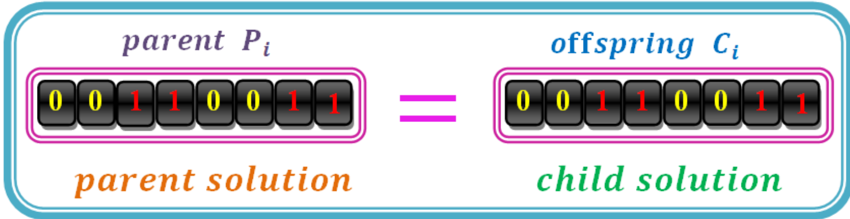

Figure II.39: Example of cloning.

There are several variations of crossover. In binary encoding, the chromosomes may crossover at a single point, two-point, uniformly or arithmetically.

II.4.6.1 Single point crossover

In Single point crossover [104] a random single crossover location in the parent's chromosome is selected and the data before this point are exactly copied from $parent_1$ to $child_1$ and from $parent_2$ to $child_2$ and the data after this point are exactly copied from $parent_1$ to $child_2$ and from $parent_2$ to $child_1$, as shown in Figure II.40.

Figure II.40: Single point crossover.

II.4.6.2 Two-point crossover

Multi-point crossover is an extension of single point crossover, where two or more crossover points are selected in the parent chromosome, in the case of two-point crossover the data between the two points are exactly copied from $parent_1$ to $child_2$ and from $parent_2$ to $child_1$ and the data out the two points are exactly copied from $parent_1$ to $child_1$ and from $parent_2$ to $child_2$. Figure II.41. illustrates an example of a two-point crossover just explained.

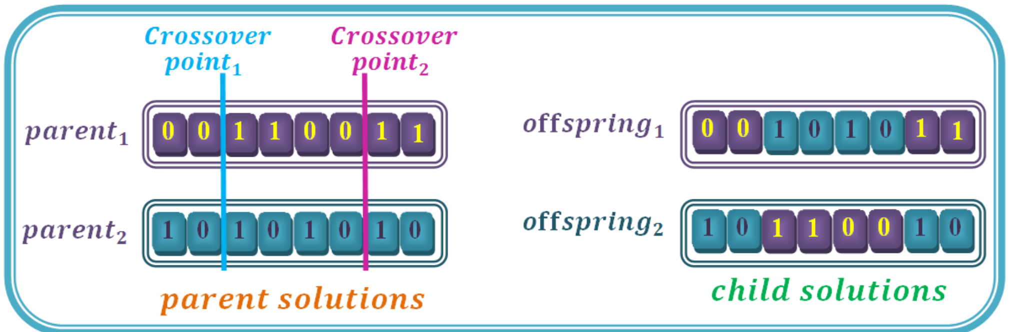

Figure II.41: Example of multi-point crossover with two crossover points.

II.4.6.3 Uniform crossover

In uniform crossover [104] a mask that contains the same number of genes as the parent chromosomes are randomly generated. The Boolean numbers (1 *and* 0) in the mask indicate whether the bit from $parent_1$ or $parent_2$ should be translated to each $child$. Figure II.42 illustrates an example of uniform crossover, where a 0 in the mask indicates for $child_1$ that the bit should taken from $parent_1$ and a 1 indicates that the bit should be taken from $parent_2$. The reverse is true for $child_2$.

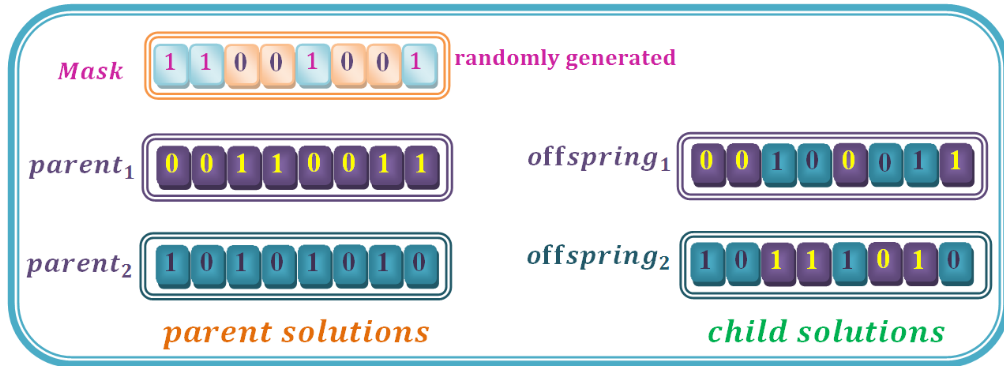

Figure II.42: Uniform crossover.

II.4.6.4 Arithmetic crossover

Figure II.43 shows an *example of arithmetic crossover*, where the crossover of chromosomes is performed by AND and OR operators to create new offspring.

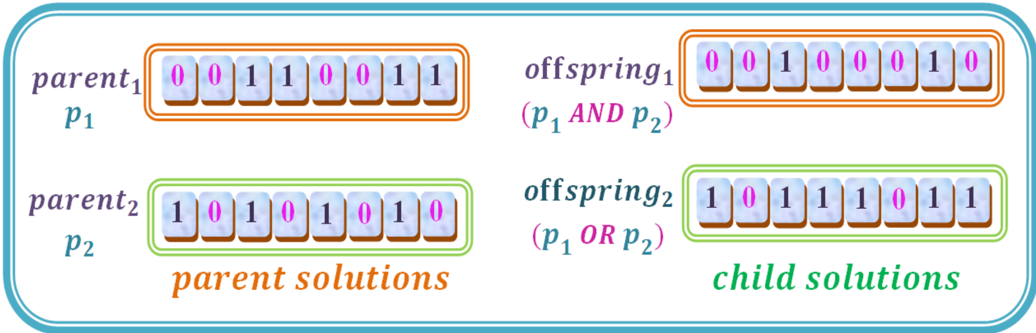

Figure II.43: Example of Arithmetic crossover.

II.4.7 Mutation operators

After a crossover is performed, mutations take place. They are used for the purpose of maintaining diversity within the population and prevent premature convergence. The mutation changes randomly the new chromosome at the bit level and happen by changing a randomly chosen bit from "1" to "0" or from "0" to "1" as illustrated in Figure II.44. The mutation operator depends on the mutation probability P_m: If the random number which is generated randomly by GA in the interval [0, 1] is less than the predetermined mutation rate, then muthe tation is applied and vice versa. Mutation rates used in lithe terature are usually very small (e.g. 0.001) [105].

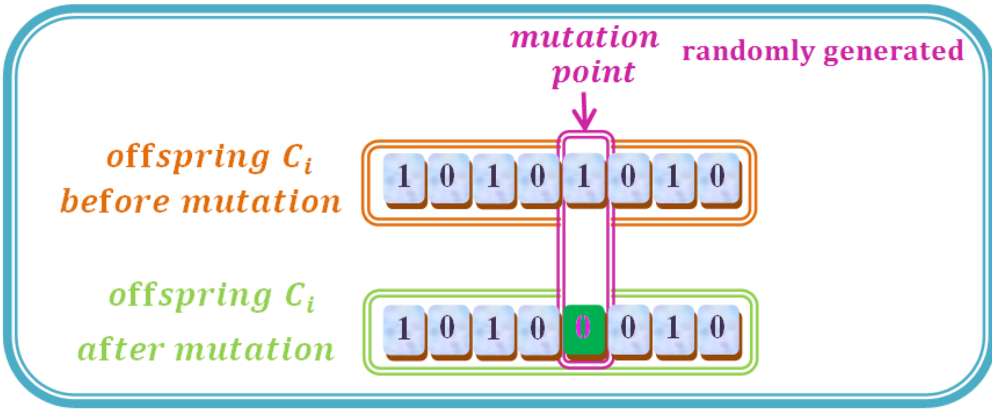

Figure II.44: Mutation operator.

The aim of mutation operator is to introduce new genetic structures in the population, helping the search algorithm to escape from local optimum by reaching new points in the search space.

II.4.8 Replacement operators

A genetic algorithm operates on a population of constant size. An initial population is randomly generated. Once the new offspring are created via genetic operators, the need for replacement takes place. During replacement operation, the current generation of individuals is replaced by newly generated offspring using the specific replacement strategy in other words replacement strategy helps to find out the individuals that would replace the current generation to form next generation of the population. The most common replacement schemes are generational replacement, steady-state replacement, and Elitism replacement scheme.

• In generational replacement scheme, the entire population of genomes is replaced at each generation. It means all the individuals of the successor population are deleted and replaced with the same number of newly generated individuals. Two consecutive generations are non-overlapping using generational replacement.

• Steady-state scheme replaces few individuals in each generation. Only a small number of newly created offspring are put in place of the least fit individual. The main idea of steady-state selection is that larger part of chromosome should retain to the successive population.

• In case of Elitism scheme, the complete population is replaced except one or two individuals with the highest fitness are chosen to be included in the next generation without modification.

II.4.9 Convergence criteria

The convergence criteria also are known as stopping conditions and termination condition are a list of criteria that, if only one of them is satisfied, will ensure that the algorithm eventually finds the optimal solution in infinite time. The common GA convergence criteria can be listed as follows:

• The fitness function value must be below a given threshold value.

• Number of Iterations: It is the number of generations of the sample population, the genetic algorithm stops when the specified number of iterations have evolved. This prevents the algorithm from spending too much time refining an existing solution.

• The difference between the best and the average fitness is less than a given fraction of the fitness of the average individual.

• No change in fitness: If the difference between the best individual of the current population and the best individual so far must be very small the genetic process will end.

II.5 Hybrid Soft Computing

In previous three sections, we considered three *independent and distinct* soft computing techniques that are fuzzy logic, neural networks, and genetic algorithms. We investigated these three techniques individually. And we can notice that in human nature and also in real-world applications we would require not only to obtain knowledge from various sources but also to combine different intelligent techniques. The need for such a combination has led to the appearance of hybrid soft computing.

Hybridization of intelligent systems using soft computing techniques has been identified as a promising research field of computational intelligence. Voire II.5.2

A hybrid soft computing is one that combines at least two soft computing techniques. For instance, combining a neural network with genetic algorithms results in a hybrid genetic neural networks system.

The combination of several independent algorithms forms the core of soft computing, an emerging approach to building hybrid soft computing technique capable of reasoning and learning in an uncertain and imprecise environment.

II.5.1 Hybridization rules

It is reputed that Lotfi A. Zadeh has said that a good hybrid would be 'British Police, German Mechanics, French Cuisine, and Swiss Banking'. But 'British Cuisine, German Police, French Banking, and Swiss Mechanics' would be a bad one. Similarly, a hybrid soft computing can be good or bad, it depends on which components add up to the hybrid algorithm. So to build a good hybrid soft computing is to select the right components and put them in the right place in the algorithm.

Each independent technique has its own strengths and weaknesses.

- Fuzzy logic is mainly addressed with imprecision or vagueness in input and output,

- Neural networks mimic the human to adapt to circumstances and the ability to learn from past experiences,
- The genetic algorithm can systemize random search and for optimum characteristics.

To design a good hybrid algorithm is to choose the advantages of these techniques and put them together in the right manner. A comparison of different soft computing techniques in term of strengths and weaknesses is summarized in Table II.2.

The terms used for grading in Table II.2 are: bad, rather bad, rather good and good

Table II.2: Comparison of fuzzy logic (FL), neural networks (NN) and genetic algorithms (GA).

The name of the soft computing technique	Fuzzy Logic	Neural Networks	Genetic Algorithms
Knowledge representation	good	bad	rather bad
Uncertainty tolerance	good	good	good
Imprecision tolerance	good	good	good
Adaptability	rather bad	good	good
Learning ability	bad	good	good
Explanation ability	good	bad	rather bad
Knowledge discovery and data mining	rather bad	good	rather good
Maintainability	rather good	good	rather good

It is therefore appropriate that hybridization of these three techniques is done so as to surmount the weakness of one using the strength of the other.

II.5.2 Possibilities of integrating two techniques

It is entirely necessary to investigate the alternatives of integrating any two techniques, in order to exploit the preferred strength of both types of techniques to produce improved results. For instance and in order to facilitate this investigation we will take Fuzzy logic and ANN as the two techniques to hybrid. To combine these two techniques to work together competitively and/or cooperatively there are three possibilities:

1. The first possibility is known as an auxiliary hybrid system, it can be realizable if the task in hand can be divided broadly into two parts, one part are problems need qualitative modeling and other parts are problems need quantitative modeling.

The qualitative work is done using fuzzy logic and quantitative work is done by ANN. As illustrate in Figure II.45 both of these two techniques work together in cooperation. In other words, one technology calls the other technology as a subroutine.

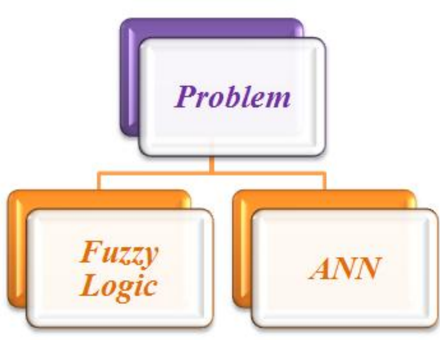

Figure II.45: Auxiliary hybrid system with Fuzzy Logic and ANN.

2. The second possibility is known as a sequential hybrid system, where Fuzzy Logic work at a higher level in the hierarchy and neural networks execute the inferior level computations as illustrate in Figure II.46. We can also identify that the two techniques are used in a pipelining manner.

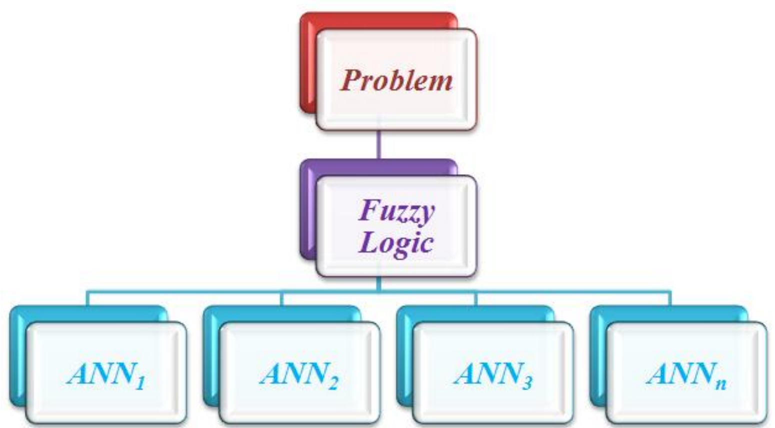

Figure II.46: Fuzzy Logic and ANN working in a hierarchal manner.

3. The third possibility is emerging Fuzzy Logic and ANN techniques; it exists two ways to do this task:

(a) One way is by neuralizing fuzzy systems, i.e. the introduction of neural network concepts in fuzzy systems. Technically, it may be realized by mapping out fuzzy systems into the neural network as illustrated in *Figure II.47a*.

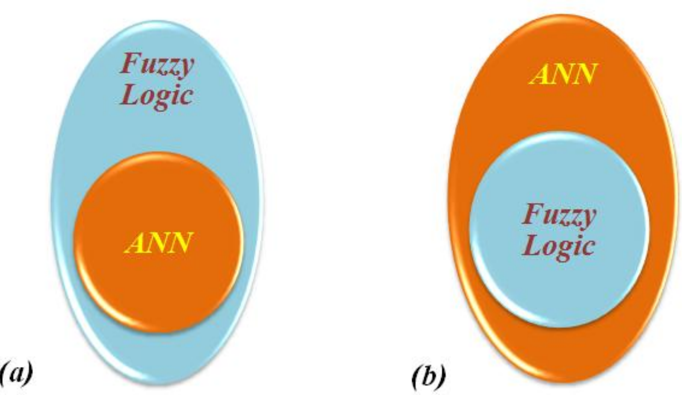

Figure II.47: Emerging Fuzzy Logic and ANN techniques: (a) Neuralizing the Fuzzy Logic (b) Fuzzifying ANN.

(b) The other way is by fuzzifying neural networks by introducing fuzzy logic in neural networks as illustrated in *Figure II.47b*. The fuzzy neural networks retain the basic properties and architecture of the neural network and simply fuzzify some of their elements.

Note that these three possibilities for combining techniques just investigated are applicable for all hybridization, and it's the role of the designer to choose the best one for obtaining good results.

II.5.3 Neuro-fuzzy systems

Neuro-fuzzy systems are the hybridization of the two techniques Neural Network and Fuzzy Logic, where we combine elements from FL and NN. This idea of hybridization originates from two observations:

1. Fuzzy Systems are neither capable of learning, adaptation or parallel computation, whereas these characteristics are clearly attributed to NNs.

2. NNs lack flexibility, human interaction, interpretability or knowledge representation, which lies at the core of FL.

There are two ways to do hybridization:

- One is to provide NNs with fuzzy capabilities, thereby increasing the network's expressiveness and flexibility to adapt to uncertain environments.

- Second, is to apply neural learning capabilities to fuzzy systems so that the fuzzy systems become more adaptive to changing environments. This method is called NN driven fuzzy reasoning.

II.5.4 Adaptive Neuro-Fuzzy Inference Systems (ANFIS)

In this hybrid technique, we combine both artificial neural network and fuzzy logic. The resulting hybrid technique is named Adaptive Neuro-Fuzzy Inference Systems (ANFIS) will be investigated in details in chapter V where it is chosen as our tool to predict the lifetime of the Gate All Around Junctionless cylindrical MOSFET (GAA JL MOSFET) device.

II.6 Conclusion

In this chapter, the reader is introduced to various soft computing techniques namely Fuzzy Logic (FL), Artificial Neural Network (ANN), and Genetic Algorithm (GA) which they are well explained. These soft computing techniques were mainly designed to model and perform solutions to complex problems, which are not yet modeled or too difficult if it is not imposible to model, mathematically. SC techniques have gained increasing attention over the past years due to their suitability for problem solving and also provide flexible information processing that are capable to handle real-life confusing situations.

This chapter is an essay to understandd common concepts and general building blocks used in diverse individual techniques as well as hybrid (combined) techniques. Each independent technique has its own strengths and weaknesses, and therefore the selection of the techniques (in the case of independent techniques) and the selection of the suitable elements to combine (in the case of hybrid techniques) strongly depends on the problem to be solved. Despite the variousness of the huge availability of independent and hybrid techniques, in this modest dissertation Genetic Algorithm will be used as an individual tool in chapter III to optimize a new Double Gate Junctionless ($DGJL$) $MOSFET$ device, by contrast ANN and F,L will be combined together to form a new hybrid technique namely Adaptive Neuro-Fuzzy Inference System ($ANFIS$) which is used as a predictor of lifetime of a new $JL\ GAA\ MOSFET$ device.

Chapter III: New DGJL MOSFET design to improve analog/RF performance

III.1 Introduction

The scaling of CMOS-based technology faces important challenges to control the short channel effects (SCEs) and limits the further reduction of MOSFET dimension. The short channel effects can degrade both analog and Radio Frequency (RF) performance and energy consumption of the device. Therefore, these SCEs should be removed, or at least reduced in order to improve the device performance. A number of new architectures have been reported to mitigate these effects. In this context, Double Gate (DG) MOSFET design is considered, by the International Technology Roadmap for Semiconductors (ITRS)[5], as a promising candidate for deep submicron applications due to its higher drive current capability, better Drain Induced Barrier Lowering (DIBL), better scaling capability and effective SCEs handling capability as two gates control the channel from both sides [106-110]. Nevertheless, despite the actual stage of maturity of DG MOSFET devices at the deep submicron level, several parasitic effects still persist that affect the device performance, especially for analog and RF applications. In fact, some problems are closely related to the formation of p-n junctions between the source/drain extensions and the channel. For these junctions, some suggestions in terms of doping profile and shape need to be satisfied during the fabrication procedures. In this context, the elaboration of abrupt p-n junctions using extremely high doping concentration gradients can be a difficult task in experimental techniques available at present, such as flash annealing [111]. Recently, Junctionless MOSFET has been aggressively driven into deep submicron scales in order to reach the desired enhancement in fabrication process cost [111-114]. The idea behind this design is based on the suppression of the doping concentration gradient between source/drain regions (n^{++}) and the channel (p) region, so a uniform type doping is obtained, which avoids the establishment of junctions. Numerous experimental studies have demonstrated the superior fabrication process properties of the junctionless device in comparison with the conventional one [111,116,117], but still, a lot of improvements are required for their applications in high performance digital and analog/RF applications. One of the key areas in improving the performance of the junctionless transistor is the development of new modified designs to improve the drain current driving capability and remove the dramatic increase in the series resistance effect. This effect is achieved by reducing the temperature during the fabrication process which means that this problem is a difficult problem to overcome even at room temperature. Therefore, new designs and comprehensive models of double gate junctionless (DGJL)

MOSFET are required in order to improve the device performance, especially for analog/RF applications, in which the high drain current and low series resistance values are required. These aspects have been extensively treated in the literature due to their importance in a wide range of circuit applications [118-120]. In this context, several studies have been reported to investigate and improve the DGJL MOSFET performance [112-117,121-124]. However, to the best of our knowledge, no design approach based on the junctionless aspect and device global optimization was reported to improve the device performance for analog and RF applications.

This chapter presents two stage investigation frameworks of a new long channel DGJL MOSFET design dedicated to deep submicron RF and analog circuit applications. It should be mentioned that two promising features are adopted in this structure namely the gate material engineering and the drain/source extension paradigms. As a first step, compact models for the proposed long channel device associated to the drain current, analog and RF parameters (cut-off frequency, intrinsic gain, drain current drivability, transconductance, transconductance-to-drive current ratio and linearity characteristics) are deduced from the solution of Poisson's equation including the adequate boundary conditions. The impact of dual-material gate engineering and two highly doped extension regions on the analog/RF performance of DGJL MOSFET is supported through the gate work function and the bulk voltage variables. The obtained results have been validated against the data obtained from TCAD software simulations for a wide range of design parameters [125]. In the second step, the developed analytical models are used in the context of a genetic algorithm based approach as a weighted sum mono-objective function to optimize the device analog/RF performance. The comparison held with respect to other structures (inversion-mode (IM), and conventional junctionless devices) shows clearly that our proposed design outperforms significantly the other two counterparts, where the proposed design exhibits excellent ability in improving the analog/RF performance and provides improved figures-of-merit. This result makes the proposed design a potential candidate to push further the miniaturization procedure deeper to the nanoscale level.

III.2 Modeling methodology

Figure III.1 shows schemas for the DGJL MOSFET devices without and with our design modification. For the conventional DGJL MOSFET, the channel body and the source/drain extensions are uniform highly doped regions, which are denoted by $n^+/n^+/n^+$. By contrast, the proposed device consists of a gate with dual-material (DM) regions and drain/source extensions. These extensions are both highly doped regions compared with that of the channel body; thus, the doping concentration distribution is given by $n^{++}/n^+/n^{++}$. In this work, we are considering a long channel structure, which means that Poisson equation reduces to the 1-D problem. Moreover, quantum transport and confinement effects are not considered in this investigation, since the quantum effects start to become more apparent with silicon film thickness smaller than 5 nm [126]. It is to note that the proposed design is a feasible technique from a practical viewpoint because it only involves one ion implantation step for the S/D extensions. Moreover, the work-function value for both gate materials can be controlled by adjusting the doping level of each poly-silicon gate region.

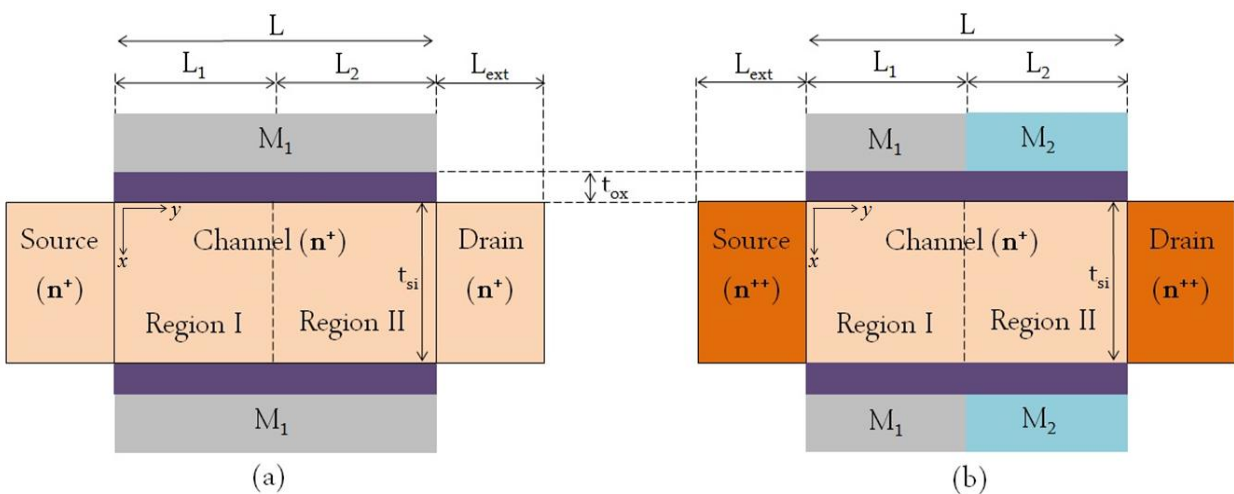

Figure III.1: Cross-sectional view of (a) DGJL MOSFET without extensions and gate material engineering (b) DGJL MOSFET with extensions and gate material engineering.

III.2.1 Drain current model

Poisson equation for an n-type device, with a doping impurity concentration N_d is given by

$$\frac{d^2\Phi}{dx^2} = \frac{qN_d}{\varepsilon_{si}}\left(exp\left(\frac{\Phi(x)-V}{V_t}\right) - 1\right) \qquad \text{(III.1)}$$

where $\Phi(x)$ represents the electrostatic potential through the x direction (see Figure III.1), ε_{Si} is the silicon permittivity, q is the electron charge, $\Phi(x)$ is the thermal voltage and V is the potential shift across the silicon film, from the source $V_S\ (y=0)=0V$ to the drain $V_D\ (y=L)$

In our proposed design, the boundary conditions for $\Phi(x)$ under the condition of zero electric field at the middle of the semiconductor film $(x=\frac{t_{si}}{2})$, can be given as

$$\Phi(0)=\Phi_0 \quad \text{(III.2-a)}$$

$$\left.\frac{d\Phi}{dx}\right|_{x=\frac{t_{Si}}{2}}=0 \quad \text{(III.2-b)}$$

where Φ_0 is the potential at the center of the silicon layer. By integrating Eq. (III.1) from x=t_{si}/2 to x=0 and using the appropriate boundary conditions we can find

$$\left[\frac{d\Phi}{dx}\right]^2=\frac{2qN_dV_t}{\varepsilon_{si}}\left(exp\left(\frac{\Phi_s-V}{V_t}\right)-exp\left(\frac{\Phi_0-V}{V_t}\right)-\frac{\Phi_s-\Phi_0}{V_t}\right) \quad \text{(III.3)}$$

Where Φ_s represents the surface potential.

To get the solution of Poisson equation in depletion and accumulation modes, an approximation should be made in order to simplify the resolution of this equation. In this context, we suggest assuming a parabolic potential profile in the semiconductor, which is an accurate presentation in full depletion mode. However, this potential profile is considered as an approximation presentation for the accumulation mode, where several works have used this approximation to investigate the accumulation mode [113]. Thus, using the appropriate boundary conditions and after some mathematical manipulations the potential profile can be found as

$$\Phi(x)=\frac{\Phi_s-\Phi_0}{\left(\frac{t_{si}}{2}\right)^2}\left(x-\frac{t_{si}}{2}\right)^2+\Phi_0 \quad \text{(III.4)}$$

To calculate the mobile charge we need to apply Gauss theorem around the silicon film at x=0 (oxide/silicon interface) as follows:

$$\left.\frac{d\emptyset}{dx}\right|_{x=0}=\frac{Q_m-\frac{Q_{fix}}{2}}{\varepsilon_{si}} \quad \text{(III.5)}$$

where the fixed charge density is calculated from $Q_{fix} = 2qN_d t_{si}$, $Q_i = 2\varepsilon_{si} V_t / t_{si}$.

So, using Eq. (III.4) and Eq. (III.5) we can find the following relationship

$$\frac{\emptyset_s - \emptyset_0}{V_t} = \frac{\emptyset_m - \frac{Q_{fix}}{2}}{2Q_i} \tag{III.6}$$

In this stage we can exploit the charge based model developed in Ref. [113], the motivation behind the exploitation of the model developed in Ref. [113] rather than other several models presented in other published work [112,114,115] is that we can obtain an accurate, simple and compact model for the drain current. This latter can easily be used to formulate our objective function, which will be explored for our metaheuristic optimization of the device performance. In this context, according to [113], we assume a parabolic potential profile in the x-direction and a Gaussian distribution profile of the mobile charge centered in the middle of the channel, the mobile charge in a sub-threshold regime where $\emptyset_s < \emptyset_0$, can be obtained by integrating Boltzmann's distribution as follows

$$\mathrm{Q_m} = \frac{1}{2}\sqrt{\pi \mathrm{Q_{fix}} \mathrm{Q_i}} \exp\left(\frac{\emptyset_\mathrm{s} - \emptyset_0}{\mathrm{V_t}}\right) \tag{III.7}$$

So, Eq. (III.6) becomes

$$\frac{\emptyset_s - \emptyset_0}{V_t} = \frac{\left(\sqrt{\pi Q_{fix} Q_i} exp\left(\frac{\emptyset_s - \emptyset_0}{V_t} - \frac{Q_m}{2Q_i}\right)\right) \emptyset_m - \frac{Q_{fix}}{2}}{2Q_i} \tag{III.8}$$

It is clearly seen in this equation that if the accumulation mode is considered Eq. (III.8) will be reduced to Eq. (III.6). Thus, Eq. (III.8) seems to be quite reasonable for both operating regimes accumulation and depletion.

So, using the solution provided by the first integration of Poisson's equation and Eq. (III.8), we can find an implicit equation of the total mobile charge density for both sub-threshold and above threshold regimes. Hence, the total mobile charge can be written, after some mathematical manipulations, as

$$Q_m = Q_{fix} Q_i \frac{1 - \mathrm{C} \exp\left(\frac{t_{si}\left(Q_m - \frac{Q_{fix}}{2}\right)}{4\varepsilon_{si} V_t}\right)}{Q_m - \frac{Q_{fix}}{2}} exp\left(\frac{\Phi_s - V}{V_t}\right) \tag{III.9}$$

The parameter C is a constant depending mainly on different charges in the device. This latter is given by

$$C = 1 + \sqrt{\pi \frac{Q_{fix}}{4Q_i}} \frac{1}{2\left(1+\frac{Q_e}{2Q_i} ln\left(\exp\left(\frac{Q_{fix}}{4Q_i}\right)+1\right)\right)} \quad \text{(III.10)}$$

Using appropriate boundary conditions for the symmetrical case, the surface potential Φ_s, can be given as

$$\Phi_s = V_{gs} - V_{FB} - \frac{Q_m - \left(\frac{Q_{fix}}{2}\right)}{C_{ox}} \quad \text{(III.11)}$$

where V_{gs} is the applied gate voltage, C_{ox} represents the oxide capacitance which is given by $C_{ox} = \varepsilon_{ox}/t_{ox}$, with t_{ox} and ε_{ox} are the oxide thickness and the oxide permittivity, respectively.

Substituting Eq(III.9), in Eq(III.11) and using the same methodology presented in Ref. [113], we obtain the mobile charge inside the channel for both accumulation and depletion modes $Q_m(V)$. This latter is given as an implicit function, which can be solved using Lambert function $LW(z)$:

$$LW(z) = \ln(1+z)\left(1 - \frac{\ln(1+\ln(1+z))}{2+\ln(1+z)}\right) \quad \text{(III.12)}$$

$$Q_m(V) = Q_e LW\left[\frac{KC}{Q_e} \frac{\exp\left(\frac{Q_{ma}(V)}{2Q_i}\right) - \left(C \exp\left(\frac{Q_{fix}}{4Q_i}\right)\right)}{Q_{ma}(V) - \frac{Q_{fix}}{2} - 2Q_i \ln(C)} exp\left(\psi(V)\right)\right] \quad \text{(III.13)}$$

where $Q_{ma}(V)$ denotes the mobile charge for the accumulation mode, which can also be calculated using the Lambert function as

$$Q_{ma}(V) = C_{ox} V_t LW\left[\frac{K exp\left(\psi(V)\right)}{C_{ox} V_t} \frac{1 - \exp\left(\frac{\frac{Q_{fix}}{2} - C_{ox} V}{2Q_i} ln\left(\exp\left(\psi(V)\right)+1\right)\right)}{C_{ox} V_t ln\left(\exp\left(\psi(V)\right)+1\right) - \frac{Q_{fix}}{2}}\right] \quad \text{(III.14)}$$

with

$$K = Q_{fix} Q_i \quad \text{(III.15)}$$

$$Q_e = \frac{2Q_i C_{ox} V_t}{2Q_i + C_{ox} V_t} \quad \text{(III.16)}$$

$$\psi(V) = \left(V_{gs} + V_{FB} + \frac{Q_i}{C_{ox}} + V\right)/V_t \tag{III.17}$$

where V_{FB}, is the flat-band voltage, which is given by

$$V_{FB} = \phi_{ms} + V_t ln\left(\frac{N_d}{n_i}\right) \tag{III.18}$$

which is depending on ϕ_{ms} (the difference between the silicon and gate work functions).

Refer to Figure III.1, the boundary conditions at the source and drain sides are given, respectively, by:

$$V(y = 0) = V_{bi} \tag{III.19a}$$

$$V(y = L) = V_{bi} + V_{ds} \tag{III.19b}$$

where V_{ds} is the applied drain-source voltage and V_{bi} represents the built-in potential. which is given by

$$V_{bi} = V_t ln\left(\frac{N_{dext}}{N_d}\right) \tag{III.20}$$

where N_{dext} represents the source/drain extensions doping concentration.

Considering the drift-diffusion model, the drain current for each value of V_{gs} can be calculated by the integration of the mobile charge Q_m between the two values of drain and source bias $V_2 = V_{ds} + V_{bi}$ and $V_1 = V_{bi}$, respectively.

$$I_{ds} = \frac{2W\mu_n V_t}{L}\int_{V_1}^{V_2} Q_m dV \tag{III.21}$$

where μ_n denoted as the electron mobility in the silicon channel region, is mainly depending on the channel doping concentration and it can be expressed as

$$\mu_n = \mu_{min} + \left(\frac{\mu_{max} - \mu_{min}}{1+\left(\frac{N_d}{N}\right)}\right) \tag{III.22}$$

Where $\mu_{max} = 1400,\ \mu_{min} = 68.8$ are the maximum and the minimum silicon mobility, respectively, $\alpha = 0.71$ and $N = 9.2.10^{16}$.

By assumption that $V_s = V_1,\ V_D = V_2$, and after calculating the integral given in Eq. (III.21), in which the mobile charge for both subthreshold and above threshold regimes is given by Eq. (III.14), a compact analytical expression for the drain current is given as

$$I_{ds} = \frac{2W\mu_n V_t}{L}\left(F(V_{bi}) - F(V_{bi} + V_{ds})\right) \tag{III.23}$$

where $F(V_{bi})$ and $F(V_{bi}+V_{ds})$ can be found by substituting $V=V_1$ and $V=V_2$, respectively, in the following analytical equation

$$F(V)=\frac{Q_m(V)^2}{2Q_e}+2Q_m(V)-Q_m(V)ln\left(1+\exp\left(\frac{Q_m(V)-\frac{Q_{fix}}{2}}{2CQ_i}\right)\right)$$

$$+Q_{fix}\ln\left(\frac{Q_m(V)-\frac{Q_{fix}}{2}}{4Q_i\left(\exp\left(\frac{Q_m(V)-\frac{Q_{fix}}{2}}{4Q_i}\right)-1\right)}\right) \quad \text{(III.24)}$$

A dual material gate aspect used in the proposed device with S/D extensions can be modeled as two sub-devices connected in series, with two different material work functions ϕ_{M1} and ϕ_{M2}. So, the flat-band voltage, for each transistor should be different and they are given by

$$Q_e=\frac{2Q_iC_{ox}V_t}{2Q_i+C_{ox}V_t}$$

$$V_{FB1}=\phi_{MS1}+V_t ln\left(\frac{N_d}{n_i}\right) \quad \text{(III.25)}$$

and

$$V_{FB2}=\phi_{MS2}+V_t ln\left(\frac{N_d}{n_i}\right) \quad \text{(III.26)}$$

Using Eq. (III.21) and the appropriate boundary conditions for each region, the drain current expressions can be given as

$$I_{ds1}=\frac{2W\mu_n V_t}{L_1}(F_1(V_{bi})-F_1(V_p)) \quad \text{(III.27a)}$$

$$I_{ds2}=\frac{2W\mu_n V_t}{L_2}(F_2(V_p)-F_2(V_{ds}+V_{bi})) \quad \text{(III.27b)}$$

where V_p represents the interface potential between two elementary transistors and $F_1(V)$, $F_2(V)$ are found by substituting the flat-band by V_{FB2} and V_{FB1}, respectively, in Eq. (III.24). For the second elementary transistor (near to the drain side), the applied gate voltage should be taken equals to $V_{gs}-V_p$.

Hence, to calculate V_p we need to apply the continuity of the drain current at the interface between both regions, $I_{ds1}-I_{ds2}$, then resolving numerically the nonlinear resulted

equation. Thus, a new drain current model which includes the gate-engineering aspect and the S/D extensions can be developed.

III.2.2 Analog/RF parameter models

After calculating the channel voltage V_p between the two gate-materials, we can easily calculate the drain current of the device and the transconductance, which is an important parameter to evaluate the analog/RF device performance. This latter can be derived by differentiating the drain current with respect to V_{gs} as

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=cst} \tag{III.28}$$

If we suppose that an output conductance load of *r=20 KΩ* is affected to both DMDGJL MOSFET without and with S/D extensions devices, we can simply calculate the intrinsic gain which is an essential parameter to characterize the analog performance as follows

$$A_v = g_m r \tag{III.29}$$

The cut-off frequency of both DMDGJL MOSFET with and without S/D extensions can be computed based on the transconductance, and the oxide capacitance using the formula

$$f_c = \frac{g_m}{2\pi C_{ox}} \tag{III.30}$$

The nonlinearity of transistor results causes harmonic distortion and useful output power pert. So, we need to model the non-linearity characteristics of our proposed device to estimate the impact of the gate engineering aspect and the S/D extensions on the device RF behavior (linearity performance). To do that we need to develop Taylor series of the drain current as a function of the applied gate voltages. In this context, the drain current can be expressed as

$$I_{ds} = I_0 + \sum_{i=1}^{n} g_{mi}\, V_{gs}^{i} \tag{III.31}$$

where I_0 is the current at DC operation point and $g_{mi} = \frac{\partial^i I_{ds}}{\partial V_{gs}^i}$ represents the nth order derivative of I_{ds} with respect to V_{gs}.

The transconductance, its first and second derivatives are used as device linearity criteria. So, in order to evaluate the linearity performance of our design, we need to extract the values of g_{mi} (i takes integer values from 1 to 3) at a fixed value for the drain current, then we compute the following device parameters of merit [127]

$$VIP_2 = 4\frac{g_{m1}}{g_{m2}} \tag{III.32}$$

$$VIP_3 = \sqrt{24\frac{g_{m1}}{g_{m3}}} \tag{III.33}$$

And

$$IIP_3 = \frac{2}{3}\frac{g_{m1}}{g_{m2}R_s} \tag{III.34}$$

It is to note that for better linearity performance and to achieve a lower limit on the distortion, the parameters VIP_2, VIP_3 and IIP_3 be as high as possible.

III.3 Results and discussions

In this section, we have twofold objectives. First, we provide a comparison between different considered architectures using the developed analytical models of performance criteria. Second, a genetic algorithm based approach is proposed for the optimal design of our proposed structure to be employed as a component for building efficient analog applications.

The variation of the drain current as a function of the drain voltage at different gate voltages ($V_{gs} = 1.5V$ and $V_{gs} = 2.5V$) for conventional DGJL MOSFET, DMDGJL MOSFETs with and without S/D extensions are presented in Figure III.2, the channel length in this case is fixed to 100nm.

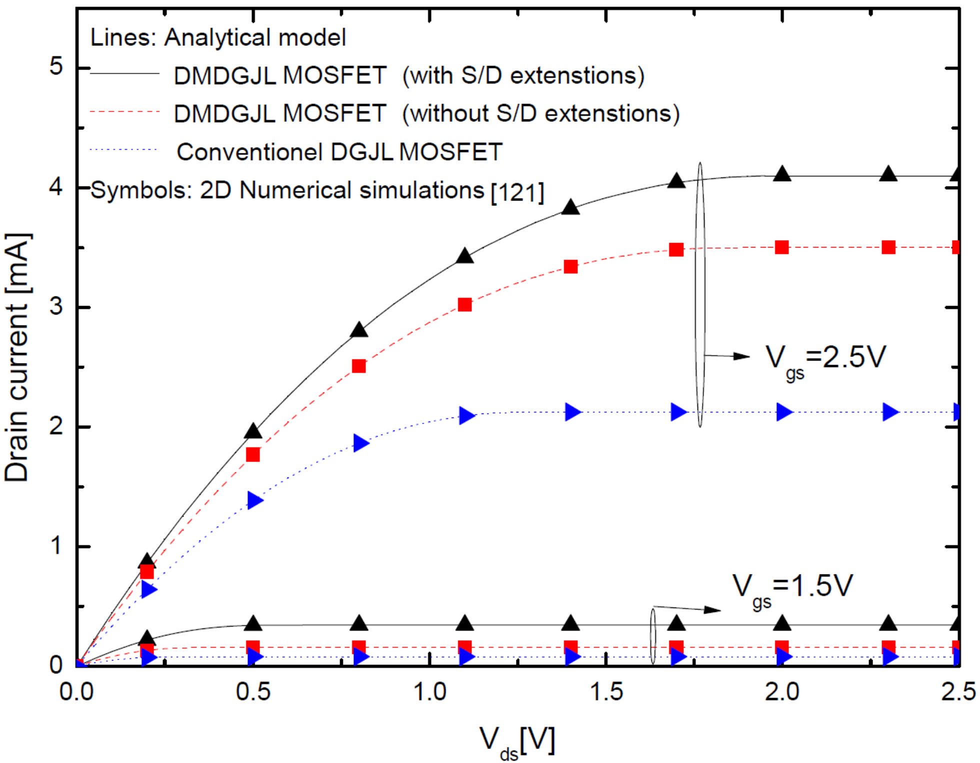

Figure III.2: Variation of the drain current as a function of the drain voltage (N_d=5.10^{18} cm^{-3}, N_{ext}=5×10^{19} cm^{-3}, t_{si}=10 nm, t_{ox}=5 nm, L=100 nm, L_1=L_2=L/2, $\phi_{M1} = 5.1eV$ $\phi_{M2} = 4.5eV$).

It can be noticed that the DMDGJL MOSFETs with S/D extensions exhibits higher drain current in comparison with other two structures and this discrepancy becomes larger with the increase of the gate voltage. Such improved behavior can be attributed to the redistribution of the electric field at the drain side so that the electron concentration remains unaffected in the inversion layer.

Figure III.3 shows the curve of the transfer characteristic with an applied drain voltage $V_{ds} = 1.5V$ for the conventional structure compared to both devices DMDGJL MOSFETs with and without S/D extensions.

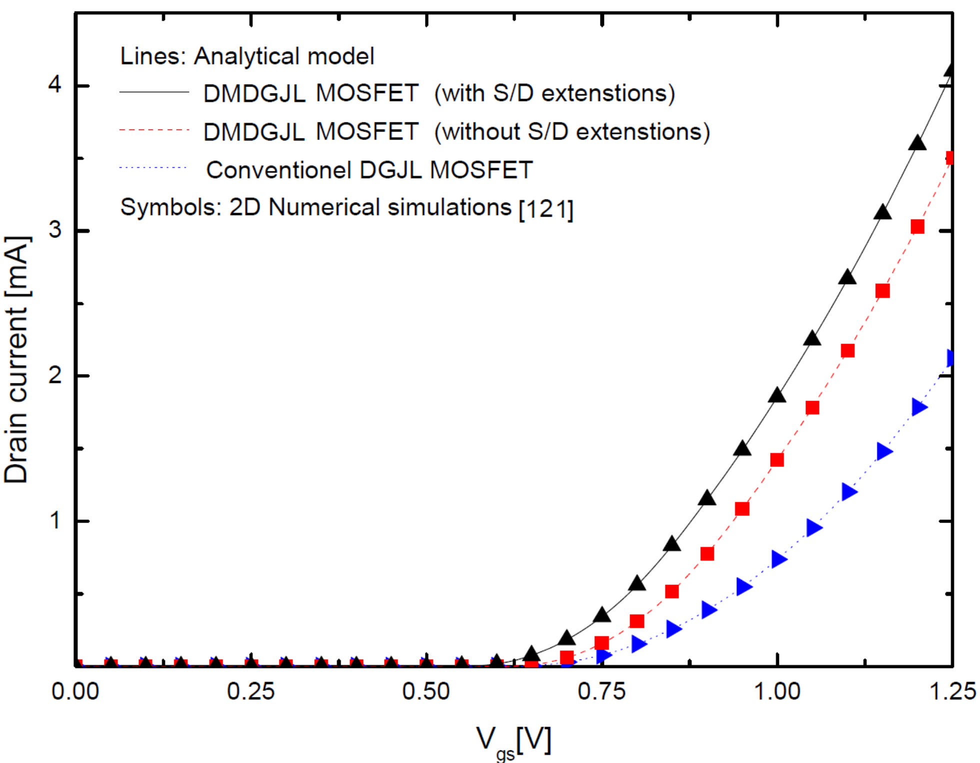

Figure III.3: Transfer characteristics $I_{ds}(V_{gs})$ in linear scales (V_{ds}=1.5V, N_d=5.10^{18} cm^{-3}, N_{ext}=5×10^{19} cm^{-3}, t_{si}=10 nm, t_{ox}=5 nm, L=100 nm, L_1=L_2=L/2, $\phi_{M1}=5.1eV$ $\phi_{M2}=4.5eV$).

In a similar manner to the direct characteristics, it is clearly observed that the proposed device offers better drain current capability in comparison to the conventional one, which is a very important parameter for high-performance analog/RF applications. The improvement of the drain current when increasing the doping concentration of the S/D extensions is caused by the reduction of the source/drain series resistance. While at low source/drain doping concentration, the drain current may be degraded due to the existence of some depletion regions inside the source and drain.

In Figure III.4, the variation of the ON-current as a function of the channel thickness is depicted for conventional DGJL MOSFET, DMDGJL MOSFETs with and without S/D extensions. It can be seen that the ON-current for all cases has a linear profile with respect to the channel thickness increase.

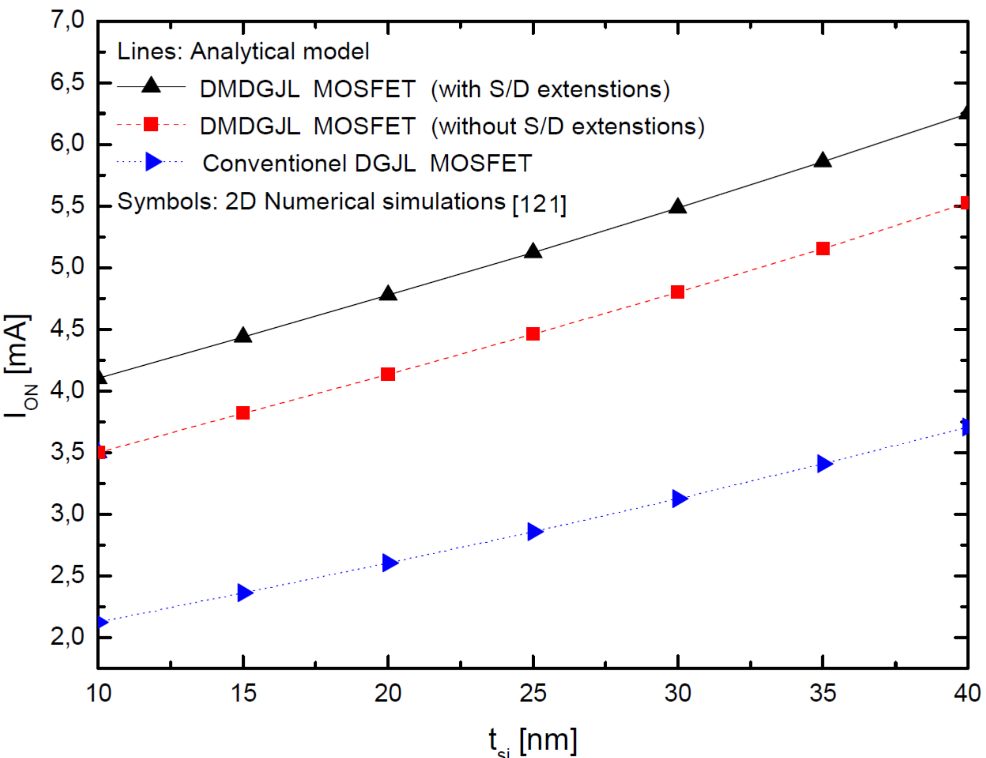

Figure III.4: Variation of the ON-current as a function of the channel thickness (N_d=5×10^{18} cm^{-3}, N_{ext}=5×10^{19} cm^{-3}, t_{ox}=5 nm, L=100 nm, L_1=L_2=L/2, V_{ds} = 2 V, V_{gs} = 2 V, $\phi_{M1}=5.1eV$, $\phi_{M2}=4.5eV$)

The S/D extensions lead to a significant improvement of the current due to the reduction of the parasitic series resistance effect. Moreover, as expected, in this Figure the increase of the device thickness leads to an enhancement of the drain current. This is mainly due to the degradation in threshold voltage value. Besides, this degradation can be explained by the increasing of the silicon body volume which makes the gate control over the channel worse. As a result, the threshold voltage decreases with increasing the silicon thickness. Thereby the drain current will be improved.

Figure III.5 illustrates the variation of both gain and transconductance versus the channel thickness for all three proposed structures. It can be easily observed that the device including the gate engineering and S/D extensions provides the highest performance since the S/D regions contribute to the amelioration of the drain current magnitude while the gate engineering allows screening the effect of some parasitic phenomena near the drain side.

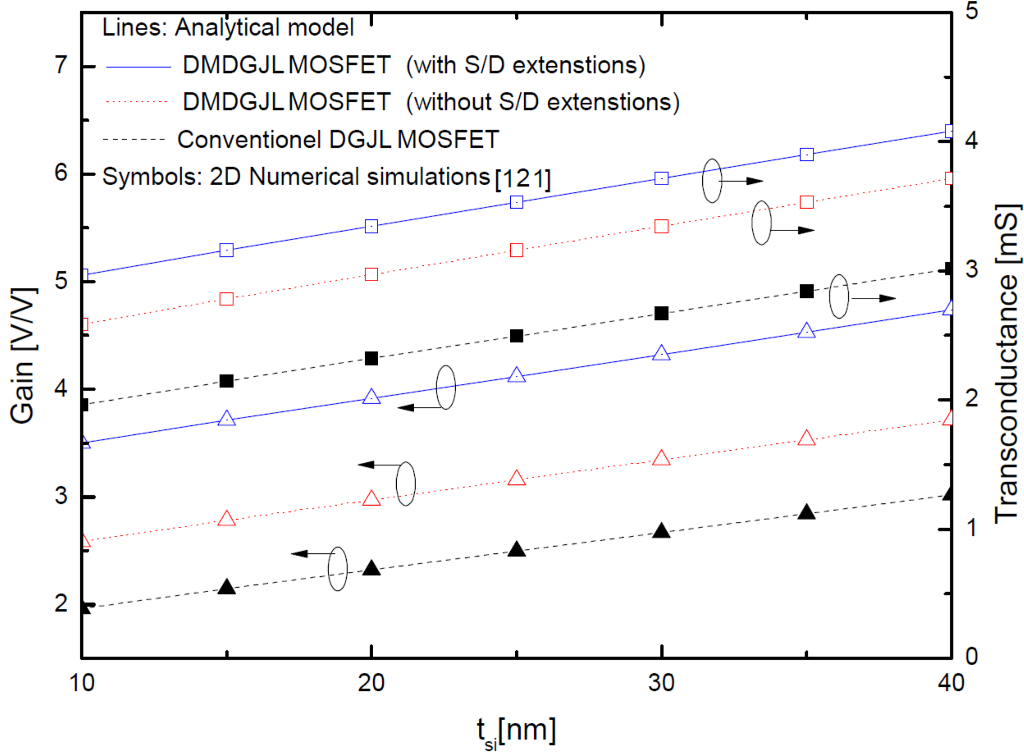

Figure III.5: Variation of gain and transconductance as a function of the channel thickness (N_d=5×10^{18} cm^{-3}, N_{ext}=5×10^{19} cm^{-3}, t_{ox}=5 nm, L=100 nm, L_1=L_2=L/2, V_{gs} = 2 V, V_{ds} = 2 V, $\phi_{M1} = 5.1eV$, $\phi_{M2} = 4.5eV$).

In order to evaluate the adaptability of our proposed architectures for high-frequency switching applications, the cut off frequency is computed to assess the analog/RF performance.

Figure III.6 presents the variation of the cut off frequency as a function of the channel thickness.

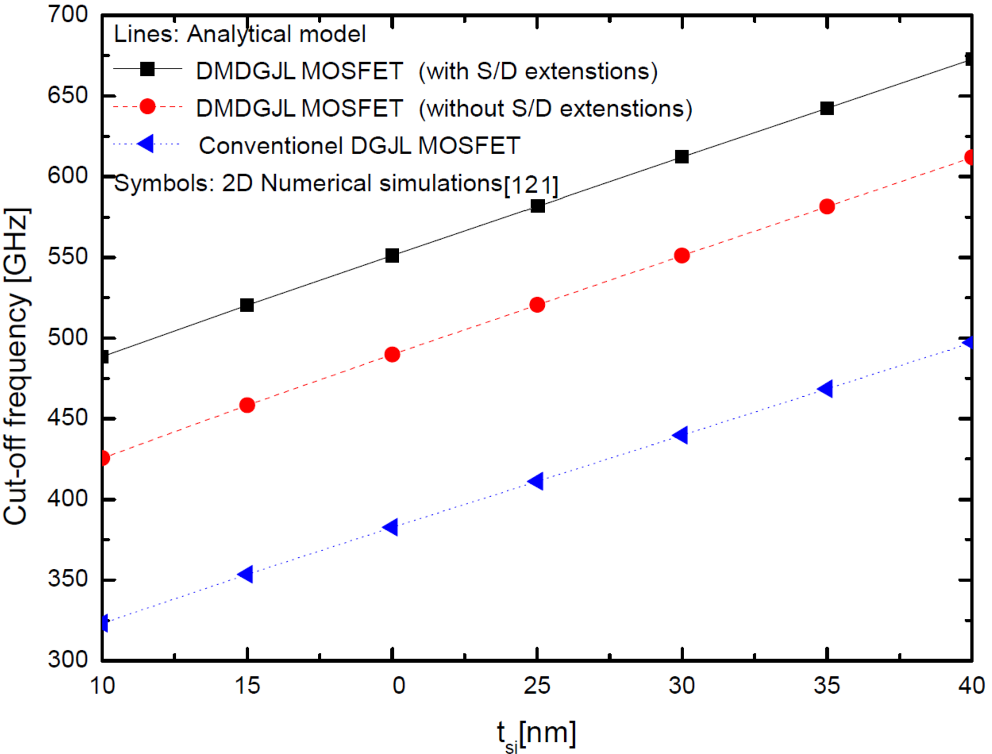

Figure III.6: Variation of the Cut-off frequency versus the channel thickness (N_d=5×10^{18} cm^{-3}, N_{ext}=5×10^{19} cm^{-3}, t_{ox}=5 nm, L=100 nm, L_1=L_2=L/2, V_{gs} = 2 V, V_{ds} = 2 V, $\phi_{M1} = 5.1eV$, $\phi_{M2} = 4.5eV$).

By calculating the relative improvement with respect to the conventional DGJL MOSFET, we find that DMDGJL MOSFETs without and with S/D extensions have 55% and 36% improvement rate respectively. It should be mentioned that the obtained magnitude of the cut off frequency is in good concordance with some similar studies [128,129,131].

The progress of the objective functions of the conventional and the proposed junctionless devices is illustrated in Figure III.7 and Figure III.8, respectively.

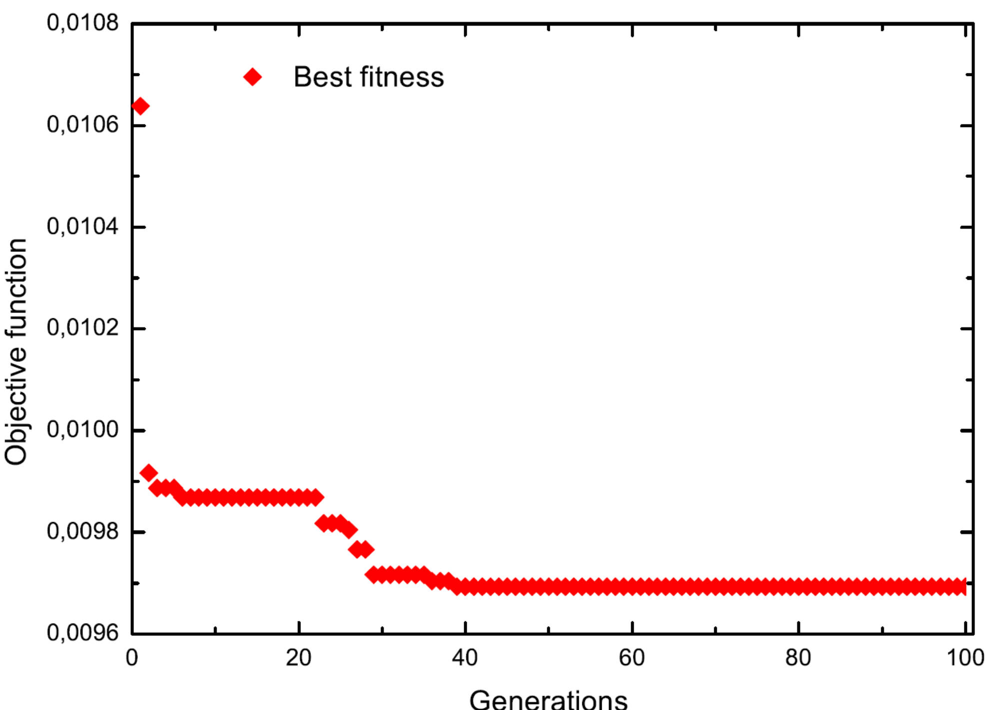

Figure III.7: Evolution of the normalized overall objective function versus the number of generation of conventional DGJL MOSFET.

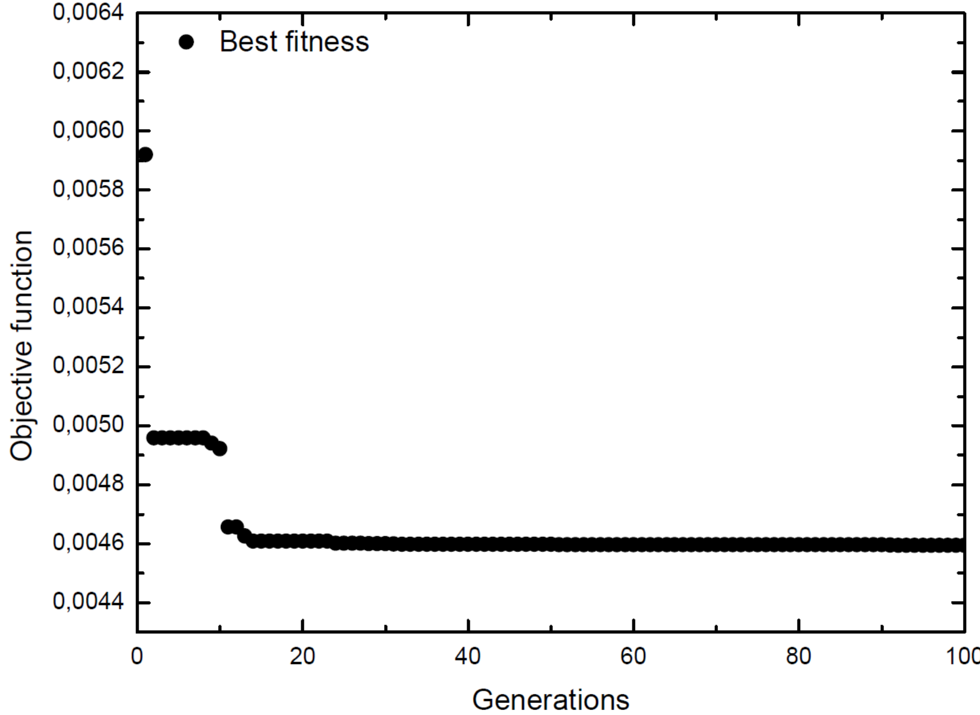

Figure III.8: Evolution of the normalized overall objective function versus the number of generation of DGJL MOSFET with extensions and gate material engineering.

It is clearly shown that the objective function associated to the proposed design converges more rapidly to the best solution (0.0046)(Figure III.8) within the limit of 25 generations,

while the objective function of the conventional junctionless design reaches its stability (0.0097)(Figure III.7) in 40 generations.

III.3.1 Optimization of DGJL MOSFET performance

In what follows, we focus on the optimal tuning of geometrical and electrical parameters of our proposed design in order to obtain the best performance. For this purpose, we adopt genetic algorithms as an optimization tool since they have shown to be very efficient in dealing with hard multivariable problems. During the resolution procedure of genetic algorithms, successive populations are generated using selection, crossover and mutation operators applied to individuals inside a single population which allows exploring areas in the solution space with the aim to find better combinations.

The exploitation of our proposed design for RF/analog applications requires the accurate definition of objective functions to be included within the optimization framework. Indeed, the DMDGJL MOSFET structure can offer a higher performance by satisfying the following goals in terms of considered objective functions:

- Maximizing the cut off frequency
- Maximizing the derived drain current
- Maximizing the three linearity parameters

By using the weighted sum approach method, all the five objective functions can be integrated in a single objective function with the introduction of weighting coefficients. So, the expression of the overall objective function is given by

$$F(X) = w_1 f_c + w_2 I_{DMAX} + w_3 VIP_2 + w_4 VIP_3 + w_5 IIP_3 \quad \text{(III.35)}$$

where different objective functions have equal weighting factors (w_i=0.2), and X represents the design parameters vector (Table III.2). These parameters should satisfy the following constraint:

$-g(x) : x \in [x_{imin}, x_{imax}], x_i \in X$ (each design parameter should be confined within a given range, in order to ensure that specified design requirements are met).

Some numerical tests have been conducted in order to deduce the genetic algorithm parameters values that lead to satisfactory results in terms of solutions quality and computational costs. For the obtained configuration, the evolution of the normalized overall objective function reaches converges to a steady state in about 40 an 30 iterations for conventional and proposed designs, respectively, as indicated in both Figure III.7 and

Figure III.8, which takes about 18 minutes on *i*7 processor (3.4 GHz) running under Windows 7 system for both structures.

The parameters values used during the optimization procedure are summarized in Table.III.1.

Table.III.1: Configuration parameters used for the genetic algorithm based optimization for both conventional and proposed structures.

Parameter	***Value***
Number of variables	11
Population size	20
Maximum number of generations	100
Selection	Stochastic uniform
Crossover	Constraint dependent
Mutation	Scattered
Migration	Forward
Crossover fraction	0.8
Migration fraction	0.2

Once the simulation is completed, the comparison of the optimized devices with an IM-DG MOSFET is possible as illustrated in Table.III.2.

In the following table, it is clearly shown that our optimized DGJL MOSFET yields 40% enhancement of I_{ON}, 85.6% improvement in Cut-off frequency and enhanced values of linearity parameters as compared to reported results [130] for devices with 100 nm channel length. It should be noted that the optimal solution varies with the values of the weighting factors of the overall objective function.

Table.III.2: Comparison of performance metrics obtained from our optimized JL devices with that of an IM-DG MOSFET for analog/RF applications.

Symbol	Optimized conventional DGJL MOSFET	IM-DG MOSFET [124]	Optimized DMDGJ MOSFET with S/D extensions
Channel length $L(nm)$	100	100	100
Channel length for first gate $L_1(nm)$	-	-	51
Channel length for second gate $L_2(nm)$	-	-	49
Oxide thickness t_{ox} (nm)	4	5	4
Silicon thickness t_{si} (nm)	20	30	32
S/D extensions doping concentration N_{dext} (cm^{-3})	-	-	7×10^{19}
Channel doping concentration N_d (cm^{-3})	1×10^{18}	5×10^{15}	1×10^{18}
First gate work function ϕ_{M1} (eV)	-	-	4.8
Second gate work function ϕ_{M2} (eV)	-	-	4.1
Gate work function ϕ_M (eV)	4.9	4.9	-
Drain voltage $V_{ds}(V)$	4	6	3
Gate voltage $V_{gs}(V)$	2.5	3	2.5
Objective functions			
Cut-off frequency (GHz)	503	570	1058
Derived Drain current I_{DMAX} (mA)	7	3.8	9.8
VIP_2	2.58	-	4.1
VIP_3	3.78	-	9.41
IIP_3	0.013	-	0.018

III.4 Conclusion

In this chapter, the impact of both S/D extensions and gate material engineering on DGJL MOSFET transistor for analog/RF performance has been analytically investigated at 100 nm channel length. Moreover, a comparison has been carried out with the conventional case in terms of RF/analog performance criteria and linearity parameters. It has been deduced from the obtained results that the S/D highly doped extensions have a significant impact on the series resistance, which allows the improvement of the drain current in addition to RF criteria. The lowering of the gate work function near the drain side contributes to the enhancement of gate control capability over the channel. Therefore, the

proposed design is best suitable for low-cost and analog/RF applications. In order to boost the device performance, a multi-objective genetic algorithm based optimization has been successfully investigated in the context of our study. Promising results have been obtained where the optimized design performance outperforms considerably the conventional junctionless and IM-based designs. As a future work direction, the proposed structure can be integrated within IC design environments in order to evaluate its impact on more complicated applications.

Chapter IV: Design of DGJL MOSFETs for nanoscale circuit applications

IV.1 Introduction

There is no doubt that the scaling process constitutes the cornerstone of almost all benefits gained by modern electronics. Basically, miniaturization can bring additional possibilities for integrating more devices on a unique die, and in turn, increasing functionality options per chip. Moreover, scaling permits to obtain a circuit design having smaller dimensions, cheaper costs, and faster responses besides low power consumption. All these factors have approved new applications in today's electronic industry such as the cheap mobile manufacturing [132].

The need for integrated approaches regarding system design is mainly linked to the elaboration of methodological notions in addition to details about elementary phases in the design procedure. The high complexity of basic components prohibits us from focusing on low levels of the design but with dedicating more efforts on high abstraction levels. Since the design procedure is relatively influenced by design tools used for mapping abstract components, the designer can investigate other implementations in order to decide at an early stage the employment of a specified component [133].

In this chapter, we maintain the structure of DGJL MOSFET device proposed and investigated in the previous chapter to be assessed in the framework of an analog circuit. However, we should first answer the question: is the conventional DGJL MOSFET without gate engineering (dual gate material) and without highly doped source drain extensions better than the inversion mode DG MOSFET? In other words, we should first prove that the DGJL accumulation mode conventional is better than the DG inversion mode conventional.

To highlight the aforementioned work, the chapter is divided into two parts. The first part deals with the immunity behavior of the junctionless DG MOSFET device against the hot carrier degradation effect. The junctionless device is highly privileged because of its easy fabrication procedure, homogeneity along the channel axe in addition to its promising electrical characteristics compared to the conventional DG MOSFET with PN junction at the source and the drain sides. As a result, we demonstrate that the junctionless DG MOSFET can be a viable option to enhance the immunity performances of nanoscale CMOS-based devices technology for nanoelectronics digital applications. In the second part, the developed model adopted in the third chapter for the double gate junctionless (DGJL) MOSFET circuit performance parameters are developed incorporating the impact

of dual-material gate engineering and highly doped extension regions on the performance of the common source single stage amplifier circuit. In order to analyze the characteristics and circuit performance of the device, we have adopted mixed mode simulation under ATLAS-2D environment for the implementation of the inverter circuit. Based on the numerical outcomes satisfactory results are recorded in comparison with the conventional junctionless structure investigated in the first part.

Part (1): Two-dimensional numerical analysis of nanoscale junctionless and conventional Double Gate MOSFETs including the effect of interfacial traps

IV.1.1 Introduction

As stated by the International Technology Roadmap for Semiconductor (ITRS), the scaling process of transistor dimensions will continue to shrink down to reach the sub 10 nm region by 2018 [5]. Despite that such trend is highly encouraged by the microelectronic industry necessitating the production of smaller and smaller components, challenging drawbacks such as short channel effects still exist or became more severe at this level which in turn result in an increasing difficulty to control the device behavior [134]. In fact, this can be explained by the inner nature of a classical CMOS transistor, including two PN junctions called the source junction and the drain junction. The region separating these two junctions is of opposite doping and permits the identification of the effective channel length [135]. As an example, a typical n-channel transistor uses n-type doping at a concentration order of 10^{20} atoms/cm^3 in the source and the drain and p-type doping concentration of 10^{18} atoms/cm3 in the channel region. One of the critical problems in the newly proposed transistors resides in the accurate establishment of abrupt junctions that depends basically on extremely high doping concentration gradients in addition to a very low thermal budget processing [136]. Hence, the sophistication of fabricating these nanoscale devices can become an industrial concern for manufacturing engineers in terms of costs especially with the inappropriateness of currently adopted approaches like Flash Annealing in producing structures having perfect abrupt junctions with infinite concentration gradients [137]. In addition, the conventional MOSFET design is based on the use of semiconductor junctions, As MOSFETs enter the nanometer regime, extremely high doping density gradients are required to form these junctions. In this case, the formation of ultra-shallow junctions with high doping concentration gradients has become an increasingly difficult challenge for nanoelectronics industry

[136]. The junctionless transistor can be a promising candidate for future nanoelectronics technology as the complexity of fabrication in these devices is highly reduced compared to other transistors with junctions. Recently, many prototypes belonging to the junctionless transistor family have been proposed and fabricated by the Tyndal group, which has initiated a tremendous evolution in junctionless based concepts [138]. The idea behind this new paradigm consists in the elimination of junctions as well as the source/drain extension regions and in contacts both silicon thickness and doping density are tanned up to offer better switching between ON-OFF states. As a first guess, the published experimental and simulation results predict that the junctionless devices present excellent electrical characteristics encouraging the exploration of their use benefits for future technological applications [139-141]. The cornerstone towards the accreditation of junctionless structure for real-world practice is achieved by evaluating its behavior performance under the long duration of device working [142]. The hot carrier induced damage in MOSFET devices results mainly either in the trapping of carriers on sites in the oxide region or in the creation of interface traps at the silicon-oxide in the interface. Consequently, the most obvious result of such situation is that various parameters are affected and became dependent on the channel length when reaching very short dimensions [143, 144]. The main objective of this work is to investigate, numerically, the junctionless device immunity against the effect of the interfacial trap. Simulation results are analyzed for both junctionless and conventional DG MOSFETs in order to get a complete scene of their immunity performances under the same geometrical and electrical parameters. The first part of chapter IV is organized as follows: Section IV.I.2 is dedicated to the device design and simulations parameters. Section IV.I.3 presents and discusses the principal simulation results. Finally, concluding remarks are drawn in Section IV.I.4.

IV.1.2 Numerical simulations

In the Figure. IV.1 we have the bird eye's view of the conventional and junctionless devices used for our numerical investigation. The electrical characteristics of both devices were simulated using the Atlas 3-D device simulator [125]. For the channel region, we have adopted uniform low doping values. The source/drain extension doping profile for the conventional design was uniform too and equals to 10^{20} atoms/cm^3. As depicted in Figure.IV.1, it is clearly shown that the channel region of the proposed

junctionless design has the same doping polarity as the source and the drain. Therefore, such structure has no junctions and less variability in comparison to the conventional design. The applied gate and drain voltages were set to be 0.7 V and 0.1 V, respectively.

In our simulations, the impact of different geometrical parameters (such as gate length, fin width, fin thickness and gate oxide thickness) on the device behavior has been analyzed. In addition, the hot carrier degradation is taken into account by assuming the existence of an interfacial trap density along the 1/3 of the channel length near the drain side. The main parameters used in our investigation for both structures are summarized in Table IV.1.

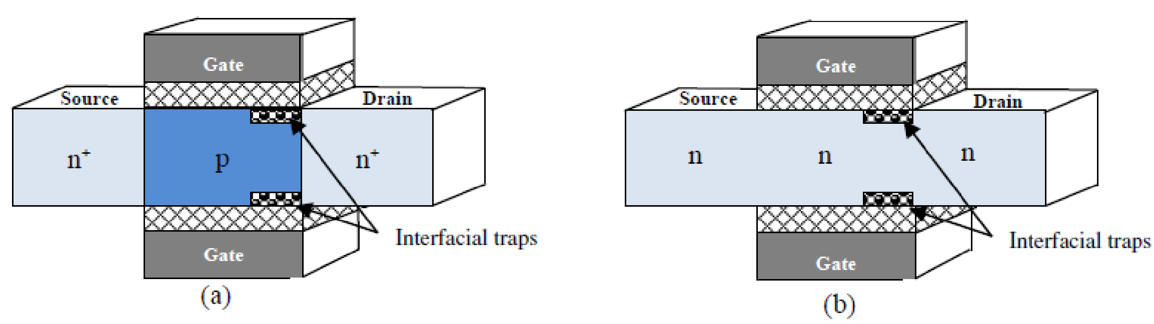

Figure IV.1: Longitudinal cross sections showing the doping profile in: (a) conventional DG MOSFET, (b) Junctionless DG MOSFET.

Appropriate constraints were included within the model in Atlas simulator, the drift-diffusion model without impact ionization, doping concentration dependent carrier mobility and electric field-dependent carrier model. SRH recombination/generation was also included in the simulation to account for leakage currents. It is to note that all computations have been carried out at room temperature. Moreover, our study has been focused to investigate the subthreshold regime (weak inversion), where the drain current is proportional to the total amount of the free electrons at the virtual cathode and their density follows the Boltzmann distribution function. Consequently, the quantum effects can be neglected in our investigation [145].

Our numerical investigation will be focussed to study the impact of the hot carrier effect on the subthreshold swing and threshold voltage. For nanoscale multi-gate MOSFETs, short-channel effects (SCEs) such as threshold voltage and subthreshold swing have an important impact on the device performances. The threshold voltage can be derived using the condition of the minimum channel potential, which depends on the hot-carrier

interface charge density. A small subthreshold swing is required to provide an adequate value of the on-to-off current ratio. The subthreshold swing of a long channel MOSFET has an ideal value (S = 60 mV/dec). To have an acceptable performance, the subthreshold swing has to be close to the ideal value.

IV.1.3 Results and discussions

Figure IV.2 shows the degradation in the subthreshold swing factor of both devices relative to the fresh cases. The influence of the interfacial trap density on the considered parameter is evaluated by parsing a set of values ongoing from 10^{10} to 5×10^{12} cm^{-2}, which is the practical range of the interfacial traps. From Figure. IV.2, it is shown that the junctionless structure provides better subthreshold slope immunity against the hot carrier degradation in comparison to the conventional design. The discrepancy between both curves is not significant for small values and increases rapidly with the interfacial traps density.

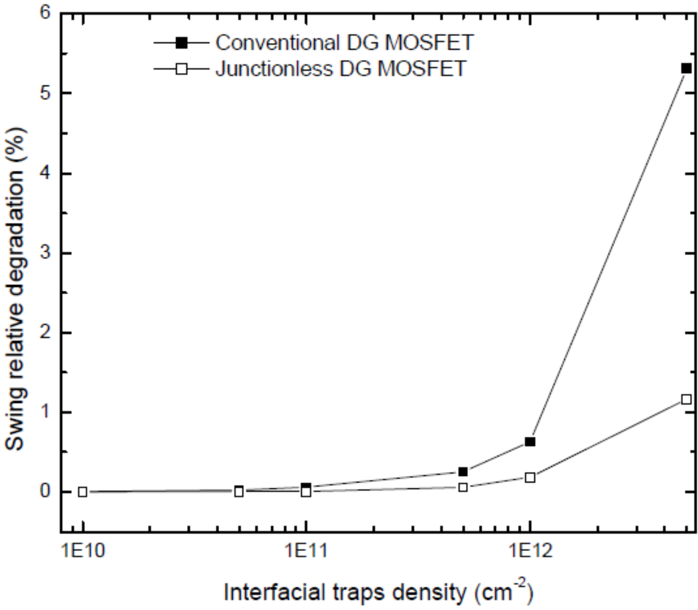

Figure IV. 2: Relative degradation of the swing factor as function of the interfacial traps density for both cases: Junctionless and conventional DG MOSFETs.

The simulated results for threshold voltage versus the interfacial trap density are plotted in Figure. IV.3, where a similar feature can be remarked and the degradation curves follow the same behavior as for the swing slope. The alteration of the threshold voltage is affected considerably from that of the fresh device which is due to the important effect of

the hot carrier induced localized charge density on the electron transport characteristics through the channel.

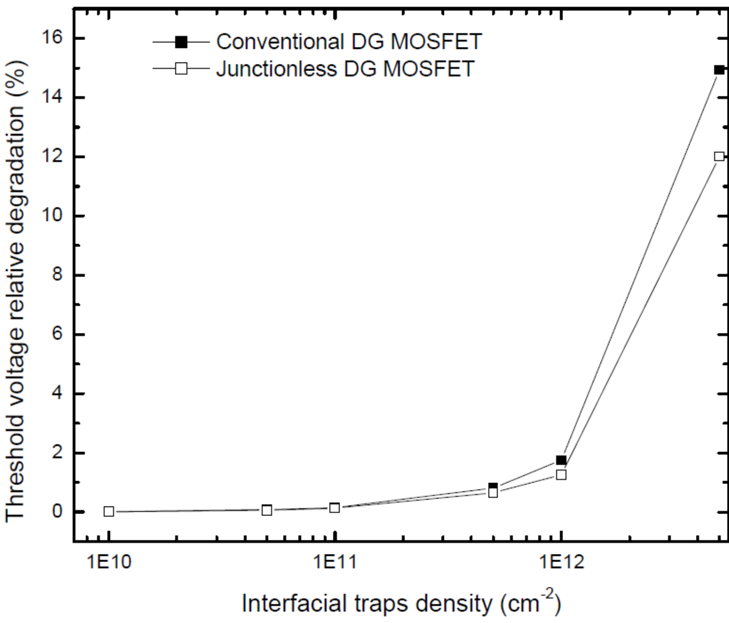

Figure IV.3: Relative degradation of the threshold voltage as function of the interfacial traps density for both cases: Junctionless and conventional DG MOSFETs.

Based on the obtained results, a key aspect regarding the potential of junctionless devices to be considered as a possible candidate for future technological nodes can be easily deduced. The immunity, of junctionless and conventional Double Gate transistors, against the hot carrier degradation in terms of the threshold voltage and swing factor has been analyzed, where low short-channel parameters degradation has been recorded in the case of junctionless design. This means that junctionless DG MOSFET has better electrical and scaling performances in comparison to the conventional design. So, the junctionless design provides better electrical and technological performances in comparison to the conventional structure. These results make the investigated design as a promising candidate for nanoscale CMOS-based devices. It is to note that the proposed investigation, in this paper, is valid for the nanoscale regime, where the channel length silicon film thickness should be taken more than 10 nm and 2 nm, respectively. In atomistic scale, other parameters, like tunnel currents, should be taken into account. Therefore, a new investigation should be developed.

Table IV.1: Simulation parameters of both devices.

Parameters	Conventional DG- MOSFET	Junctionless DG-MOSFET
Channel length	50 nm	50 nm
Channel thickness	5 nm	5 nm
Oxide thickness	2 nm	2 nm
Drain/Source doping	$10^{20}/cm^3$	/
Channel doping	$10^{15}/cm^3$	$10^{16}/cm^3$

IV.1.4 Conclusion

In this study, we have investigated numerically the immunity properties against the hot carrier degradation effects for the junctionless DG MOSFET emerged recently as a prominent design. Such device has no source and drain junctions, as the doping type and concentration is the same in the channel region and in the source and drain. The physical insight gained by this analysis allowed us to better understand and clarify the strength points of the proposed device. The immunity performances of junctionless and conventional DG MOSFETs are compared confirming well the actual trend claiming that the junctionless design is less sensitive to some function parameter variations than the conventional devices such as the case of ageing degradation. Finally, we think that such contribution can provide the guide to further research and experimental exploration of the splendid features of the junctionless paradigm with the main focus on uncovering the potential of new proposed designs in dealing with ageing phenomena generated by the long work duration.

Part (2): Impact of gate material engineering and highly doped drain/source extensions in DGJL MOSFET on nanoscale circuit performances

IV.2.1 Introduction

With nowadays advancement in the CMOS technology, the need for low power tools stimulated the implementation of new devices having deep nanoscale dimensions [145]. However, the continuous shrinking of these structures has amplified the short channel effects, which have become more pronounced particularly when going beyond thirty

nanometers [111,147-150]. In order to remedy the aforementioned parasitic effects, the junctionless paradigm was proposed as a promising vision for the elaboration of multi-gate MOSFET devices [107]. This choice can be justified by the many benefits gained at both performance and fabrication levels. From a quality viewpoint, higher drive current magnitudes are reached in addition to better electrostatic control over the channel core. From a fabrication viewpoint, the process becomes simpler with reduced costs due to the uniform doping of the channel and source/drain regions, which allows, in turn, alleviating impurity and junction creation drawbacks [146,151].

Our aim in this work is to study the impact of a new design on the analog and RF circuit behavior using the ATLAS-2D simulator. The proposed device is based on dual material gate and highly doped extensions regions [106]. Several characteristics are extracted and assessed namely gain (A_v), cut-off frequency (f_T), and static gain. These performance criteria are compared with respect to their counterparts associated with the conventional junctionless case.

The outline of the second part of chapter IV is as follows. In section IV.II. 2, we present the device structure in addition to the principal simulation parameters. Section IV.II.3 highlights the benefits of introducing the proposed modifications on the design in terms of analog and RF performance criteria over its conventional junctionless counterpart. Finally, some conclusions and future research directions are provided in Section IV.II.4.

IV.2.2 Numerical simulations

In this section, we depict the considered Double Gate Junctionless (DGJL) MOSFET and elucidate the simulation framework used for the numerical analysis of the analog and RF behavior characteristics.

IV.2.2.1 Device design

Figure.IV.4 presents both schemas of Double Gate Junctionless (DGJL) MOSFET devices including and without the approved design modifications i.e. in the cases without and with both gate engineering and highly doped source/drain extensions. For the conventional DGJL MOSFET, both gates (upper and bottom gates) have the same work function along the gate. Both the source/drain extension regions and the channel body are uniform heavily doped denoted by $n^+/n^+/n^+$. Whereas for the proposed device, two different gate materials are considered as shown in Figure.IV.4(b) with the aim of

improving the efficiency of carrier transportation. The gate material with least work function is located nearby the drain side while highest value of the work function gate material is affected to the source side. The source/drain extensions are both characterized by high doping values in comparison to the channel body. Thus, the doping concentration densities are noted by $n^{++}/n^{+}/n^{++}$. It is worth mentioning that the suggested structure is in practice a suitable technique since it only requires one ion implantation phase for the implementation of the S/D extensions. Furthermore, the work function value associated with both gate materials can be controlled by tuning the doping magnitude of each poly-silicon gate region. The geometrical and electrical parameters related to the conventional and the proposed devices in addition to their associated values are illustrated in Table IV.2.

Table IV.2: values associated with the configuration parameters used for both conventional and proposed structures

Symbol	*Conventional DGJL MOSFET*	*Proposed DGJL MOSFET*
Channel length L(nm)	100	100
Channel length for first gate L_1(nm)	-	50
Channel length for second gate L_2(nm)	-	50
Oxide thickness t_{ox} *(nm)*	3	3
Silicon thickness t_{si} *(nm)*	10	10
S/D extensions doping concentration N_{dext} (cm^{-3})	1×10^{18}	7×10^{19}
Channel doping concentration N_d (cm^{-3})	1×10^{18}	1×10^{18}
First gate work function ϕ_{M1} *(eV)*	4.9	4.8
Second gate work function ϕ_{M2} (eV)	4.9	4.1
Input voltage $V_{gs}(V)$	1.5	1.5

The schematic view of the investigated structures is depicted in Figure.IV.4, where Figure.IV.4 (a) presents the conventional DGJL MOSFET design without gate material

engineering and Figure.IV.4 (b) shows the DGJL MOSFET design including gate material engineering and highly doped drain/source extensions.

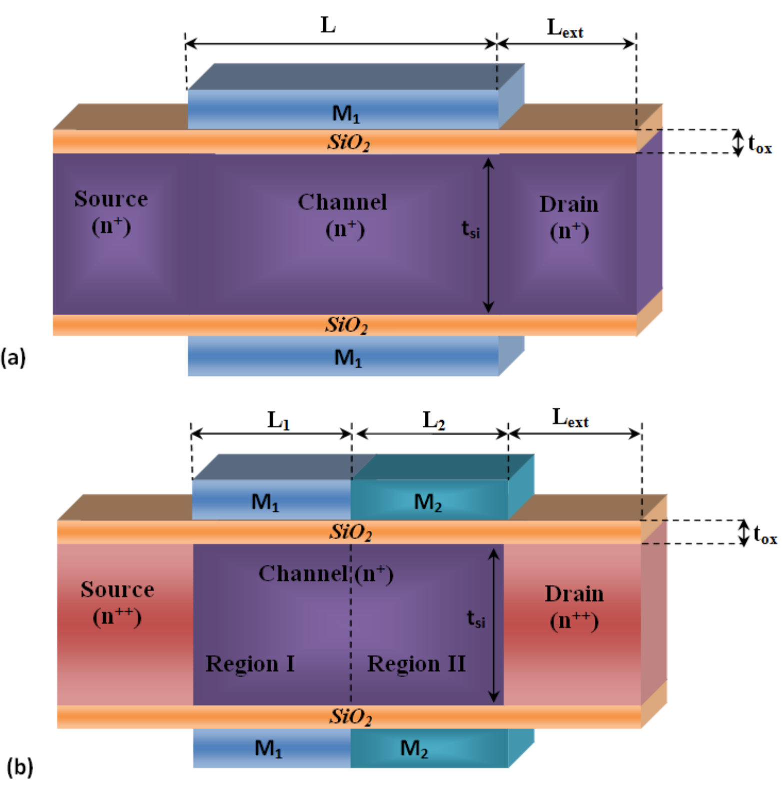

Figure IV. 4: 3D view of (a) DGJL MOSFET without gate material engineering (b) DGJL MOSFET with highly doped drain/source extensions and gate material engineering.

IV.2.2.2 Simulation models

The analog and RF behavior of the designs under study is handled based on the ATLAS-2D simulator with adequate configuration. It is assumed that all simulations are executed at the ambient temperature (300 K). In order to get accurate simulation framework with regard to the realistic behavior, supplementary effects are inserted in the models section. The Shockley-Read-Hall model is included to account for various phenomena related to generation/recombination effects. The expression of the transverse field, doping dependent and temperature dependent elements of the mobility is achieved using Matthiessen's rule in the context of the Lombardi CVT model. Besides, the density gradient model is used for electrons and holes to introduce the quantum confinement aspect of carriers at the nanoscale level.

IV.2.2.3 Inverter circuit design

The elementary circuit component widely used for IC applications is the logic inverter. Inverters can be implemented based on two complementary transistors in a CMOS configuration. It is also possible to construct the inverter using a single NMOS or PMOS transistor jointly with a resistor. In our work, the inverter circuit design adopted in mixed mode simulation is illustrated in Figure.IV.5, where both types of transistors (conventional DGJL MOSFET and proposed DGJL MOSFET) are included as drivers to the common source single stage amplifier circuit for comparison purposes. The numerical simulations are achieved thanks to mixed mode simulation under the ATLAS-2D environment

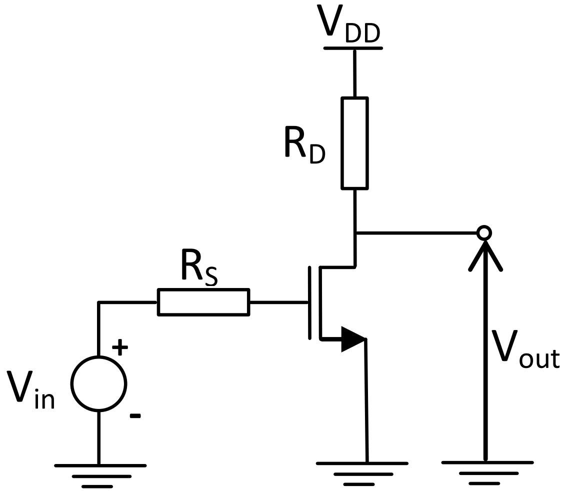

Figure IV. 5: Common source single stage amplifier circuit.

IV.2.3 Results and discussion

From the plot of the voltage transfer characteristics of the inverter circuit illustrated in Figure.IV.5, it can observed that the inverter circuit based on the conventional DGJL MOSFET requires dual polarization voltages in order to ensure the working regime which is not the case for the inverter circuit based on the proposed DGJL MOSFET since the negative polarization is omitted. In addition, the value of gain static provided by the inverter circuit based on the conventional DGJL MOSFET is less than the value provided by the inverter circuit based on the proposed DGJL MOSFET.

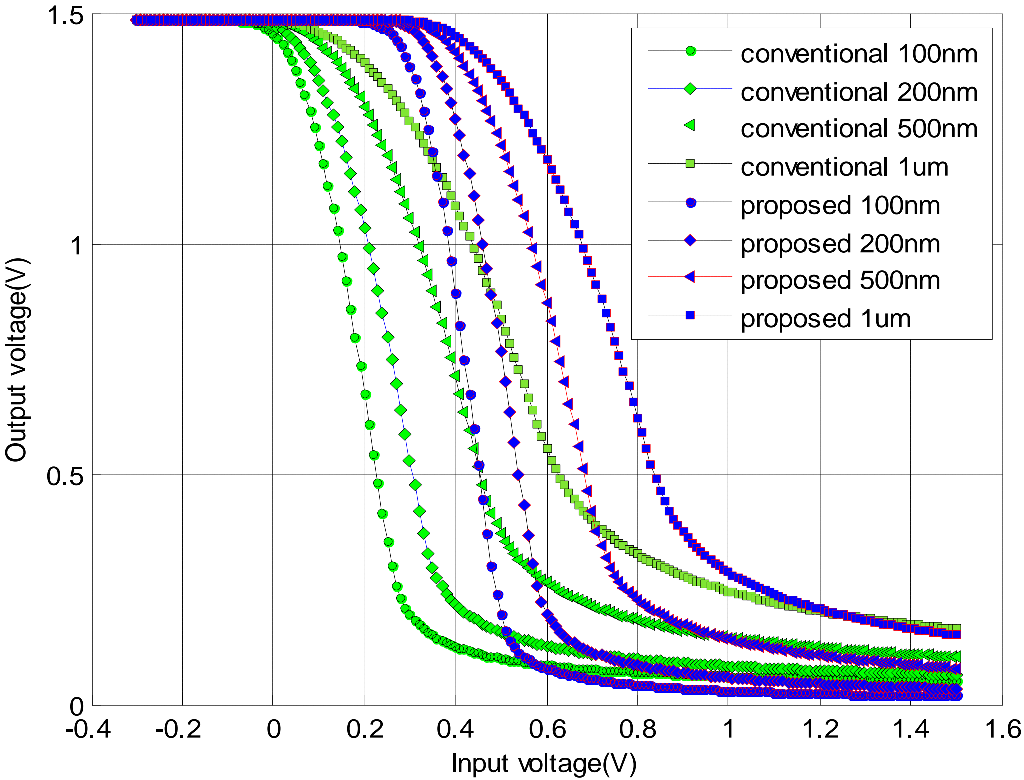

Figure IV. 6: Voltage transfer characteristics of DGJL MOSFET based inverter circuit using conventional and improved transistors with different lengths.

The circuit gain as a function of frequency is computed from the following equation [152]

$$A_v = \frac{V_{out}}{V_{in}} = \frac{R_D C_{gd} s - g_m R_D}{R_s R_D C_{gd} C_{gs} s^2 + \left[R_s \left(1 + g_m R_D\right) C_{gd} + R_s C_{gs} + R_D C_{gd}\right] s + 1} \qquad \text{(IV.1)}$$

where C_{gd} and C_{gs} are the gate-to-drain and gate-to-source capacitances respectively, R_S is the source and R_D is the resistance connected from the drain to the source V_{DD}.

However, it should be mentioned that such expression is not valid for high values of the frequency greater than 100 GHz. As given by Figure.IV.7(a), we notice that the inverter circuit based on the proposed device provides higher gain values in comparison with the inverter circuit based on the conventional device

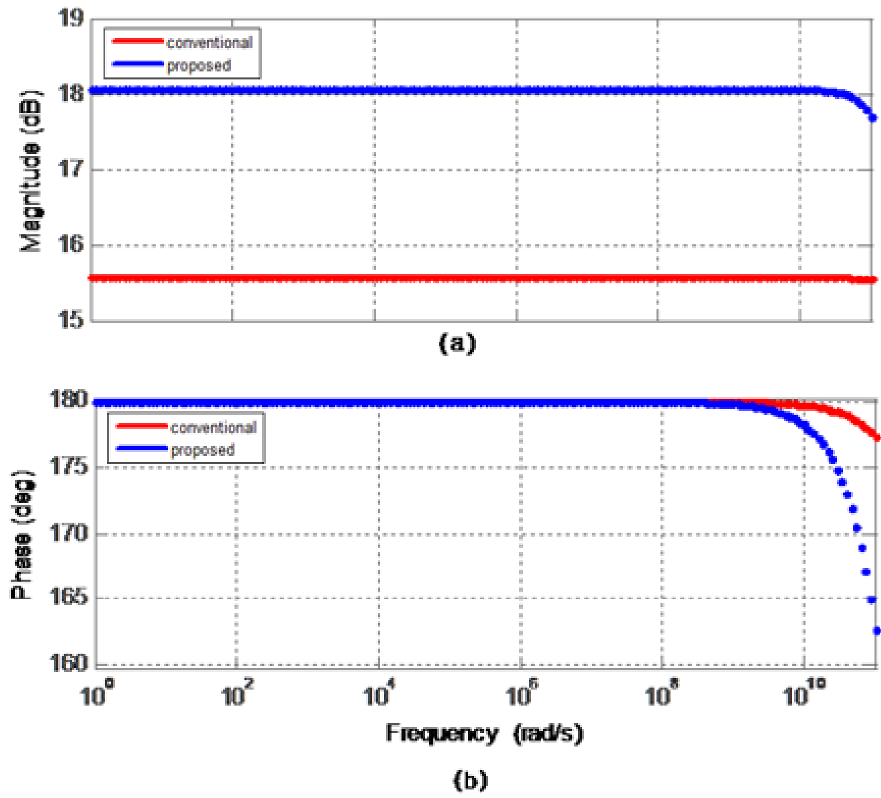

Figure IV. 7: Bode plot of the transfer function of the single stage amplifier (a) gain curve (b) phase curve.

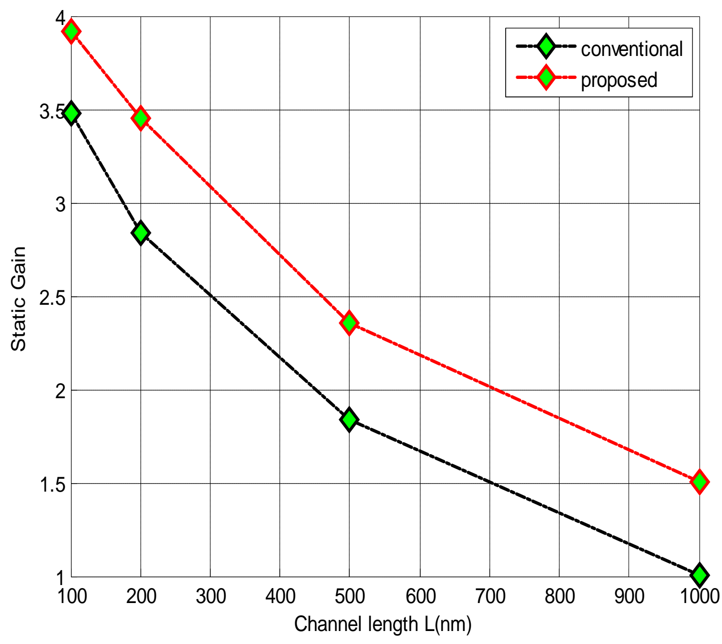

Figure IV. 8: Variation of static gain with respect to channel length of DGJL MOSFET based inverter circuit using conventional and proposed transistors.

The static gain of the inverter circuit based on our proposed device is higher than its counterpart of the conventional circuit and this tendency remains valid over the entire length range of the channel as depicted in Figure.IV.8. In addition, the relative improvement of the static gain increases with the augmentation of the channel length (from 12.68 % for 100 nm to 49.89 % for 1000 nm). This can be explained by the fact that the parasitic effects are more significant for low values of the channel length leading to an alteration of the relative improvement.

IV.2.4 Conclusion

In this work, we have studied the impact of both highly doped drain/source extensions and gate material engineering on DGJL MOSFET transistor for analog and RF performance. Moreover, the circuit performance of DGJL MOSFET based inverter circuit using conventional and proposed transistors with different channel lengths has been numerically investigated using mixed mode simulation under ATLAS-2D environment. From various comparative curves of both circuits, it can be deduced that the integration of the DGJL MOSFET with gate engineering materials and highly doped drain/source extension features in the context of an inverter circuit lead to superior performance. Hence, it can be reasonably claimed that our proposed design constitutes an appropriate candidate for efficient analog/RF applications.

Chapter V: ANFIS-based Approach to Predict the Degradation-related Ageing of Junctionless GAA MOSFET

V.1 Introduction

Over the past few years, extensive efforts have been accentuated on the continuous miniaturization procedure of MOSFET devices, where several amendments have been introduced in order to remedy the parasitic aspects such as the hot carrier injection effects. In fact, these effects tend to be more pronounced with the reduction of the channel length due to the increase of the electric field inside the channel, which has twofold consequences namely the loss of gate control over the channel and the gain of sufficient energies by the carriers leading to their injection into the oxide layer [153]. A serious drawback altering the downscaling process is related to the fabrication procedures since the elaboration of abrupt source/drain junctions at nanoscale level requires enhanced doping profile and thermal budget techniques, which may be in some cases an intractable task. Motivated by the aforementioned reasons, the junctionless paradigm has emerged recently as a competitive alternative to the conventional inversion mode structures. Several studies have demonstrated that the junctionless MOSFET devices offer good subthreshold swing factor in addition to high ION/IOFF ratio in comparison with the conventional designs [154,155]. The Gate All Around Junctionless cylindrical MOSFET (GAA JL MOSFET) can be considered as an ideal structure especially that its manufacturing procedure is based on rounding up the corners of a square shape, which is more flexible for fabrication [156].

In order to accurately predict the long-term reliability of a GAA JL MOSFET device, it is necessary to analyze the hot carrier injection mechanisms. An important operation regime for the hot-carrier effects is closely related to the maximum substrate current occurring at conditions (the applied drain voltage value is twice the applied gate voltage value). Several works have stated that the lifetime of NMOS devices follows a power time law. However, such power time dependence suffers from several disadvantages such as the failure to explain saturated degradation [157]. Up to our knowledge, there is a significant lack of works dedicated to the estimation of multi-gate MOSFET devices lifetime, which requires additional efforts to enlighten such aspect.

The main goal of this chapter is to present an Adaptive Neuro-Fuzzy Inference System (ANFIS) based approach for the prediction of GAA JL MOSFET lifetime. The device is stressed electrically at biasing voltage conditions of $V_{gs} = \frac{V_{ds}}{2}$, which corresponds to the maximum substrate current $I_{sub,max}$. The device lifetime is associated to the stress time

resulting in a relative degradation of the transconductance equals to 10%. The extensive numerical simulations show the strong dependence of the device lifetime on the channel length. Thanks to the deployment of ANFIS method, it is possible to extrapolate with a satisfactory degree of precision the device lifetime for a reduced channel length.

The organization of the chapter is as follows. In Section 2, we describe the numerical model developed by ATLAS-2D simulator, which is used for the design and modeling of the considered GAA JL MOSFET. In the third Section, we showcase the main properties of the ANFIS approach. We present in Section 4 the principal results and we provide some interpretations. In the last Section, we summarize with some concluding remarks. The whole proposed approach can provide some insights on the lifetime prediction of multi-gate junctionless devices.

V.2 Numerical simulations

The 3D schematic and cross-sectional views of the GAA JL MOSFET under study are depicted in Figure V.1 (a), (b) and (c), respectively. The channel, source, and drain regions are uniformly doped and are denoted by $n^+/n^+/n^+$.

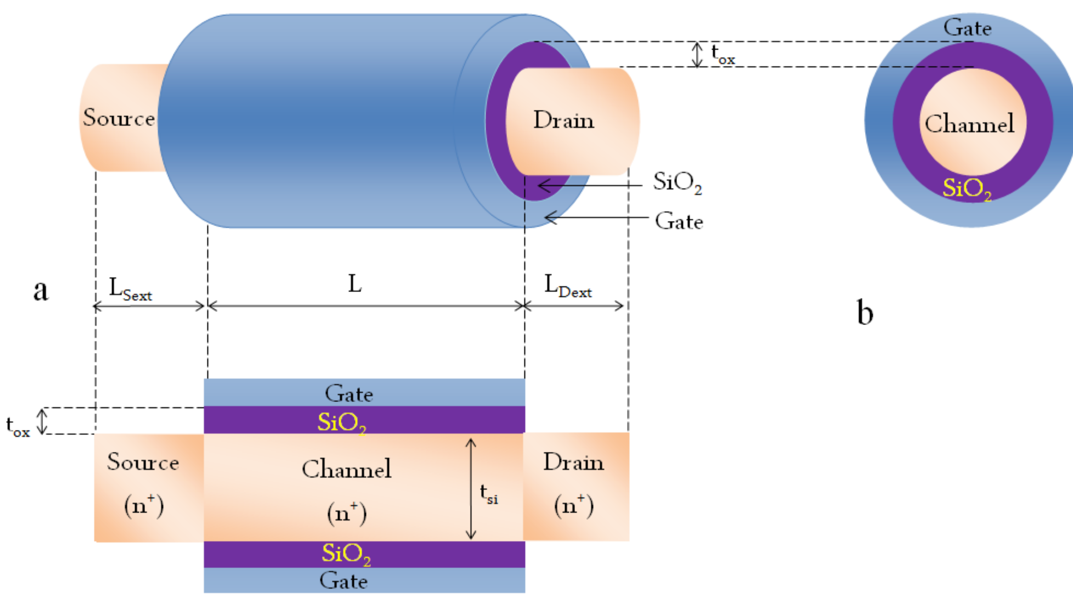

Figure V.1: (a) Three dimensional (b) and (c) Cross-sectional views of GAA JL MOSFET.

The main parameters remaining fixed during numerical simulations are provided in Table V.1. It should be mentioned that the choice of a moderate doping (10^{18} cm^{-3}) for the

proposed JL device can be explained by the resulted improvement in many performance criteria such as ON-OFF current ratio and threshold voltage sensitivity in the case of ultra low power applications as indicated by a recent study [158].

Table V.1: Values of device design parameters.

Parameter	Notation	Value
Channel doping	N_d	$10^{18}\ cm^{-3}$
Source/Drain extension doping	N_{ext}	$10^{18}\ cm^{-3}$
Source/Drain extensions length	L_{Sext} / L_{Dext}	$10\ nm$
Channel thickness	t_{si}	$10\ nm$
Oxide thickness	t_{ox}	$1.5\ nm$
Gate workfunction	$Ø_{MS}$	$4.9\ eV$

The numerical simulations are conducted using ATLAS-2D simulator, which has emerged in recent years as a powerful engine for electronic devices' modeling and analysis [125]. The following configuration issues are considered during simulations. The Lombardi model (CVT) is used to express the carriers' mobility in the inversion layer. The mobility, in this case, is composed of three components (transverse field, doping dependent and temperature dependent) combined using Matthiessen's formula [159]. The Shockley-Read-Hall (SRH) recombination is a trap assisted mechanism, where a localized state within the band gap serves as an intermediate energy state for the electrons' transition between bands. Hence, the difference in energy is propagated in the form of phonons with the lattice [160]. The Auger recombination is also considered in our numerical framework, where the excess energy resulted by electron/hole recombination is transferred to a third carrier. Due to the three-particle interaction nature of this process, it is only pronounced under non-equilibrium conditions with high carrier density [161]. In order to model the hot electrons injection, the lucky electron model is adopted, where an electron is injected from the channel into the oxide region by gaining energy sufficient to surmount the semiconductor/insulator barrier [162]. The injected gate current is given by

$$I_{inj} = \iint P_n(x,y)\left|\vec{J_n}(x,y)\right| dxdy + \iint P_p(x,y)\left|\vec{J_p}(x,y)\right| dxdy \quad \text{(V.1)}$$

with $\overrightarrow{J_{n,p}}(x,y)$ are the electron and hole current densities at a point (x, y) of the semiconductor and $P_{n,p}(x,y)$ are the probabilities that a portion of the injected gate current passes to the oxide region and injected into the gate electrode.

Since the charge transport given by the drift-diffusion model ignores non-local transport effects having a strong impact on the properties of the submicron device, we use the energy balance transport model that includes the carriers' temperature effect within the continuity equations framework. In order to simulate the GAA JL MOSFET degradation when subject to stress conditions, we employ the DEVDEG command in the models section of the numerical model. The main phenomena responsible for the device degradation are the hot carrier injection into the oxide layer besides the trapping of carrier charge at the semiconductor/oxide interface. The degradation, given by the amount and position of the oxide damage, is expressed as a function of stress time based on transient computations [163]. Thus, the trap rate equation is solved which allows obtaining the trapped carriers concentration as follows:

$$\begin{cases} \frac{dN_n(x,t)}{dt} = \frac{\sigma_E}{q} J_{inj,n}(NTA(x) - N_n(x,t)) \\ \frac{dN_p(x,t)}{dt} = \frac{\sigma_H}{q} J_{inj,p}(NTD(x) - N_p(x,t)) \end{cases} \quad \text{(V.2)}$$

with $N(x,t)$ is the trapped carrier density at the interface for a given time. The NTA and NTD are parameters denoting the acceptor and donor-like trap densities at time=0. The parameter J_{inj} is the injected current density for both carrier types, σ_E and σ_H represent the capture cross section of electrons and holes, respectively. The running of numerical simulations is conducted under ambient temperature (300 K).

V.3 ANFIS based approach

ANFIS is the abbreviation of Adaptive Neuro-Fuzzy Inference System, which denotes a class of artificial intelligence based approach. ANFIS can be seen as hybridization between the artificial neural network and fuzzy inference paradigms. We can mention here that Fuzzy inference systems are also known as fuzzy-rule-based systems, fuzzy models, fuzzy associative memories (FAM), or fuzzy controllers when used as controllers. As we know that each individual soft computing technique has certain weaknesses and strengths and they cannot be applied commonly to every problem. Thanks to both paradigms' strengths characteristics, ANFIS inherits the high potential of

neural networks in learning from numerical data and the flexible representation ability of fuzzy theory using linguistic variables [164].

An adaptive neuro-fuzzy inference system is composed of four main components namely: fuzzification, rules, inference and defuzzification components [165]. Numerical data are transformed into linguistic inputs using several membership function types. The set of rules are given as Takagi-Sugeno-Kang fuzzy IF-THEN rules, where their general expression is represented by

$$IF\ \left(\left(x_1\ is\ A_1\right)\wedge\ldots\wedge\left(x_k\ is\ A_k\right)\right)Then\ y = p_0 + \sum_{i=1}^{k} p_i x_i \tag{V.3}$$

In its original form, the back propagation algorithm has been used extensively for training in order to adjust different fitting parameters. Once the overall rules are tuned up, it is possible to infer weighted linguistic variables and defuzzify them in order to get a crisp outcome. However, it should be mentioned that many other alternatives are also adopted in the training stage instead of the back propagation method like genetic algorithms or the particle swarm optimization. This may improve the optimum value obtained based on the gradient of the error function which is local in nature [166].

Several works have been dedicated to the degradation of MOSFET devices using the ANFIS approach. For instance, the subthreshold behavior of nanoscale DG MOSFETs including short channel, quantum confinement, and hot carrier effects has been modeled using neuro-fuzzy approaches with the test of several membership functions. The adaptability of such tools for prediction tasks has been also validated statistically [167].

We introduce first the global flowchart of our proposed approach in what follows (Figure V. 2) and then we present in a detailed manner the associated elementary steps.

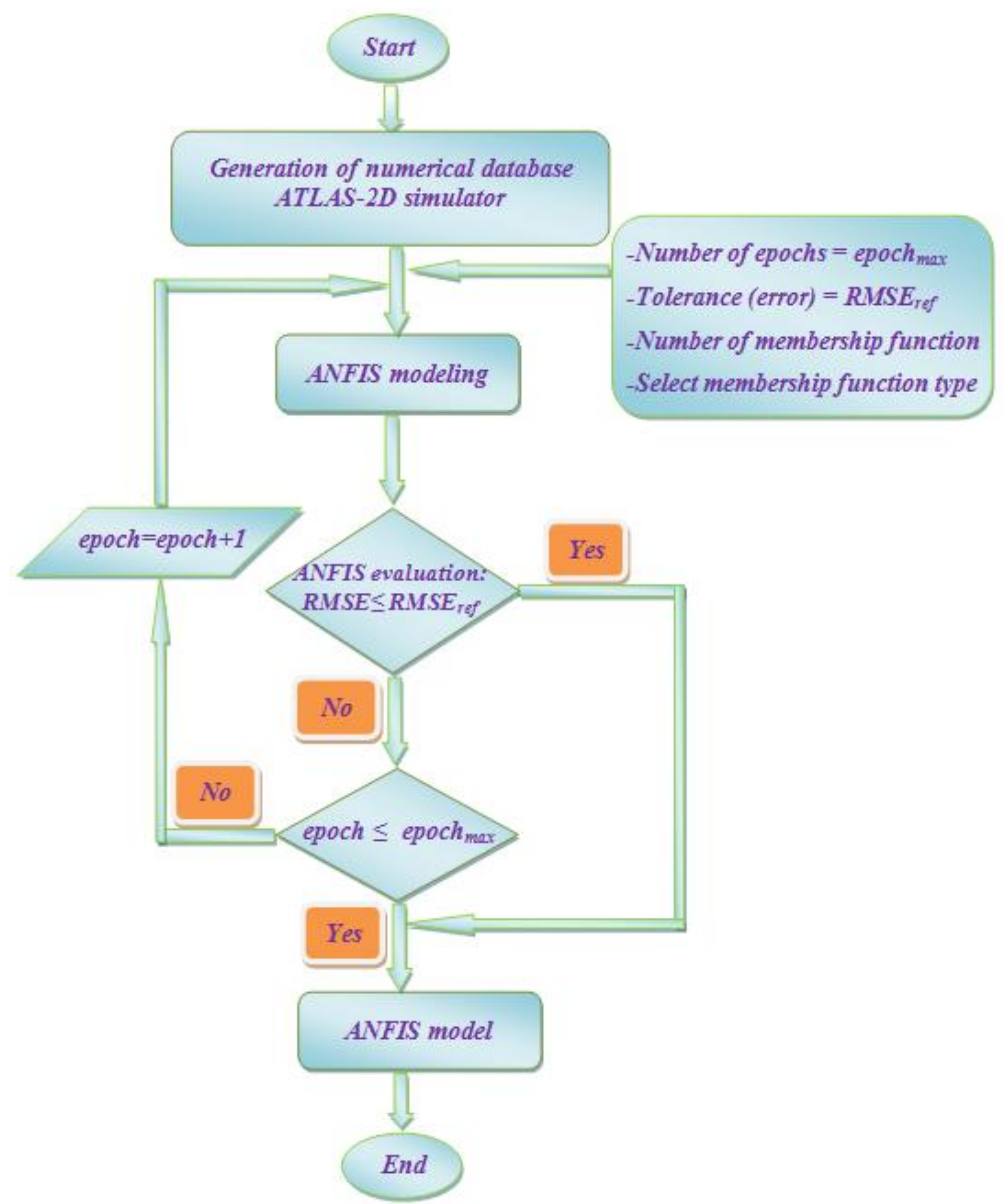

Figure V.2: Different stages of the proposed framework.

V.4 Results and discussion

In this section, we study the influence of the stress process on the performance of the GAAJL MOSFET device in terms of the drain current and transconductance parameters. Moreover, we exploit the detected transconductance relative degradation versus the stress

time for the estimation of the junctionless device lifetime using a neuro-computing technique. In Figure V.3, we highlight the variation of the drain current as a function of the applied gate voltage for different stress times. The obtained curves reveal that the current decreases with the increase of the stress time duration where the discrepancy between different curves becomes more pronounced for high applied gate voltages. We notice the presence of a breakdown region associated to the values of the gate voltage higher than 1 V. Indeed, we consider a wide range of the gate voltage values [0V-3V] in order to highlight the behavior of the device from a global viewpoint.

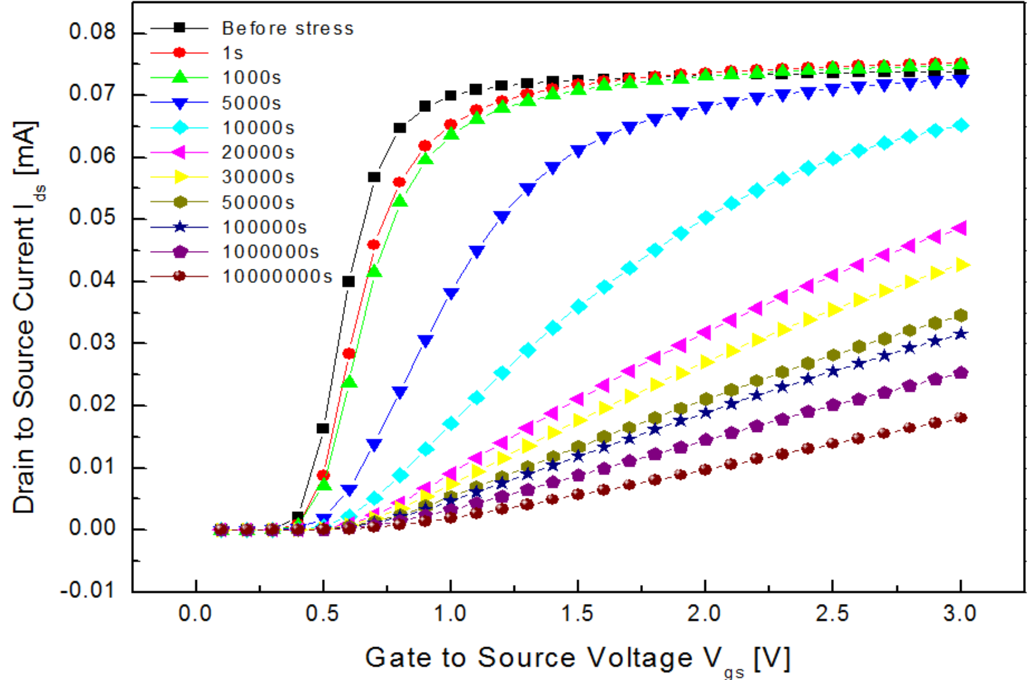

Figure V.3: Variation of the drain current I_{ds} as a function of the applied gate voltage for different stress times (L=100 nm and V_{ds} = 0.15 V).

The behavior of the transconductance as a function of the applied gate voltage for different stress times is represented in FigureV.4. As can be noticed, a significant degradation is recorded on the overall transconductance values due to the stress process. Moreover, the maximum value shifts to higher values of the gate voltage, which reflects less performance of the device. Hence, such degradation may affect its applicability for analog applications.

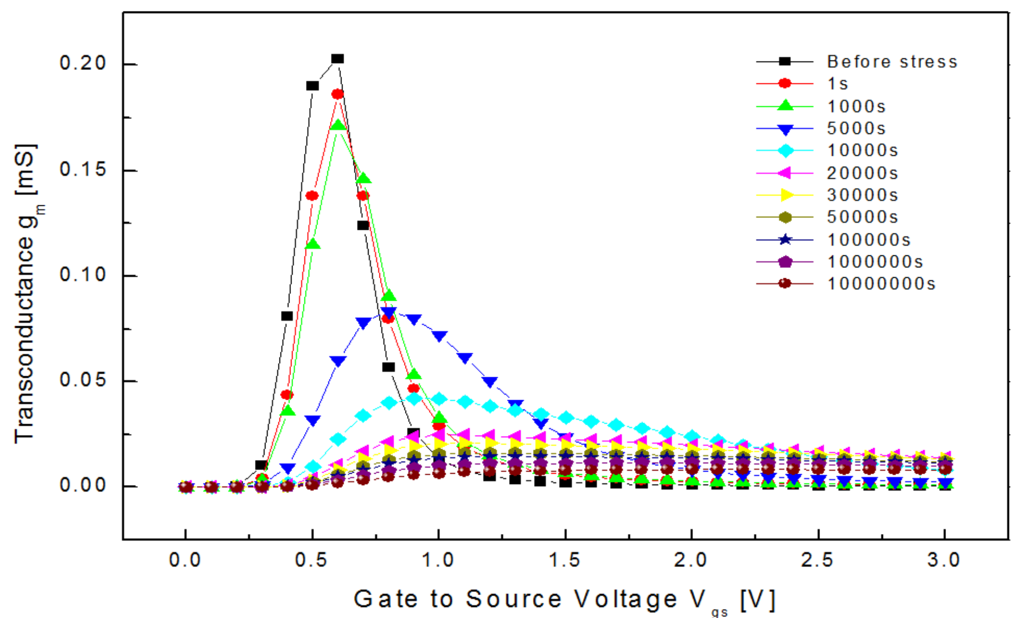

Figure V.4: Variation of the transconductance g_m versus the applied gate voltage for different stress times (L=100 nm and V_{ds} = 0.15 V).

In order to underline the device degradation more accurately, we extract the variation of the maximum transconductance as a function of the stress time. In this case, we have a decreasing tendency of the maximum transconductance with the applied stress times as indicated in Figure V.5.

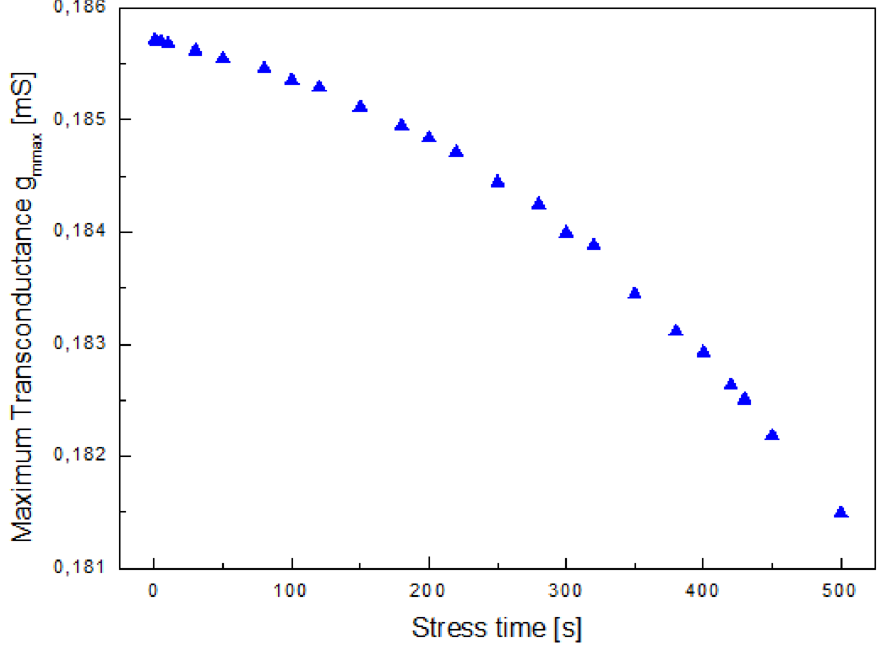

Figure V.5: Maximum transconductance g_{mmax} as a function of stress time (L=100 nm and V_{ds} = 0.15 V).

The following figure is devoted to the impact of the channel length on the junctionless device lifetime (Figure V.6). It can be observed that the slope of the curve tends to be more important for long channels, which expresses that the lifetime of the device decreases drastically with the decrease of the channel length value. Such behavior can be explained by the significant parasitic effects occurring with the downscaling process such as the short channel and hot carrier effects. The resulted degradation is more apparent for small values of the geometrical configuration parameters. However, the numerical computation of the device lifetime for a given length is really cumbersome since it requires a large number of numerical trial and error tests, which are time-consuming. Hence, it would be preferable to seek for other more flexible and easy to use approaches.

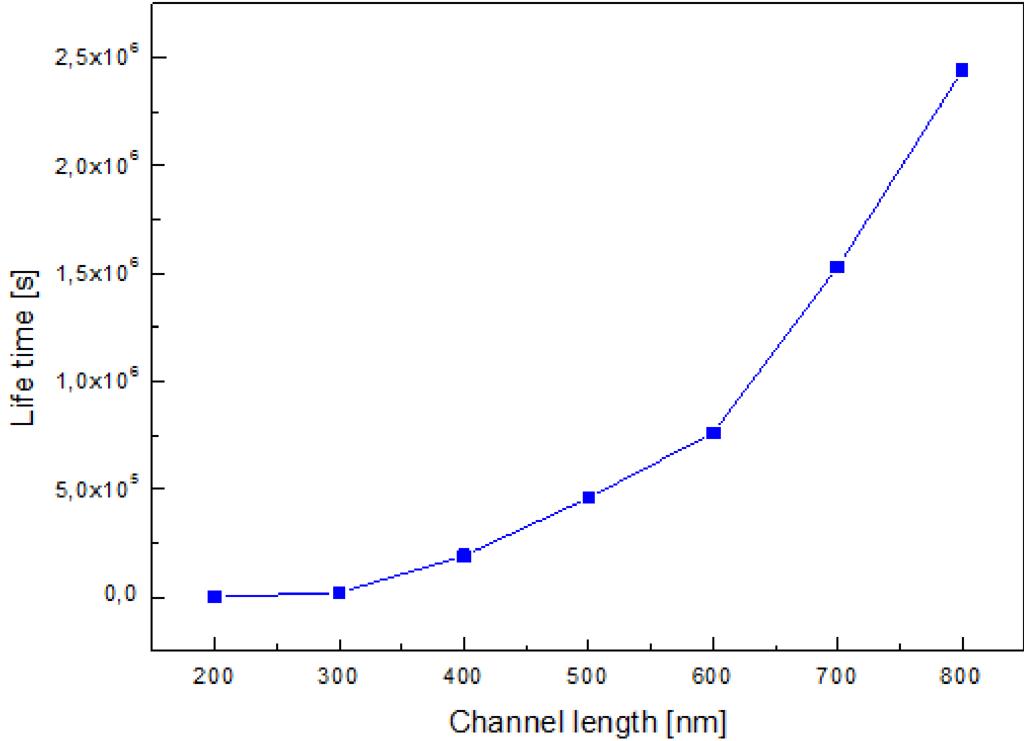

Figure V.6: Variation of the device lifetime as a function of channel length (V_{ds}=0.15 V).

In order to estimate the lifetime of the junctionless device with a channel length of 100 nm, we propose to use an ANFIS based approach. The elaboration of the neuro-fuzzy model is based on the database obtained using the numerical model developed by ATLAS-2D simulator. Each entry in the database is expressed as a vector $\left(-\frac{\Delta g_{mmax}}{g_{mmax\ 0}}, t_{stress}\right)$, where t_{stress} is the stress time, $g_{mmax\ 0}$ is the maximum transconductance corresponding to the fresh device (before stress), and Δg_{mmax} is the

difference between the maximum transconductance at a fixed stress time and $g_{m\max 0}$ which means $\Delta g_{mmax} = g_{mmax} - g_{mmax\,0}$. The data base is partitioned into two sets: the training set including 15 observations used to tune up the hyper parameters of the membership and linear functions. The second set is the test set composed of 8 observations and are used to validate the accuracy of the ANFIS prediction ability. The flowchart of the developed ANFIS is shown in Figure V.7.

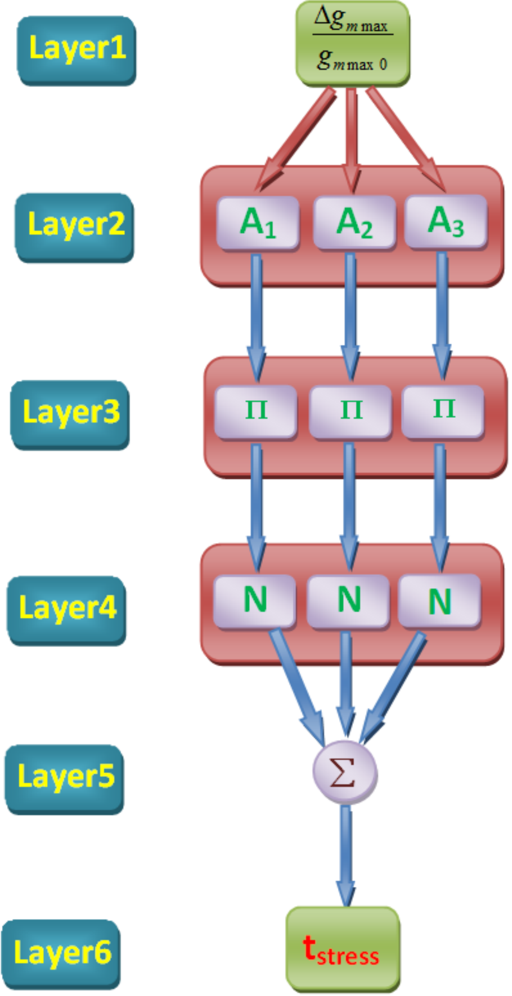

Figure V.7: Illustrative representation of the developed ANFIS with a single input and three MFs.

The general structure of our ANFIS approach is divided into several layers as defined below:

Layer 1: introduces the input parameter $\frac{\Delta g_{mmax}}{g_{mmax\ 0}}$ to the inference system;

Layer 2: contains three membership functions used as a partition of the input parameter range of values;

Layer 3: is composed of different elaborated inference IF-THEN rules;

Layer 4: serves to compute the output of given rules using the selected linear expressions;

Layer 5: includes only one node for the calculation of the overall output through the addition of all provided inputs;

Layer 6: denotes the crisp output as indicated by the stress time parameter t_{stress} .

In Figure V.8, we elucidate the comparison between results delivered by ATLAS-2D simulator and ANFIS based approach. We can deduce that we have a good prediction capacity of the ANFIS model, where it succeeds in catching the variability behavior of the reliability performance evolution of the device. The lifetime of the junctionless device in terms of the stress time corresponds to a relative degradation of the transconductance equals to 10%. The predicted lifetime for the device with 100 nm gate length is relatively small in comparison to the lifetime of devices with a channel length higher than 100 nm. We can explain such significant discrepancy by the drastic amplification of parasitic effects with the downscaling of the channel length as illustrated by many studies (see for example [168]). This leads to a considerable reduction of the predicted lifetime for the device with 100 nm gate length in comparison to superior gate length values (L>100 nm).

It is worthy to mention that the data of Figure V.6 are not used to extrapolate the lifetime of the device with 100 nm gate length due to the limited number of observations in this case in addition to the dependence of the lifetime on several previous temporal observations of the same device, which motivates the adoption of data in Figure V.8 instead of Figure V.6 as a training database in order to get satisfactory results.

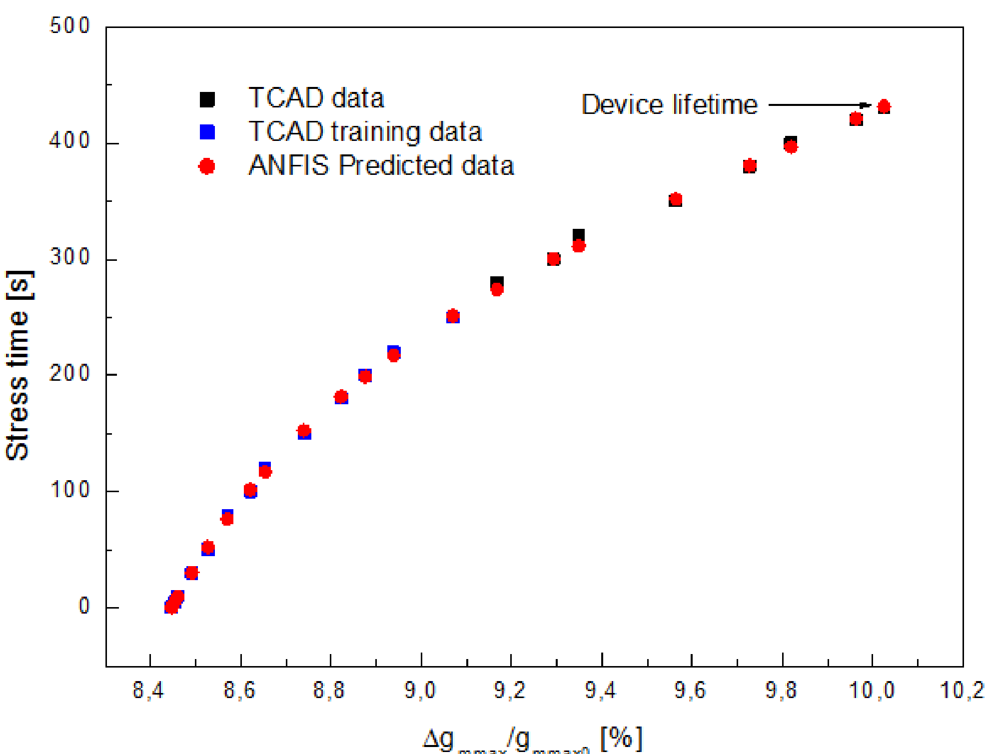

Figure V.8: Comparison between the predicted and simulated lifetime of the junctionless device (L=100 nm and V_{ds} = 0.15V).

In order to confirm the good performance of our ANFIS model, we visualize the scatter plot associated to the ANFIS predicted and the TCAD numerical results (Figure V.9). The obtained points are slightly dispersed around the best fitting line which reflects a strong correlation between simulated and predicted outputs. The correlation coefficient (R^2) is equal to 0.99 while the root mean squared error (RMSE) is equal to 4.04.

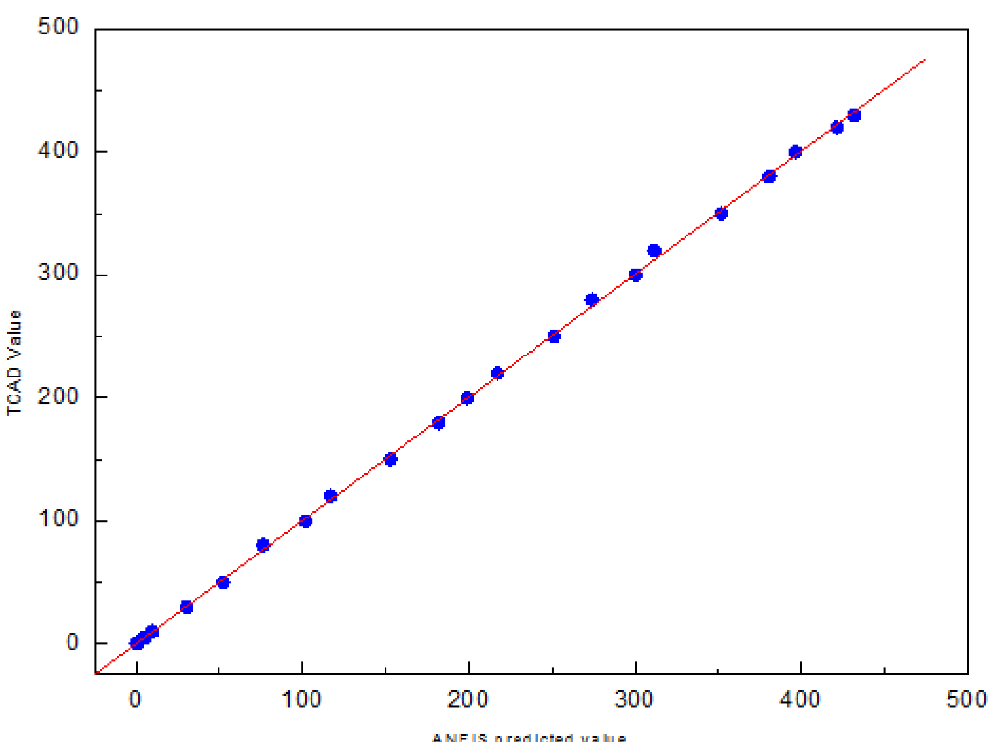

Figure V.9: Comparison of the predicted and the numerical outcomes using the correlation plot.

Thus, the relative degradation of the transconductance and the stress time are considered as the input and output parameters respectively. In fact, even with a single input parameter, the prediction of the expected lifetime is difficult due to two main reasons:

- Atlas 2D simulations achieved are based on the use of stress time as the input parameter and the transconductance as the output parameter. The process of obtaining the expected lifetime from the relative degradation of the transconductance can be considered as an inverse mapping $t_{stress} = f^{-1}\left(-\frac{\Delta g_{mmax}}{g_{mmax0}}\right)$. From a mathematical viewpoint, it is often very difficult to establish an analytical formula for such inverse mapping which requires the map f to be a bijection. Hence, we use ANFIS in order to elaborate a fuzzy-neural model for such inverse relation and based on the obtained model, it is possible to deduce the time associated to 10% of relative degradation in the transconductance magnitude, which expresses the expected lifetime of the device;
- The degradation of the device transconductance as a function of stress time even for a fixed gate length has a very complicated behavior. Indeed, such behavior is not steady but tends to decrease drastically for some specific values of the applied stress

time and under this situation, it becomes intractable to adopt a simple extrapolation or regression approaches.

Despite that it would be more interesting to apply the proposed lifetime forecasting approach for channel values beyond the 100 nm, we hope that this work will constitute the first step towards more rigorous contributions dealing with the lifetime prediction of nanoscale MOSFET devices. However, in this case, new numerical models should be implemented using Atlas 2D simulator with the accurate support of additional parasitic effects prevailing at this level.

V.5 Conclusion

In this work, we have been thoroughly interested in the reliability behavior of GAA JL MOSFET for channel lengths ranging from 800 nm to 100 nm. In order to account for the degradation resulted from the hot carrier injection, we have developed a numerical model using ATLAS-2D simulator including several ageing mechanisms. Numerical simulations have been conducted for a wide range of stress times to analyze the influence of stress conditions on the drain current and the transconductance. Moreover, we have adopted the relative degradation of the transconductance as a measure to predict the lifetime of the junctionless device using an ANFIS based approach. Therefore, the obtained findings have allowed us to confirm the appropriateness of the hybrid soft computing technique which is neuro-fuzzy computation tools for the forecasting of MOSFET reliability measures. As a future work direction, we intend to focus not only on supplementary input parameters (channel thickness, work function, doping concentration…etc) but also on the consideration of other degradation measures based on the threshold voltage or gate current variation.

Conclusion:

Conclusions and future work

VI Conclusions and future work

VI. 1 Contributions and conclusion

It is well-known that electronic circuits at nanoscale levels nowadays are very advanced, and they grow rapidly and in an unstoppable manner, Multi-gate MOSFETs have become very competitive in comparison with their conventional counterparts. Multi-gate transistors were first fabricated, in the early 1990s, since that time they have been considered as strange devices that are worthy just of academic research but far from industrial mass manufacturing. On May 4, 2011, however, semiconductor giant Intel announced its decision to use 3D tri-gate FET devices for its 22 nm technology instead of the planar one of 32 nm technology. And in the first half of 2015 again the 3D tri-gate FET devices in its 2nd generation (enhanced version) with less channels but higher for its 14 nm technology is available. This is a clear indication that planar MOSFET scaling is achieving its limits and that short channel effects (SCEs) can no longer be kept under control by using traditional planar transistor architectures. For this, the use of multi-gate transistors has become indispensable.

In this modest work, our two main aims are to find and study new design of multi-gate devices and investigate several soft computing techniques and use them as a tool to enhance these new designs. These soft computing techniques also help us to model, optimize, and predict the behavior of multi-gate MOSFETs in terms of their electrical performances for analog and RF applications.

Firstly, in chapter I, the reader is introduced to various concepts of the long channel and nanoscale MOSFET design. We have also presented an existing literature review of Multi-Gate transistor devices and various technologies especially double gate (DG) and Gate All Around (GAA) MOSFET transistors. This literature survey has helped to distinguish several unwanted effects related to the downscaling of the channel.

Secondly, in chapter II we have presented the main concepts related to several soft computing such as fuzzy logic (FL), Artificial Neural Network (ANN), Genetic Algorithm (GA) and hybrid techniques as well. In chapter III, we have proposed a new DGJL MOSFET design based on both gate material engineering and highly doped drain/source extensions and also we have developed an analytical model to the drain current. The analog/RF performance is compared between the proposed design and a

conventional DGJL MOSFET with similar dimensions, where the proposed device shows excellent ability in improving the analog/RF performance and provides higher drain current and improved figures-of-merit as compared to the conventional DGJL MOSFET. Moreover, the developed analytical models are used as mono-oba jective function to optimize the device analog/RF performance using Genetic Algorithms (GAs). In comparison with the reported numerical data for Inversion-Mode (IM) DG MOSFET, our optimized performance metrics for JL device exhibit enhancement over the reported data for IM device at the same channel length.

In chapter IV, the immunity behavior of the junctionless DG MOSFET device against the hot carrier degradation effect is studied. As a result, we have demonstrated that junctionless DG MOSFET can be a viable option to enhance the immunity performances of nanoscale CMOS-based devices technology for nanoelectronics digital applications. Moreover, the circuit performance parameters are developed incorporating the impact of dual-material gate engineering and highly doped extension regions on the performance of the common source single stage amplifier circuit based on DGJL MOSFET and we have analyzed the characteristics and circuit performance of the device. Based on the numerical outcomes satisfactory results are recorded in comparison with the conventional junctionless structure. Finally, in chapter V we have been thoroughly interested in the reliability behavior of GAA JL MOSFET for channel lengths ranging from 800 nm to 100 nm. In order to account for the degradation resulted from the hot carrier injection, we have developed a numerical model using ATLAS-2D simulator including several ageing mechanisms. Numerical simulations have been conducted for a wide range of stress times to analyze the influence of stress conditions on the drain current and the transconductance. Moreover, we have adopted the relative degradation of the transconductance as a measure to predict the lifetime of the junctionless device using an ANFIS based approach. Therefore, the obtained findings have allowed us to confirm the appropriateness of the hybrid soft computing technique which is a neuro-fuzzy computation tool for the forecasting of MOSFET reliability measures.

VI. 2 Suggestions for future work

No work is complete as knowledge is infinite. To go further, the following research tasks are suggested as future work in which we think further research should be carried on regarding advanced multi-gate devices.

In chapter III, where the investigation of the dual material DGJL MOSFET with highly doped S/D extensions has been conducted, the following aspects are to be considered:

- it is worthy to extend the proposed design using a triple material double-gate junctionless and compare the obtained outcomes with our current findings,
- we can enrich our design by introducing a linear or Gaussian doping at the level of the channel instead of the uniformly doped channel used in this dissertation,
- in terms of soft computing tools, it is recommended to exploit recent metaheuristics, which has proven best efficiency such as fire fly or bat algorithms,
- we aim at developing new figures of merit appropriate for realistic situations such as under thermal constraints, which requires the account of temperature as a relevant criterion,

In chapter IV, we have achieved the implementation of the proposed device in the framework of an inverter.

- Hence, we will employ this device for more circuits such as SRAM CELL.

As a future work direction for chapter V, efforts are accentuated on twofold objectives namely:

- we intend to add supplementary input parameters such as: channel thickness, oxide thickness, work function, doping concentration rather than limiting our model to a single geometrical parameter,
- besides using transconductance as a degradation measure, we can adopt other degradation measures based on threshold voltage or gate current in order to compare deduced lifetimes.

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