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Contribution to the modeling of III-V materials-based multi-gate transistors

Intitulée:

Contribution à la modélisation des transistors multi-grilles à base des matériaux III-V

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Abstract

While III-V-based FETs show some very attractive and tangible merits, there exist many difficult challenges to overcome before they will become applicable for future high speed and low-power logic applications. If the problems are indeed solved, III-V materials can play a major role along with Si in future logic and analog deep submicron devices. In this thesis, new designs of GaN-MESFET called multigate GaN-MESFETs and their 2-D analytical and numerical analysis have been proposed and investigated in order to improve the SCEs for future power switching and digital gate devices. It has been shown that the incorporation of the multigate design aspect exhibits an improvement in the screening of the channel potential variation, and an enhancement of the short-channel-effects. The found results from our study were discussed and compared to the conventional single-gate case, illustrating the improved subthreshold behavior of the Double Gate and the Gate All Around GaN-MESFETs over the conventional designs. On other hand, new Dual-Material-gate (DM) concept and optimization approach have been proposed to improve the device immunity against the short channel effects (SCEs) and optimize both the subthreshold electrical performances of the submicron Gallium Nitride (GaN)-MESFET and the analog electrical behavior of Gallium Arsenide (GaAs)-MESFETs for high speed submicron digital and analog applications, respectively. It has been analyzed that the DM design offers superior characteristics as compared to single material gate devices. In addition, a multi-objective genetic algorithms optimization (MOGAs) approaches are proposed to optimize the proposed designs in term of subthreshold and analog performances for high speed submicron digital applications and to search for optimal electrical and dimensional parameters to obtain better electrical performance of the device for analog and digital circuit applications.

Keywords: GaN MESFET, double gate, gate all around, dual material gate, multi-objective genetic algorithms optimization, subthreshold behavior

Résumé

Cependant les transistors FETs à base des matériaux III-V montrent quelques mérites très attractifs et tangibles, il existe de nombreux défis difficiles à surmonter avant qu'ils deviendront applicables pour future composant à grande vitesse de commutation et les applications numériques à faible puissance. Si les problèmes sont certainement résolus, les matériaux III-V peuvent jouer un rôle majeur avec le Si dans les futurs dispositifs logiques et analogiques fortement submicroniques. Dans cette thèse, de nouvelles conceptions de GaN MESFET appelées multi-grilles GaN-MESFET et leurs analyses bidimensionnelles et la modélisation numérique ont été proposées et étudiées afin d'améliorer les effets à canaux courts (ECC) pour la commutation de puissance et les futurs dispositifs numériques et analogiques. Il a été montré que l'implémentation de l'aspect de la conception multi-grilles présente une amélioration du comportement de potentiel du canal, et une amélioration des effets à canaux courts. Les résultats obtenus à partir de notre étude ont été discutés et comparés avec le cas des composants à une seule grille classique, illustrant l'amélioration du comportement sous le seuil pour des dispositifs à double grille et à grille enrobée en comparaison avec ceux à des conceptions classiques. D'autre part, une nouvelle conception de grille à dual (double) matériaux (DM) et une approche d'optimisation ont été proposées pour améliorer l'immunité des dispositifs contre les effets de canal court et des défauts d'interface afin d'optimiser les performances électriques sous le seuil du (GaN)-MESFET submicronique et le comportement électrique analogique de (GaAs)-MESFET pour des applications numériques submicroniques à haute vitesse et analogiques, respectivement. Il a été analysé que la conception DM offre des caractéristiques supérieures par rapport au dispositif à grille avec un seul matériau. De plus, des approches d'optimisation par des algorithmes génétiques multi-objectif (AGMO) sont proposées pour optimiser les conceptions proposées en terme de performances numériques et analogiques pour des applications submicroniques à haute vitesse et de rechercher des paramètres électriques et dimensionnels optimaux pour obtenir une meilleure performance électrique du dispositif pour les applications des circuits analogiques et numériques.

Mots clés : GaN MESFET, double grille, grille enrobée, grille à double matériaux, les algorithmes génétiques multi-objectif, comportement sous le seuil, analogique, submicronique.

ملخص

إن المركبات الالكترونية بمفعول الحقل الكهربائي المصنوعة بواسطة المعادن برهنت على كفاءتها و نوعيتها الرفيعة في مجال التطبيقات الرقمية و التشابهية في الترددات العالية. لكن, هناك مجموعة من العوائق و التحديات تمنع من تحسين أداء التصاميم المستعملة حاليا من تخطي مجالات الترددات العالية جدا. إذا, الهدف الرئيسي من هذه الرسالة هو اقتراح حلول و تصاميم جديدة من اجل تجاوز هذه العوائق و ذلك بتطوير نماذج رياضية جديدة تعتمد على التحليل تنائي الأبعاد للمركب الالكتروني وذلك من اجل تحسين خصائص سرعة التبديل للمركبات و كذا تحسين خصائص القنوات القصيرة, حيث أننا برهنا أن استعمال مفهوم المركبات متعددة البوابات و المعادن تسمح بتحسين خصائص المركب الالكتروني في المجالات الرقمية و التشابهية. قمنا في هذه الدراسة باقتراح نموذج جديد لتصميم المركبات الالكترونية باستعمال تقنية الخوارزمية الجينية المتعددة الأهداف و ذلك من اجل اقتراح التصاميم المثلى التي تسمح بتحسين خصائص المركب الالكتروني. النتائج المتحصل عليها سمحت لنا بالحصول على خصائص كهربائية عالية الجودة مقارنة مع التصاميم الكلاسيكية مما يثبت كفاءة النماذج الرياضية و التقنيات المقترحة في تصميم الدارات المتكاملة عالية الجودة.

كلمات المفاتيح: ثنائي البوابة, البوابة الدائرية, بوابة متعددة المعادن, الخوارزمية الجينية متعددة الأهداف, تطبيقات تشابهية

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Contents

Introduction

After four decades of successful scaling of transistors, the trend is reaching fundamental material limits. Much interest has been generated in exploring high mobility materials such as III-V, Ge, graphene, as replacements for Si channel to sustain future CMOS nodes [1]. The intrinsic properties of these materials may add to the challenge of successful device realization. Since III-V-based-materials have been a work horse in communications, optoelectronics and power electronic industries, they have been heavily researched. The success of III-V in potential CMOS technology will depends on heterogeneous integration on silicon with thinner buffer layers; compatible, low leakage and thermally stable gate dielectric with low interface state density, as well as defect free junctions with low external or access resistance. In addition, it is key to develop and orient various physical and electrical characterization techniques to probe and evaluate the interface and bulk characteristics effectively and correctly at the atomic level.

III-V-based semiconductor devices are not novel materials for digital circuits. GaAs-based digital integrated circuit (IC) utilizing mainly implanted n-channel MESFET were in production since the 1980s [1]. These ICs demonstrated almost an order of magnitude faster clocking speeds and 2–3 times intrinsic speed advantage over Si MOSFETs. The ICs with over 100 000 transistors directly-coupled GaAs MESFET gates per chip were commercially available in early 1990s and were employed in supercomputers, such as Convex C3800 and Cray-3 (with more modest gate-per-chip count). In fact, many thought that GaAs digital ICs would quickly replace silicon. However, the functional complexity of silicon chips was well ahead the GaAs ICs mainly due to low static power dissipation and simple circuitry of Si CMOS circuits. Digital GaAs ICs were pushed out of mainstream computing applications to data- and telecomm chips with the clock frequencies of 1–10 Gb/s and later 40 Gb/s and less-demanding complexity [1].

As technology scaling is pushing device dimensions into sub-0.1 μm regime, short channel effects and reliability issues have become areas of severe concern. Since conventional gate oxide thickness scaling gives rise to higher gate leakage, alternative approaches such as the use of gate engineering to alleviate these concerns will be a critical part of device design [2]. The continuous downscaling of FET-based technology

has made it attractive for system-on-chip applications, where the analog circuits are realized with the digital systems in the same integrated circuit to reduce the cost and improve the performance [3], [4]. But conventional FET-based technology is facing greater challenges in terms of scaling due to reduced gate control, increased short-channel effects (SCEs) and high leakage currents [5]. The double gate (DG) or multigate devices provide a better scalability option due to its excellent immunity to SCEs [6–8]. Due to the presence of second gate, the effective gate control increases, reducing DIBL. Also the channel is very lightly doped or undoped and this results in reduced mobility degradation. This technique also avoids random microscopic dopant fluctuations [9]. Numerous III-V-based FET structures have been reported and investigated to have reached this goal and optimized over the last few years [10-13]. However, these works have been focused to model and investigate the single gate device behavior by using numerical and analytical approaches. These conventional FET-based devices have some limitations and challenges in terms of scaling due to reduced gate control, high leakage currents and increased short-channel effects (SCEs). Therefore, new designs, approaches and techniques are required to overcome these limitations in order to improve the electrical performance for Large Scale Circuit Integration (LSCI) applications.

Evolutionary-based computation is a research area which involves applications of Evolutionary Computation in the domain of electronics. This new field of research has shown a potential which is attracting not only researchers, but also electronic circuit manufacturers, technology developers, end-users from the aerospace community, and engineers [14]. Our motivations, to use this computation approach, are various: the need of high performance electronic circuits with more sophisticated specifications; the increasing number of requirements that must be satisfied by a design in electronics; the appearance of more complex technologies; the availability of mature reconfigurable circuits platforms; the trend towards the achievement of fast, low-power and low area integrated circuits; the issue of fault tolerant systems for harsh environments; and the high cost of experienced electronic designers, mainly in analog electronics.

The main objective of this work is to propose new approaches and optimized III-V-based FET design using Multi-Objective Evolutionary Algorithms (MOEAs) and Multi-gate Engineering aspect to improve the electrical performance and the scaling capability of the device for the future high speed digital and analog circuit applications.

Layout of the Thesis

To make the work understandable and more consistent this thesis is divided into five chapters.

Chapter 1 presents an overview of the reasons for considering III-V materials in digital logic, as well as the challenges presented in their implementation. It also highlights the optical and electrical properties of wideband gap materials in a comparative manner taking into account their basic material parameters. Also the scope of applications of these materials in different areas is presented.

As one of the most widely used microwave devices, the gallium arsenide metal semiconductor field effect transistor (GaAs FET) dominates in modern MIC/MMIC applications. General overview of GaAs FET and the device model, followed by the concept of multi-gate technologies, problems solved by them and their limitations are given in chapter II. Chapter III covers the description of evolutionary computation and different evolutionary techniques. Also the discussion of the genetic algorithms in more detail and the concept of multi-objective optimization are described.

For the modeling of Gallium Nitride (GaN)-FET, new deep submicron double gate and Gate all around GaN MESFETs and their 2-D subthreshold analytical and numerical models are proposed and developed in chapter IV. Finally, chapter V is devoted to the study of new optimized Dual-Material-gate (DM) III-V MESFET-based design using Multi-Objective Genetic Algorithms. Results and discussions are also presented in this chapter. In conclusion, a few suggestions for future research directions are included.

Chapter I
III-V Materials and their applications

I.1 Introduction

Recently there has been much interest generated and good progress made in the study of non-Si electronic materials, such as carbon nanotubes, semiconductor nanowires and III-V materials, for future high-speed and low-power computation applications [15, 16]. These materials, in general, have significantly higher intrinsic mobility (either higher electron or hole mobility) than Si, and they can potentially be used to replace Si as the channel of the transistor for very high speed applications.

Long term research is focused on replacing charge-based electronics with spintronics, quantum computers, or optical computers [17]. In the near term, researchers are looking for ways to continue improving traditional devices with alternative materials and structures that could outperform silicon CMOS. Some possible options include nanotube or nanowire transistors [18], [19], and devices that incorporate III-V semiconductors [20].

This chapter will start with an overview on the III-V materials. After this, we will describe the challenges of III-V materials-based deep submicron devices, in which we will indicate that the GaN offers better electrical performance over conventional semiconductors. Finally, we will give an overview of different GaN-based application areas.

I.2 III-V Materials Overview

Most III-V semiconductors have a direct bandgap, thus making them highly suitable for optoelectronic applications. Motivation for consideration of III-V materials in traditional MOS transistor structures for digital applications is the extremely high electron mobility. This high mobility is a result of the electronic band structure of the material, and the small electron effective mass of the valley at the Γ point in k-space. Figure I.1a shows the band structure of silicon (indirect bandgap), and the parabolic effective mass approximation for the conduction band minima along the <100> (X) crystal direction. Conversely, figure I.1b is the band structure of gallium arsenide (GaAs), a common III-V material, with the parabolic approximation for the valley.

More curvature in the parabolic approximation corresponds to lighter effective mass and higher electron velocity and mobility. The light effective mass, as determined by the unique band structure of every material, may allow a logic device to be built from III-V materials that would operate much faster but at lower power than modern silicon devices [20]. However, this idea has proven difficult to confirm experimentally, mainly due to the challenges associated with fabricating even the simplest III-V devices on a very small scale.

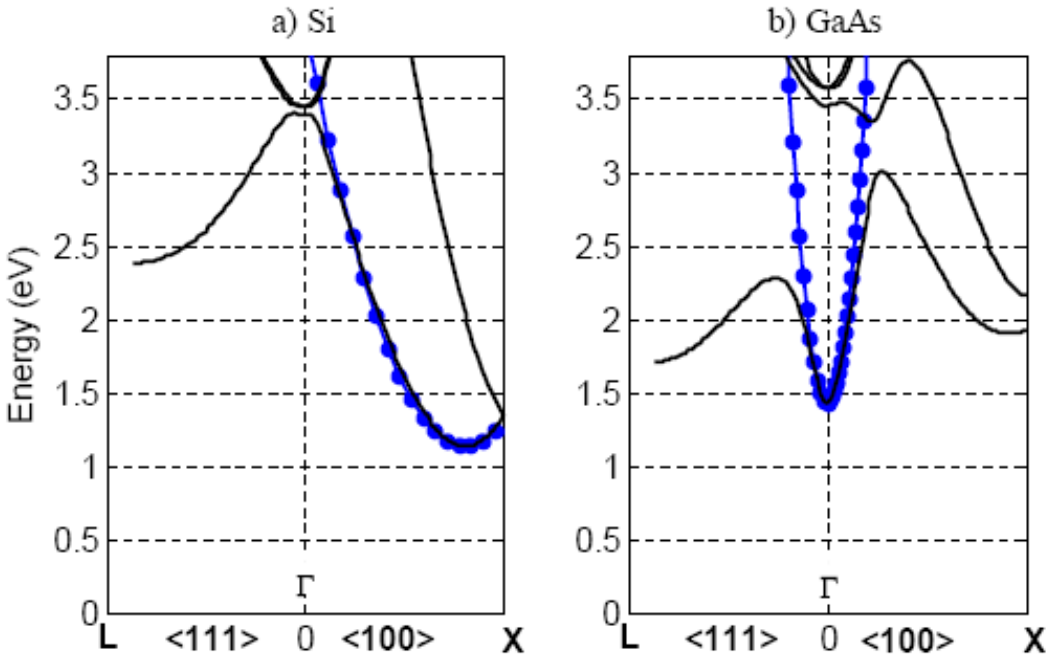


Figure I.1: Electronic band structure of two common semiconductors calculated for the bulk case [21], and their respective parabolic fit (circles). Zero energy corresponds to the top of the valence band. a) Si conduction band is shown with a parabolic fit in the X direction corresponding to $m^*=0.91m_0$. b) GaAs band structure showing the parabola at the point where the effective mass is very light ($m^*=0.067m_0$).

I.3 Challenges of Implementing III-V Materials in deep submicron devices

Silicon was chosen as the channel material in the early stages of integrated circuit fabrication because it was easy to form a stable insulator with a high quality interface on the surface simply through oxidation (silicon dioxide, SiO_2). The recent introduction of high-k insulators like hafnium dioxide (HfO_2) and metal device contacts in place of polycrystalline silicon [22] represent the first changes to the fundamental material composition of electronic devices for digital applications in decades. Similar fabrication and materials challenges are faced for successful III-V implementation, the most prominent being high-k dielectrics with quality interfaces. Techniques to fabricate

structures and deposit the insulators, such as molecular beam epitaxy (MBE) [23] and atomic layer deposition (ALD) [24] are currently being used, and the latter is delivering relatively good results. Unfortunately, it is difficult to argue the economic feasibility of these methods in large-scale integration at this time. In addition to the high-k problem, the light electron masses in III-V materials make them highly susceptible to electron tunneling effects, and achieving a small device with acceptable leakage will prove difficult. Finally, III-V materials lack a hole mobility advantage. Thus, p-type devices needed for CMOS technology may make it necessary to incorporate the III-V on silicon or other substrate [20].

Because of the fabrication challenges, modeling and simulation could help predict whether III-V devices will offer a significant advantage over silicon. However, III-V materials can be difficult to model. The effective mass fit shown in figure I.1b for GaAs is already highly suspect because of the non-parabolicity of the valley. Then, there is complication due to the valleys in the L and X directions, which are only a few hundred meV above the bandgap, both with a heavy effective mass. In many situations, it is important to consider some or all of the upper valleys, and mathematical transformations of the effective masses into the appropriate coordinate system are necessary. In the case of strong quantum confinement and the differences in effective mass (even including energy offset of the valleys) will cause the X, L, and Γ subbands to re-order, with the X lowest in energy. This situation is not believed to be realistic, and a model with the proper effective masses or one which incorporates the full band structure is needed. Unfortunately, treating the full band structure can be computationally expensive when including sophisticated electron transport calculations. All these issues will be addressed in this work to attain an accurate conclusion about the performance potential of III-V materials in deep submicron transistors.

I.4 Material properties

Table I.1 shows the fundamental material properties of GaN, SiC, diamond, Si, GaAs, and InP that are most important to electronic device performance [25, 26, 27].

A large bandgap energy (Eg) results in high electric breakdown fields (Ec), which enable the application of high supply voltages. Furthermore, it allows the material to withstand high operating temperatures and provides for improved radiation hardness. GaN and SiC have bandgap energies about two to three times those of conventional semiconductors such as Si, GaAs, and InP. The electric breakdown fields for the wide

bandgap (WBG) materials are excellent and very high, typically one order of magnitude larger than for the conventional semiconductors.

Generally, to achieve high currents and high frequency operation, high charge carrier mobility (μ) and high saturation velocity (v_{sat}) are desirable. The high value for electron mobility of GaAs (8500 cm^2/Vs) is the main reason that field-effect transistors (FETs) fabricated from this material have such excellent high-frequency performance. A primary disadvantage of fabricating transistors from bulk GaN and SiC is the relatively low values for the electron mobilities, which are 900 cm^2/Vs for GaN and depending on the polytype approximately 700 cm^2/Vs for SiC. However, these values are sufficient for transistors specifically designed for high-power operation. In general, wide bandgap semiconductors have relatively low mobility but very high values for the saturation velocity, which is reached at high electric fields that can easily be supported. The mobility and saturation velocity of the 2DEG at the $Al_xGa_{1-x}N$/GaN heterojunction is very suitable for high-power, high-frequency device applications. The room temperature (RT) mobility of the 2DEG, which is typically between 1200 cm^2/Vs and 2000 cm^2/Vs, is significantly better than that of bulk GaN and SiC.

The thermal conductivity (κ) of a semiconductor material is extremely important since this parameter is a measure for the ease with which dissipated power can be extracted from the device. Poor thermal conductivity leads to degraded device operation at elevated temperatures. In general, conventional semiconductors are poor thermal conductors, particularly GaAs and InP. Conversely, SiC and especially diamond are excellent thermal conductors and GaN is comparable with Si, the best of the conventional semiconductors.

Table I.1: Material properties of conventional and wide bandgap semiconductors at 300 K [25,26, 27].

Property	GaN AlGaN/ GaN	SiC	Diamond	Si	GaAs AlGaAs/ InGaAs	InP InAlAs InGaAs
Bandgap Energy, E_g (eV)	3.44	3.26	5.45	1.12	1.43	1.35
Electric breakdown field, E_c (MV/cm)	3	3	10	0.3	0.4	0.5
Saturated (peak) velocity electrons, v_{sat} (v_{peak}) ($\times 10^7$cm/s)	2.5 (2.7)	2.0 (2.0)	2.7	1.0 (1.0)	1.0 (2.1)	1.0 (2.3)
Electron mobility, μ_n (cm^2/V.s)	900 2000$^{\alpha}$	700	4800	1500	8500 10,000$^{\beta}$	5400 10,000$^{\chi}$
2DEG density, n_s ($\times 10^{13}$ cm^{-2})	1.0	N.A	N.A	N.A	<0.2	<0.2
Thermal Conductivity, κ (W/cm.K)	1.3-2.1	3.7-4.5	22	1.5	0.5	0.7
Relative Permittivity, ε_r	9.0	10.1	5.5	11.8	12.8	12.5

$^{\alpha, \beta, \chi}$ values for the corresponding heterostructures.

The relative permittivity (ε_r) is an indication of the capacitive loading of a transistor and affects the device terminal impedances. Table I.1 shows that the values of ε_r for the WBG semiconductors are considerably lower than those for the conventional semiconductors. In the case of GaN and SiC the values of ε_r are about 20% lower whereas for diamond the value of ε_r is even about 55% lower. This permits for example

a GaN device to be about 20% larger in area for a given impedance. As a consequence, this increased area enables the generation of larger currents and higher microwave output power.

For a better comparison of the possible high-power and high-frequency performance of different semiconductor materials, several figures of merit have been proposed. These figures of merit combine the most relevant material properties with respect to high-power and high-frequency applications into one number that represents a rough measure of the relative strengths of the alternative materials. Johnson's figure of merit (JFOM) [28] takes into account the breakdown voltage and saturated electron drift velocity in defining a value for the high-frequency handling capability of a certain semiconductor. For GaN, the JFOM is 728 times that of silicon, about 93 times that of GaAs, and about twice that of SiC. Baliga's figure of merit (BFOM) [29] is calculated based on the relative permittivity, electron mobility, and electric breakdown field and is a measure for the high-power handling capability. Based on its properties, the BFOM for GaN is about 133 times that of Si, 11 times that of GaAs and three times that of SiC [30]. Form these figures it is very clear that GaN offers much better high-power/high-frequency performance possibilities than GaAs and SiC.

I.5 Application areas

The direct bandgap of GaN and its alloys enables the material to be used for both optical and electronic applications. At 300 K the bandgap of GaN is 3.44 eV which corresponds to a wavelength in the near ultra violet (UV) region of the optical spectrum. Figure I.2 shows a plot of the bandgap energy versus lattice constant in combination with the visible optical spectrum for various semiconductors including the wide-bandgap materials SiC, GaN and its alloys indium nitride (InN) and aluminum nitride (AlN). It can be seen that the $Al_xIn_yGa_{1-x-y}N$ alloys cover bandgap energies from 1.9 eV to 6.2 eV, which correspond to wavelengths ranging from red to deep UV.

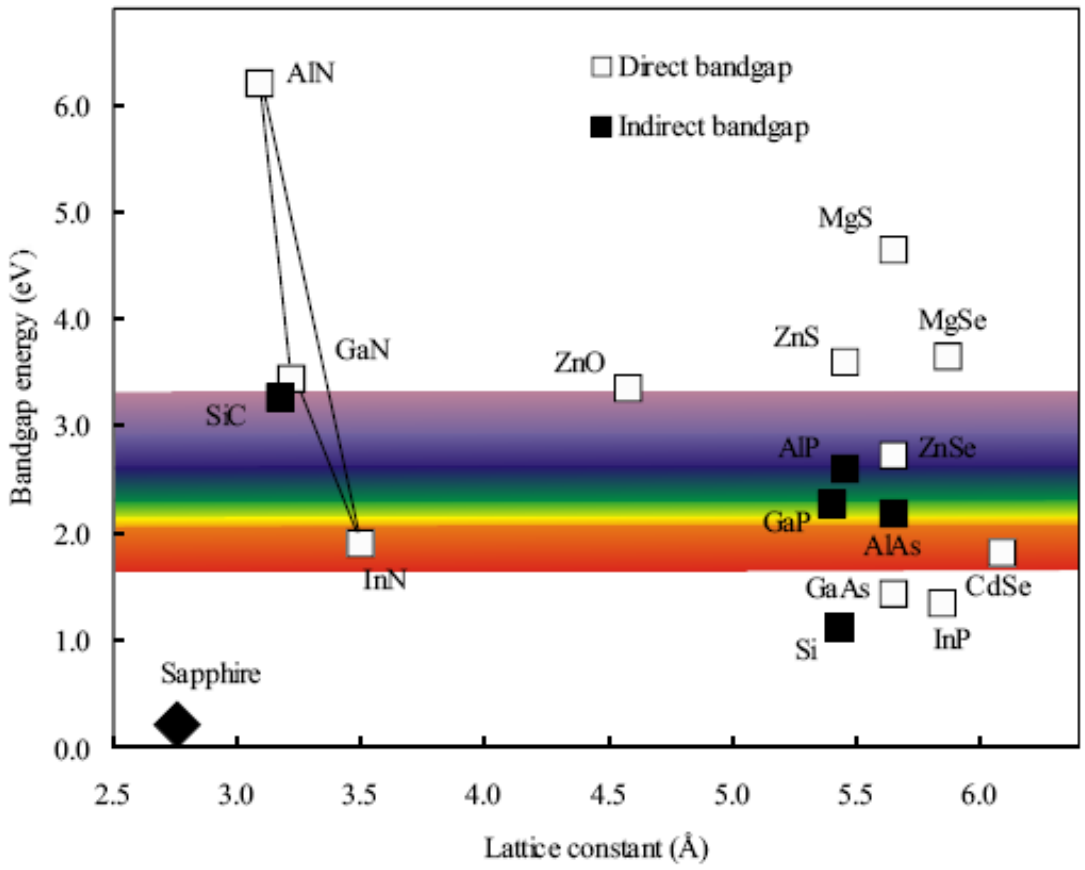


Figure I.2: Bandgap energy versus lattice constant for various semiconductors including the wide-bandgap materials SiC and GaN with its alloys [31].

I.5.1 Optical applications

In 1968 James Tietjen, working at the Materials Research Division of the Radio Corporation of America (RCA), came up with the idea to develop a flat television that could be hung on the wall like a painting. A full color image can be created combining red, green, and blue pixels in the display. Red and green LEDs were available using gallium arsenide phosphide ($GaAs_{1-x}P_x$) and gallium phosphide nitride (GaP:N) materials, respectively. All that was missing to realise a flat LED-based television set was a bright blue LED. These devices became available using either SiC or II-VI compounds such as zinc oxide (ZnO). However, because of their indirect bandgap SiC LEDs were not very efficient. The devices based on II-VI compounds mainly suffered from much too short lifetimes for commercial applications. Hence these devices could not be used in the envisioned display application. This void in solid-state lighting was filled in 1993 by Nakamura et al. [32]. By realizing high-brightness blue GaN-based

LEDs that were about 100 times brighter than the previous blue SiC LEDs they made feasible the daylight visible full color display application.

- LED applications

The main economical benefits of LED-based lighting are low power requirement, high efficiency, and long lifetime. In addition, solid-state design renders LEDs impervious to electrical and mechanical shock, vibration, frequent switching and environmental extremes. Several major markets are being addressed with these newly developed solid-state light sources. Automobile exterior lighting has been moving rapidly to incorporate transparent-substrate $Al_xIn_yGa_{1-x-y}P$ technology into high-mount braking lights and into the full amber and red-orange taillight assembly. Full-color, outdoor, changeable message signs and full-motion video displays have been adopting $Al_xIn_yGa_{1-x-y}N$ and $Al_xIn_yGa_{1-x-y}P$ technologies and will continue to proliferate as costs are reduced. Traffic-signal applications have begun to incorporate red AlInGaP and AlGaAs LEDs for traffic lights and are moving toward incorporating amber and blue-green LEDs to produce a completely LED-based signal head. All of these markets are rapidly expanding and will provide enormous growth opportunities in the future.

By using multiple LEDs, an LED cluster lamp continues to provide light even if one or more emitters fail unlike when the filament breaks in an incandescent bulb. Taking also into account an average life span of more than 100,000 hours (approximately 11 years), LEDs operate reliably year after year and are an excellent replacement for incandescent bulbs in hard-to-reach places and environments that depend on reliable lighting (e.g. hospitals, airports). Furthermore, colored lenses or filters are not needed since LEDs emit colored light that is determined by the composition of the semiconductor material comprising the diode. As LEDs are an energy-efficient light source and are virtually maintenance free, the cost savings are substantial. Other important GaN-based LED applications are backlighting (cell phones, PDAs), white light (flashlights, car head lights), general lighting (interior and exterior), water purification systems, and medical (sensors, surgical goggles).

- Laser applications

Infra-red AlGaAs-based and red AlInGaP-based laser diodes (LDs), such as those in today's CD and DVD systems, have been around for decades. To increase the storage capacity on a CD, the pit size must be made smaller. A shorter wavelength LD is

required to focus onto the smaller pit size. The current generation of DVD systems uses a LD with an emission wavelength of 650 nm. In the last few years the market for DVD systems has increased rapidly. However, the majority of these systems is read-only and is based on a 5 mW AlInGaP LD emitting at 650 nm. For further advances in the market recordable DVD was an obvious necessity. This required higher output power from the 650 nm LD (typically 30 - 40 mW). To also achieve faster read/write speeds even higher powers are required.

GaN-based blue-violet LDs with an emission wavelength of 405 nm will be the cornerstone of next-generation DVD player-recorders and optical high-density data-storage systems for computers. Using these components it is already possible to write huge amounts of data (27 GB) on a single-layer 12 cm DVD disk which is almost six times the storage capacity possible with ordinary red LDs. This is enough to store more than two hours of high-definition (HD) video or 13 hours of standard-definition (SD) video.

In 2003, Tokyo-based Sony Corporation was the first consumer electronics company to begin offering next-generation DVD recorders. Sony leads a consortium called Blu-ray Disc, which is pushing one of two competing standards for the design of the discs, players, and recorders that use blue GaN-based LDs. The consortium further consists of the following major consumer electronics companies: Hitachi, LG Electronics, Matsushita Electric Industrial, Pioneer, Royal Philips Electronics, Samsung Electronics, Sharp, and Thomson. The other standard, high-density DVD (HD-DVD), has been proposed by Toshiba, Sanyo, and NEC [33]. Other GaN-based LD applications are laser printing, projection displays, and medical.

GaN-based blue LDs are used for the laser-induced fluorescence method (LIF) employing endogenous ("autofluorescence") and exogenous fluorophores. LIF is applied for clinical diagnosis in dermatology, gynecology, urology, lung tumors as well as for early dentin caries. The LIF method, which is fundamental for many medical applications, uses excitation radiation with a wavelength around 400 nm that could only be applied using tunable dye lasers or titanium lasers. This makes it only adequate for laboratory investigations. Development of GaN-based LDs provides the possibility to design portable, compact diagnostic devices as multi-channel analyzers of fluorescence spectra and surface imaging devoted to clinical applications. The designed systems used for spectra measurement and registration of fluorescence images include LDs with an output power of 5 - 30 mW at wavelengths of 405 - 407 nm. Dentistry diagnosis is a

new field in which GaN-based LDs can be applied. After induction with blue light, decreased autofluorescence intensity can be observed when dentin caries occur [34].

I.5.2 Electronic applications

With respect to electronics, GaN is an excellent option for high-power/high-temperature microwave applications because of its high electric breakdown field (3 MV/cm) and high electron saturation velocity (1.5 x 10^7 cm/s). The former is a result of the wide bandgap (3.44 eV at room temperature) and enables the application of high supply voltages, which is one of the two requirements for high-power device performance. In addition, the wide bandgap allows the material to withstand high operating temperatures (300^{o}C - 500^{o}C). A big advantage of GaN over SiC is the possibility to grow heterostructures, e.g. AlGaN/GaN. The resulting two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction serves as the conductive channel. Large drain currents (> 1 A/mm), which are the second requirement for a power device, can be achieved because of the high electron sheet densities (1 x 10^{13} cm^{-2}) and mobilities (1500 - 2000 cm^2/Vs). These material properties clearly indicate why GaN is a serious candidate for next-generation microwave high-power/high-temperature applications. Figure I.3 shows an overview of GaN-based micro-electronic applications.

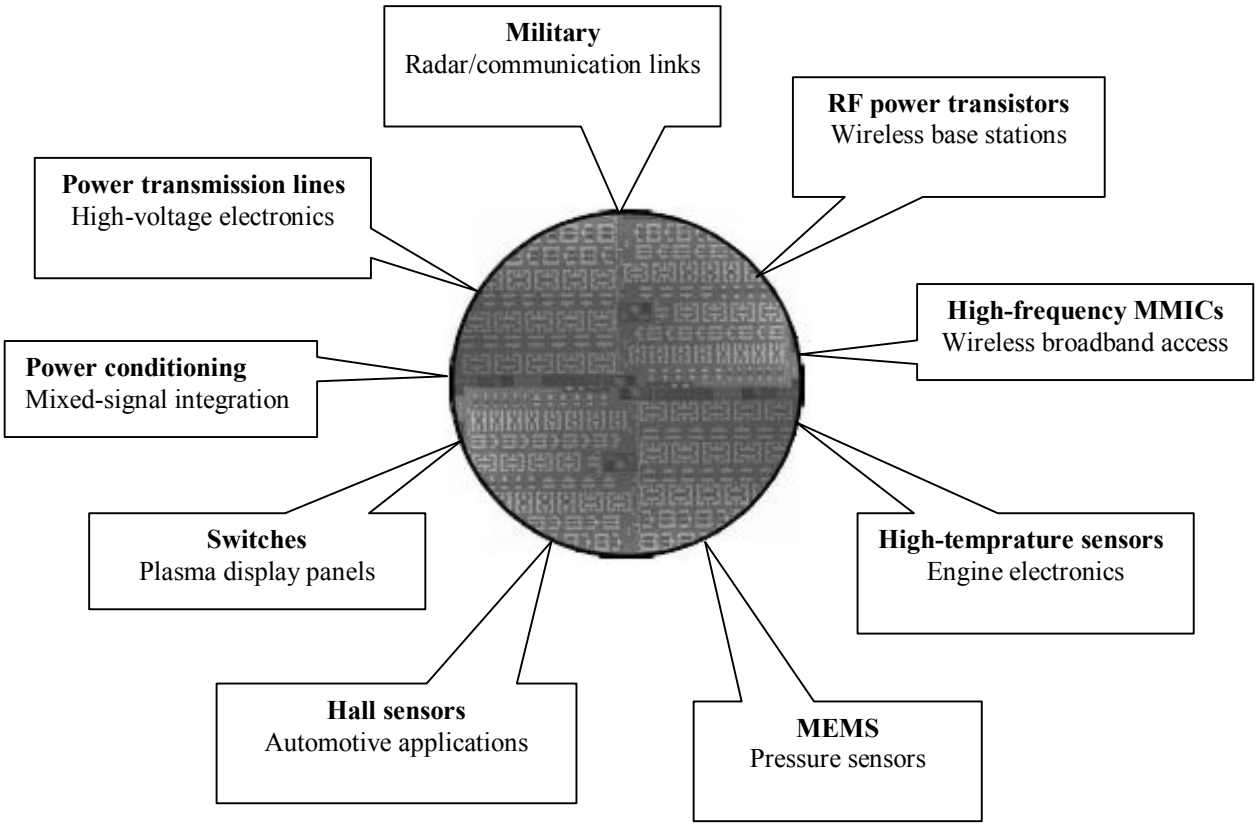


Figure I.3: GaN-based micro-electronic applications [35].

- Military applications

Despite the superior material properties and expected advances in device and system performance, the driving force behind research towards GaN-based microwave high-power/high temperature electronics over the last decade has been almost exclusively military in nature. The main reason for this is the enormous costs that are involved with the early stages of GaN electronic device research. Several European countries, including France, Germany, United Kingdom, Italy, Spain, Sweden, and the Netherlands have defense oriented research programs, some of which are joint efforts such as the Swedish - Dutch SiC and GaN program (period: 2000 - 2005) and the new very big European GaN program KORRIGAN (Key Organization for Research on Integrated Circuits in GaN Technology) (period: 2005 - 2009). The frontiers of academic and military research and the commercialization of GaN-based electronics however are mainly in the US and to a lesser extent in Japan. US and Japanese research programs towards military microwave systems have been and continue to be heavily funded by the respective Departments of Defense (DoD). The US's Defense Advanced Research Projects Agency (DARPA) has granted a huge GaN program, total investment

up to $144.5 million, with a triple-pronged approach to speed up the development of GaN-based microelectronics and assure a rapid transition into military systems. Former research programs have focused on achieving hero values with respect to current densities and output power densities at microwave frequencies in order to prove the high expectations. The new programs however start for the basics (material growth, etching, contacts) and move through the stage of discrete devices to the eventual goal of GaN-based microwave monolithic integrated circuits (MMICs). The focus now is on understanding the physical reasons behind device failures and the development of physical models to predict performance in order to increase reproducibility and reliability. In general, defense research programs focus on the development of GaN technology for use in components such as surface radars, broadband seekers, jammers, battlefield communication, satellite communication links, transmit/receive modules, broadband high-power amplifiers (HPAs), and low noise amplifiers (LNAs). The frequencies of interest for these applications range from 2 GHz - 40 GHz.

- Commercial applications

Commercial GaN-based applications are on the verge of their breakthrough. The first products will most probably be high-efficiency and high-linearity power amplifiers for base-stations, which power 3G wireless broadband cellular networks in the so-called S-band (2 GHz – 4 GHz). The US-based company RF Micro Devices (RFMD), the biggest player in this field, announced that it has sampled 100 W GaN amplifiers to customers early 2005. Competition can be expected from Japanese companies Fujitsu, Matsushita Electric, and OKI Electric [36]. Other high-volume commercial applications in which GaN-based electronics could lead to significant performance enhancement and cost reduction are high-frequency MMICs (wireless broadband communication links), hybrid electric vehicles (DC-AC conversion), high temperature electronics (automotive, energy production), switches (plasma display panels, low-frequency high-power switching), high-voltage power rectifiers (inverter modules), microelectro- mechanical systems, MEMS (pressure sensors), and Hall sensors (automotive applications).

Current hybrid electric vehicle (HEV) platforms, which use silicon-based power electronics, are faced with two major challenges: size and weight. In addition to traditional cars containing internal combustion engines (ICEs), HEVs must also accommodate power electronics, energy storage, and an electric motor in the predefined volume of the automobile platform. The HEV's motor drive, a power-electronics

component that converts stored energy into an alternating-current (AC) source needed to operate the electric motor, is one of the main contributors to the system's size and weight. Typically, HEV motor drives use silicon insulated gate bipolar transistors (IGBTs) for the primary switching element, with Si p-i-n diodes as the fly-back diode, configured in a module designed to control three-phase motors. The module is positioned inside the engine compartment as close to the electric motor as possible to minimize parasitic inductance and reduce cabling weight. However, like all silicon devices they are limited to junction temperatures of 150°C - 175°C. Controlling the junction temperature of the Si electronics in the engine compartment's harsh environment requires large heat sinks and liquid cooling, but both these solutions are costly and difficult to integrate into the volume available within the engine compartment. The temperature limitations inherent to Si technology mean that state-of-the-art Si electronic components cannot meet the demands of HEV platforms to produce smaller, lighter, and cheaper electrical systems.

Besides the great opportunities that GaN-based high-temperature electronics present to HEVs, they also offer important capabilities to aerospace, energy production, and other industrial systems that will affect modern everyday life. The inherent ability of a GaN junction to properly rectify with low reverse leakage current at junction temperatures as high as 600°C enables power-device operation at higher ambient temperatures. In addition, superior power switching properties of wide bandgap devices are also present at room temperature ambient [37]. Therefore, if remaining technical challenges (e.g. material with low defect density, temperature stable contacts, and reliable packaging technologies) can be overcome, GaN is likely to play a critical role in realizing high-power electronics beyond the capability of Si at all temperatures. For low-power circuits, GaN-based electronics will likely be relegated to the temperature range beyond the reach of silicon-on-insulator (SOI) electronics, which appears to be above 300°C [38].

High-voltage power rectifiers are key components of inverter modules, which are used in power flow control circuits. Lateral AlGaN-based Schottky rectifiers with spacing of 100 μm between the Schottky and ohmic metal contacts have shown reverse blocking voltages up to 9.7 kV. The figure of merit V_B^2 / R_{on}, where V_B is the reverse breakdown voltage and R_{on} is the on-state resistance, was as high as 270 MW/cm^2 for these devices [39].

I.6 Conclusion

The III-V materials are prominent for applications of optoelectronics and electronic devices. In addition, III-V semiconductors have a potential for higher speed operation than silicon and Germanium semiconductors in electronics applications, with particular importance for areas such as wireless communications. This chapter has been focused to present a brief overview of the reasons for considering III-V materials in future high-speed and low-power computational devices, as well as the challenges presented in their implementations. The remainder of the chapter presents the material proprieties and different application areas.

Chapter II
III-V Semiconductors-based electronic devices

II.1 Introduction

Over the past three decades, by reducing the transistor lengths and the gate oxide thickness along with decreasing the supply voltage, there has been a steady improvement in transistor performance a reduction in transistor size and a reduction in cost per function. The more an Integrated circuit (IC) is down scaled, the higher becomes its packing density, the higher its circuit speed, and the lower its power dissipation [40]. Today's Integrated Circuits use the MOSFET as a basic switching element for digital logic applications and as an amplifier for analog applications. Although the basic architecture of the device has remained the same, the physical size has been continuously reduced by factor of two every 2-3 years in accordance with Moore's Law [41] (Figure II.1). However, as CMOS dimensions start approaching the nanometer regime (<100 nm), we start seeing new effects in the device performance arising from new physical phenomenon. To maintain the rate of improvement in device performance with continued down scaling, both industry and academia have been investigating alternative device architectures and materials, among which III-V compound semiconductor transistors stand out as promising candidates for future logic applications because their light effective masses lead to high electron mobilities and high on-currents, which should translate into high device performance at low supply voltage.

This chapter, primarily, deals with mathematical description of *I-V* characteristics of both long channel and short-channel FETs. It describes the different MOSFET structures which can offer the opportunity to continue scaling. It will also represent the problems solved by multi-gate FETs and their limitations.

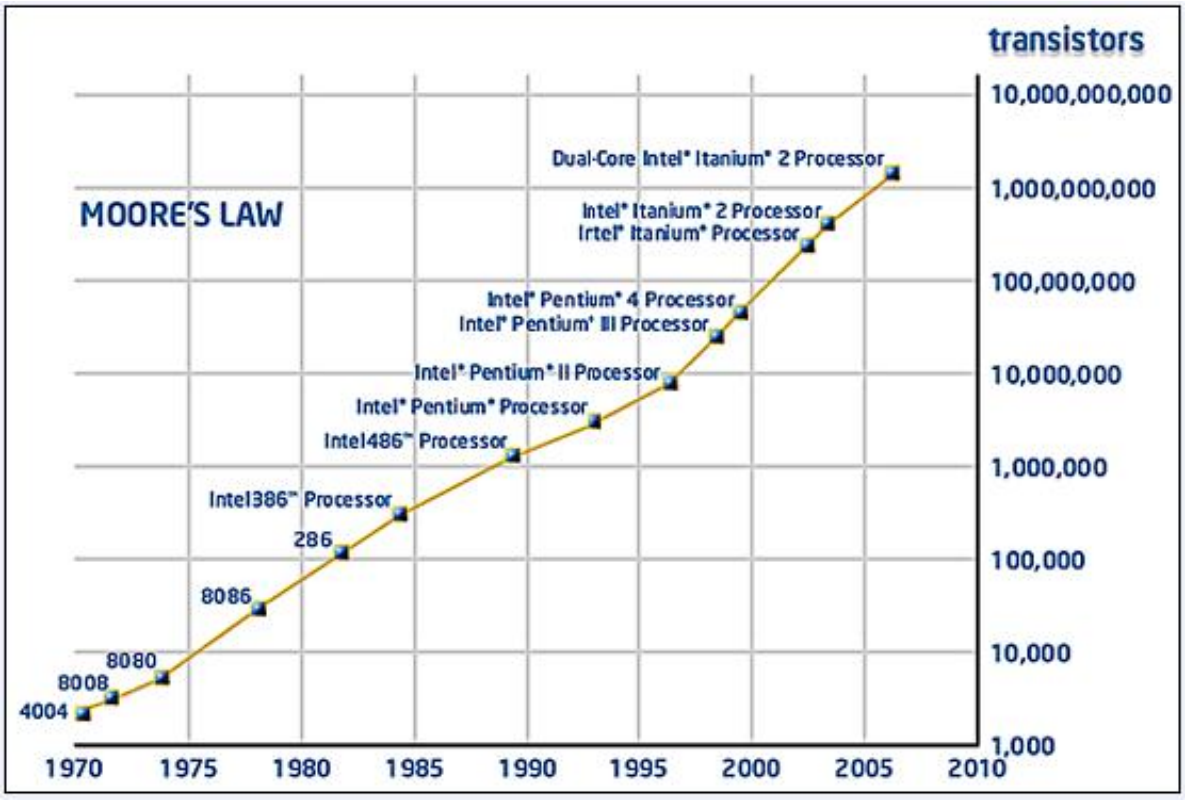


Figure II.1: Increasing number transistors with each new microprocessor technology [42]

II.2 Overview of GaAs-based FET

The first development of a prototype gallium arsenide field effect transistor using a Schottky gate was undertaken by Mead in 1966 [43]. In 1967, a GaAs MESFET was first fabricated by Hopper and Lehrer [44]. A significant step was made by Turner et al in 1971 [45], when 1 μm gate length GaAs MESFET was fabricated, giving f_{max} equal to 50GHz and useful gain up to 18GHz. With the development of the quality of GaAs materials and basic FET prototype technology, rapid progress was achieved for GaAs MESFET devices in the direction of both low noise and high power applications. The first low noise GaAs MESFET was reported by Leichti et al. [46] in 1972. And later in 1973, the first high power GaAs MESFET was announced by Fukuta et al. in Fujitsu [47]. With the early progress of GaAs MESFET technology, this had been followed by rapid improvement of the device performance. Intensive studies have been done in increasing its output power, operating frequency and power added efficiency as well as improving the distortion qualities and noise figure.

In addition to the discrete FET area, there also has been rapid development in both monolithic microwave integrated circuits (MMICs) and digital GaAs integrated circuits. MMIC technology has become popular since middle 1970s, and the first GaAs digital IC was reported in 1974 [48].

In the late 70s and the 80s, the GaAs MESFET was developed mainly for low volume, high performance military and space based systems. The manufacturing technology was not mature enough to support the cost and volume requirement for the consumer mass market. By the early 1990s, however, GaAs MESFET manufacturing technology was maturing rapidly, cost was reduced. As a result, GaAs technology became more competitive with other process technologies. Since then, the GaAs MESFET device and GaAs integrated circuits have found a wide range of applications, such as in wireless systems. Now, the GaAs MESFET is widely used in different microwave and millimeter wave systems, and has become the most important active device in both hybrid and monolithic microwave integrated circuits (HMIC and MMIC) design. Typical applications include both low noise and power amplifiers, as well as transfer switches, attenuators, oscillators, and mixers. The demand for mobile and personal communication systems has increased the use of GaAs MESFET for high-speed digital and analog integrated circuits.

In recent years, GaAs MESFET technology is also facing serious competition from silicon and silicon-germanium technologies in RF and microwave applications. CMOS continues to advance to smaller geometries. SiGe BiCMOS gives good performance for RF and high speed. Compared to silicon, GaAs has a higher electron mobility and peak drift velocity. The electron velocity at low field is sufficiently high so that high switching speed and therefore high cut-off frequency can be achieved. The primary advantages for using GaAs over silicon are large transconductance, low ON resistance, and fast switching speed. Unlike Silicon, a semi-insulting GaAs substrate can be formed. This contributes to the simple structure of the GaAs MESFET, and the high resistivity of the GaAs substrate results in very small parasitic capacitance. GaAs technology also has the strength of integrating RF functions in stripline and coplanar design into MMICs.

II.3 GaAs-based FET fabrication

A microwave GaAs MESFET device is fabricated using semi-insulating GaAs substrate. GaAs has attractive features at high frequencies compared to Silicon. The

substantial improvement in FET performance by using GaAs substrate over the Silicon is mainly attributed to the fact that:

- The conduction band electrons in GaAs have approximately six times higher mobility and twice the peak drift velocity as that of Silicon. This leads to low parasitic resistances, large transconductance and shorter transit time.
- The larger band gap in GaAs devices allows higher working temperature. This is particularly important in the small geometry of power devices which are used at microwave frequencies and dissipates a lot of heat. Furthermore, due to the relatively large band gap, GaAs devices operating at room temperature offer low thermal leakage current and thus provide a low noise figure.

In MESFET fabrication, a thin epitaxial layer of *n*-type GaAs is deposited on a semi-insulating GaAs substrate (figure II.2). The optimum value of doping concentration in the epi-layer depends on the maximum allowed gate leakage current. For a given doping concentration optimum value of active channel thickness, a is a function of gate length, L_G. It has been shown that optimum doping level for low noise *mm*-wave length device is ~ 5 x 10^{17} cm^{-3} [49]. Ladbrooke has reported that for a good L_G / a ratio which is commonly known as the aspect ratio, should be in the range of 3-5 [50]. Dambkes have reported the smallest acceptable value of L_G / a for a low-noise MESFET is 3 [51]. According to a review by Golio, most reported devices have been fabricated with L_G / a ratio that lies between 2-10 [52].

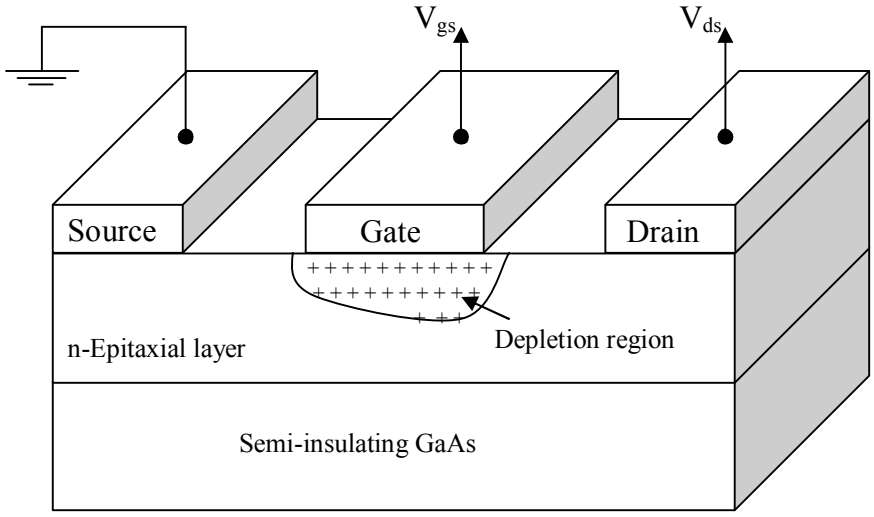


Figure II.2: A cross-sectional view of a GaAs MESFET fabricated on a semi-insulating GaAs substrate

A *mm*-wave length low noise GaAs MESFET has drain-source separation ≤ 1εm, with $L_G \leq 0.5$ εm. Drain and Source ohmic contacts are fabricated by using AuGeNi alloy which is annealed to reduce ohmic resistance. After the gate lithography, Schottky barrier gate is usually fabricated by employing Ti/Au metals, where Ti is used to provide adhesiveness to Au.

II.4 MESFET's Operation

The operation of a GaAs MESFET is similar to Si JFET, but the only difference is, in GaAs MESFET a metal semiconductor rectifying contact is used at the gate instead of a *pn* junction of a JFET [53, 54]. A MESFET device is biased by applying two voltages, V_{gs} and V_{ds} [55]. These voltages are used to control I_{ds}, which is present between the drain and the source of the device, by varying the electric field inside the channel. The field changes by changing the applied potential, giving rise to three distinct regions in the *I-V* characteristics of the device namely:

- Linear Region;
- Saturation Region and
- Pinch-off Region.

To simulate the dependence of I_{ds} on V_{gs} and V_{ds}, the field distribution inside the channel, which is dependent on device geometry, should be known [56, 57, 58]. Microwave MESFETs are of submicron gate length; called short channel devices having $L_G < a$ and usually fabricated by employing the gate recess technology [59, 60, 61]. Whereas low frequency devices having $L_G > a$ are called long channel devices [62, 63, 64].

II.4.1 Long Channel Model

MESFETs fabricated by employing the condition $L_G > a$ are called long channel devices and the model that describes the behavior of such devices is termed as long channel model. It was first presented by Shockley in 1951 [65]. To describe the basic mechanism involved in the Shockley model, consider a cross sectional view of a GaAs MESFET shown in Figure II.3. In this figure L_G is the channel length, h is the depletion width, $V(x)$ is the voltage drop underneath the gate, a is the epi-layer thickness, W_d and W_s represent width of the depletion at drain and source sides of the device respectively and $A(x)$ is the available channel height defined as

$$A(x) = a - h(x) \qquad \text{(II.1)}$$

Here $A(x)$ is a function of x because the electrons are flowing from source to drain

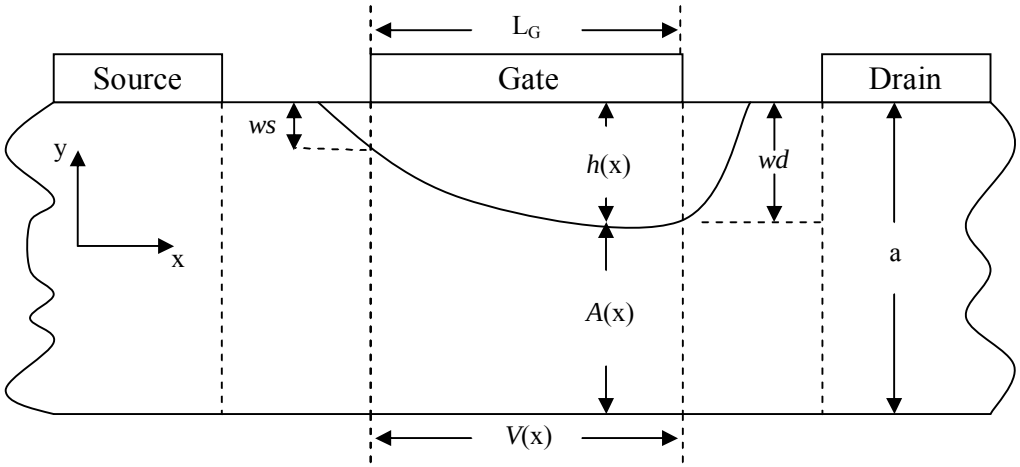


Figure II.3: A cross-sectional view of a biased GaAs MESFET channel.

Giving rise to a voltage drop $V(x)$ along the channel which varies from zero at the source end to V_{ds} at the drain side of the device. The potential difference between the gate and the channel at any point x is, therefore, given as

$$V_1 = \Phi_b - V_{gs} + V(x) \qquad \text{(II.2)}$$

here $\bar{\boldsymbol{u}}_b$ is the Schottky barrier height.

In order to calculate the width of the depletion layer formed by the Schottky barrier, it is assumed that the junction is abrupt and all the donor atoms (N_d) are ionized [66]. Under such conditions the two-dimensional Poisson's equation can be written as [66]

$$\frac{\partial^2 \Phi_b}{\partial x^2} + \frac{\partial^2 \Phi_b}{\partial y^2} = -\frac{q}{\varepsilon_s} N_d \qquad \text{(II.3)}$$

If we also assume that the variation of the potential along the length of the channel is negligibly small compared to y-directed field then Equation (II.3) can be modified as

$$\frac{\partial^2 \Phi_b}{\partial y^2} = \frac{\partial^2 E_y}{\partial y^2} = -\frac{q}{\varepsilon_s} N_d \qquad \text{(II.4)}$$

By solving Equation (II.4) one can evaluate the potential associated with the depletion region under the device boundary conditions as [53]

$$\Phi_b = \frac{qN_d h^2(x)}{2\varepsilon_s} \qquad \text{(II.5)}$$

When V_{gs} and V_{ds} both are non zero then d is not uniform and it is function of x and can be written by using Equation (II.2) and (II.5)

$$h(x) = \sqrt{\frac{2\varepsilon_s}{qN_d}[\Phi_b - V_{gs} + V(x)]} \qquad \text{(II.6)}$$

The depletion width W_d and W_s can be determined by letting $V(x) = V_{ds}$ at drain side and $V(x) = 0$ at source side of the device respectively. Thus,

$$W_d = \sqrt{\frac{2\varepsilon_s(\Phi_b - V_{gs} + V_{ds})}{qN_d}} \qquad \text{(II.7)}$$

and

$$W_s = \sqrt{\frac{2\varepsilon_s(\Phi_b - V_{gs})}{qN_d}} \qquad \text{(II.8)}$$

By increasing the magnitude of the applied potential, the value of $A(x)$ decreases to an extent that it effectively goes to zero. The voltage at which $A(x) = 0$ is called pinchoff voltage or threshold voltage, V_T and represented as

$$V_T = \frac{qN_d a^2}{2\varepsilon_s} - \Phi_b \qquad \text{(II.9)}$$

If x-directed mobility of the free carriers is given by $\boldsymbol{\varepsilon}$ and assuming the device width Z, then one can write the incremental channel current as

$$I_{ds}\, dx = qN_d \mu\, A(x)\, Z\, dV \qquad \text{(II.10)}$$

After integrating Equation (II.10) over the channel length we get

$$I_{ds} = I_p \left[\frac{V_{ds}}{V_T} - \frac{2}{3}\left(\frac{\Phi_b - V_{gs} + V_{ds}}{V_T} \right)^{3/2} + \frac{2}{3}\left(\frac{\Phi_b - V_{gs}}{V_T} \right)^{3/2} \right] \qquad \text{(II.11)}$$

where I_P is the saturation current given by

$$I_p = \frac{q^2 N_d{}^2 \mu Z h^3}{2\varepsilon_s L_G} \qquad \text{(II.12)}$$

When the current saturates $V_{ds} \geq V_{sat}$, and $V_{gs} \neq V_T$ its value is constant but non zero, whereas at $V_{ds} \geq V_{sat}$, and $V_{gs} = V_T$ its magnitude goes to zero.

Equation (II.11) represents the long channel model which is also known as the Shockley Model. The equation represents the linear I-V characteristics of a MESFET as shown in Figure II.4 In this region $V_{ds} << V_{gs}$, therefore by applying the Binomial approximation, Equation (II.11) reduces to

$$I_{ds} = \frac{I_p}{V_T}\left[1 - \sqrt{\left(\frac{\Phi_b - V_{gs}}{V_T}\right)}\right]V_{ds} \qquad \text{(II.13)}$$

The above expression demonstrates the linear variation of I_{ds} as a function of V_{ds}

In a long channel device, the saturation occurs when the channel pinches-off due to the applied $V_{ds,}$ and at this point the current becomes independent of V_{ds} under ideal conditions [67, 68]. Thus,

$$V_T = \Phi_b - V_{gs} + V_{ds} \qquad \text{(II.14)}$$

Substituting this condition in Equation (II.11), the corresponding I_{ds} value is

$$I_{ds(sat)} = I_p\left[\frac{1}{3} - \left(\frac{\Phi_b - V_{gs}}{V_T}\right) + \frac{2}{3}\left(\frac{\Phi_b - V_{gs}}{V_T}\right)^{3/2}\right] \qquad \text{(II.15)}$$

This represents long channel characteristics of a MESFET in the saturation region of operation. The combination of Equation (II.11) and (II.15) under the respective condition generates a family of characteristics both in the linear as well as saturation region of operation as shown in Figure II.4. This model is collectively known as long channel model.

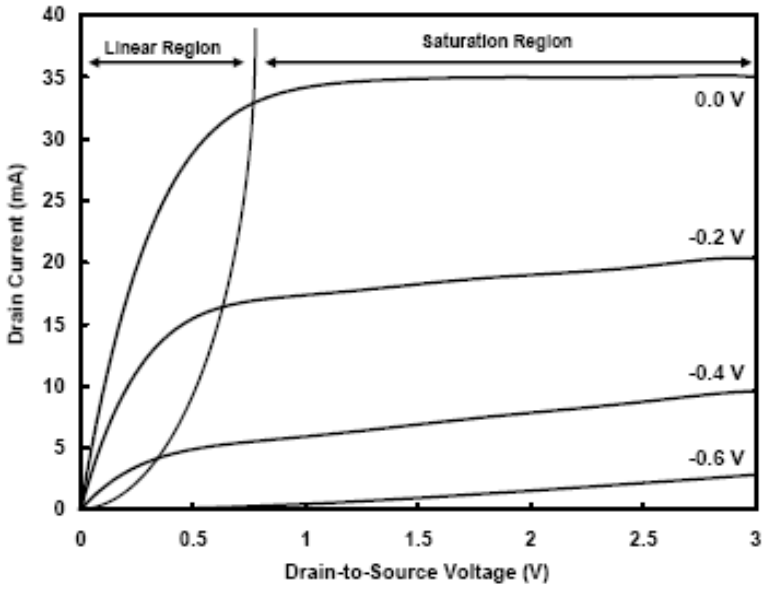


Figure II.4: Typical I-V characteristics of a GaAs MESFET showing linear and saturation regions.

Transconductance, g_m of a device after the onset of saturation is given by

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}\Big|_{V_{ds}=const} = \frac{I_p}{V_T}\left[\sqrt{\frac{\Phi_b - V_{gs}}{V_T}} - 1\right] \qquad \text{(II.16)}$$

Output conductance, $g_{d,}$ also in the saturation region is defined as

$$g_d = \frac{\partial I_{ds}}{\partial V_{ds}}\Big|_{V_{gs}=const} = \frac{I_p}{V_T} \qquad \text{(II.17)}$$

This shows that the magnitude of g_d is higher when the channel current is higher. Since a high value of g_d is an undesirable feature, the expression represents that its value could be controlled by controlling V_T of a device.

II.4.2 Short Channel Model

Devices having length $L_G < a$ are called short channel devices and the model describing the *I-V* characteristics of such devices is called short channel model [69, 50]. According to the Shockley model, the current saturation in long channel FETs occurs when the channel is pinched-off at the drain side of the gate, whereas in microwave MESFETs it is due to the velocity saturation [70]. The importance of the field dependence of electron mobility for understanding the current saturation in FETs was first mentioned by Das and Ross [71]. This concept was developed for many theoretical models which are used to describe FET's characteristics and to interpret experimental results [72, 73, 74, and 67].

As shown in Figure II.3, the width of the active channel available for the flow of current is given by

$$A(x) = a\left[1 - \sqrt{\frac{\Phi_b - V_{gs} + V(x)}{V_T}}\right] \qquad \text{(II.18)}$$

Assuming that the *x*-directed electric field, *Ex* is uniform along the channel and as V_{ds} increases from zero the value of E_x also increases until the saturation velocity electric field, E_s is obtained prior to the pinch-off. After this, the carriers will drift with saturation velocity, *vs*, and as a result I_{ds} will saturate. Thus, the saturation current for GaAs MESFETs is given by

$$I_{ds(sat)} = qN_d v_s (a-d)Z = qN_d v_s A(x)Z \qquad \text{(II.19)}$$

By combining Equations (II.18) and (II.19), we get

$$I_{ds(sat)} = qN_d v_s Za\left[1 - \sqrt{\frac{\Phi_b - V_{gs} + V(x)}{V_T}}\right] \quad \text{(II.20)}$$

where

$$V(x) \approx E_s L_G \quad \text{(II.21)}$$

A typical value of $V(x)$ where the saturation will occur is about 0.4 V [67]. Thus, indicating current saturation due to the velocity saturation mechanism in microwave FETs.

In the saturation region g_m of short channel device is, therefore, given by

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}\Big|_{V_{ds}=const} = \frac{\varepsilon_s v_s Z}{h} \quad \text{(II.22)}$$

and in saturation region g_d is also defined as

$$g_d = \frac{\partial I_{ds}}{\partial V_{ds}}\Big|_{V_{gs}=const} = -\frac{\varepsilon_s v_s Z}{h} \quad \text{(II.23)}$$

II.5 Strained III-V for p-MOSFETs

As seen in the previous chapter, III-V compounds are one of the most promising materials for future high-speed, low-power n-MOSFETs due to their high electron mobility. Recently, high performance III-V n-FETs have been demonstrated. However, for CMOS logic, there is a significant challenge of identifying high mobility III-V p-FET candidates [75–76]. Strain in silicon has been successful in significantly enhancing the p-MOS performance and is now employed ubiquitously in the industry. Use of strain to reduce hole effective masses by splitting the heavy-hole (hh) and light-hole (lh) valence bands was first demonstrated in p-channel InGaAs/ (Al)GaAs [77, 78]. More recently, the technique has been applied to strained InSb [79], GaSb [80] and InGaSb [81] based channels for improving hole mobility ($\boldsymbol{\varepsilon}_h$). Given the many choices available for materials, stoichiometry, strain, channel orientation, a modeling effort is necessary to evaluate different options and narrow down the choice for experimentation.

II.6 Challenges for III-V-based MOSFETs

Based on the comparison with mature HEMTs, it is now easy to obtain a list of essential requirements for III-V MOSFETs technology to be employed in logic (preferably CMOS) circuits. Naturally for any technology, improvement of one parameter (for example, channel mobility in a buried channel) results in degradation of

other parameters (correspondent increase of equivalent oxide thickness), therefore choice of design and technology is a subject of trade-offs and optimization.

Superior electron transport properties are a major reason why III-V materials are considered for advanced CMOS circuits. However, placing the semiconductor channel in close proximity to high-k gate oxide reduces mobility significantly in a similar way as in Si channel due to interface charges, roughness and soft phonon scattering. Reduction of these scattering mechanisms may be achieved by inserting a 3–10 nm thick wide-bandgap semiconductor barrier spacer between the channel and oxide. But this approach adds up to the equivalent oxide thickness and reinstate the scaling issues as in HEMTs. Quite obviously optimization of the spacer layer can be obtained for a particular FET design and generation.

II.7 Advanced MOSFET structures

II.7.1 Ultra Thin-Body Single Gate MOSFET

In this section we describe the UTB single gate MOSFET device structure as shown in figure II.5. The basic concept of this device is to have a thin silicon channel with an underlying, insulation oxide to eliminate leakage current paths through the substrate and to reduce parasitic capacitances to enhance the device's speed. Since most of the off - state current flows through the bottom of the body, it is desirable to replace the semiconductor substrate with an insulating dielectric. However thicker self aligned source and drain structures are required to minimize parasitic source/drain series resistance [82].

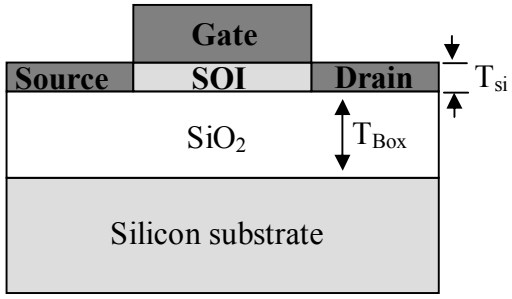


Figure II.5: Schematic diagram for UTB MOSFET [82]

II.7.2 Double gate FET / FinFET

A dual-gate device FET (DG FET) structure allows for more aggressive device scaling as short channel effects are further suppressed by doubling the effective gate

control. There have been several variations proposed for DGFET structure, but most of them suffer from process complexities, among these, the FinFET has emerged as the most practical design as shown in the figure II.6 [83]. The channel consists of a thin vertical fin around which the gate wraps on three sides. The FinFET is a double gate FET since the gate oxide is thin on the vertical sidewall but thick on the top. The fin width is an important parameter for the device as it determines the body thickness and short channel effects depend on it. For effective gate control it is required that the fin width be half the gate length or less [83].

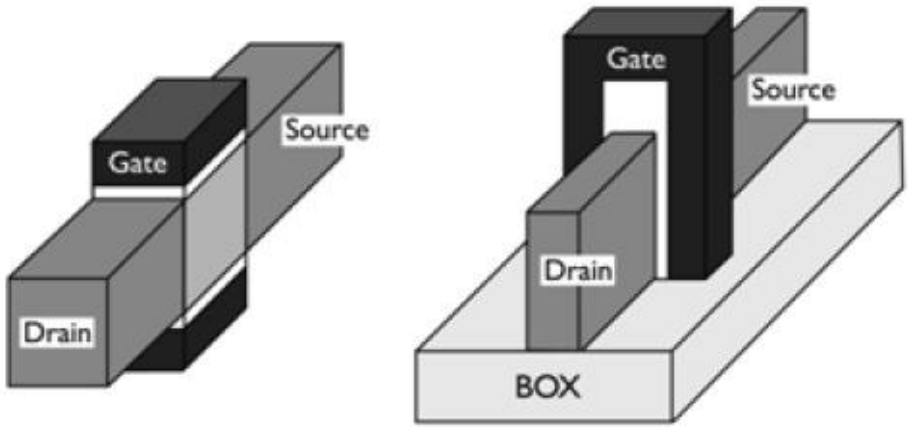


Figure II.6: Dual-Gate FET structure (left) and a FinFET structure (right)

II.7.3 Tri-gate FETs

Tri-Gate FETs [84] are currently being developed and tested by Intel. At an Intel laboratory in Oregon, Intel has been able to demonstrate promising results using Tri-Gate FETs figure II.7. An experiment was done to examine the optimum fin dimensions for a Tri-Gate FET.

Tri-Gate field-effect transistors are very similar to FinFETs in design and resemblance. However, the wires that comprise the conducting channel are significantly wider than the wires in the FinFET. Intel is currently developing integrated circuits using Tri-Gate FETs. There is also a method of construction that has been proposed known as lateral gate trenching. In this method, two lateral trenches are etched into the substrate, and are then filled with what is called lateral trench gates.

However, Tri-gate FETs are slightly more difficult to manufacture than FinFETs, as they are more reliant on dimensional parameters, Intel Corporation has successfully constructed FETs of this type, and it is likely we will see devices that utilize this design in the next decade.

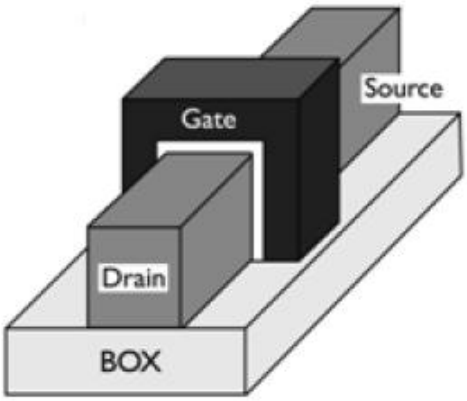


Figure II.7: Tri-Gate FET structure [84]

II.7.4 Gate-All-Around FETs

A gate-all-around (GAA) transistor is a silicon-on-insulator (SOI) double-gate transistor consisting of a bridge between the source and drain that is completely surrounded by the gate figure II.8 [85]. It is akin to three MOS transistors working in parallel, with one at the front, the back, and on the two edges of the silicon bridge. The GAA transistor is very similar to the FinFET design, but differs in that it completely surrounds the active area, or channel, with the gate oxide and metal electrode [86]. This provides it with excellent durability and analog behavior in high-temperature environments. One of the uses of this increased endurance for high temperature is the ability to pack more transistors per unit volume. The limitation of single gate field effect transistors in this aspect was apparent, for as the concentration of transistors increased so did the temperature, degrading their performance. With the GAA design it would be possible to manufacture ever smaller transistors that could fit into the same space as its predecessors whilst keeping the conductance undiminished, increasing the power output [87].

The GAA, like all multi-gate transistors, is designed with rather thin active area [88]. Thus, using the accustomed polysilicon gates would require extremely high doping levels in order to achieve the appropriate threshold voltages. This means that the transistors will have to be fitted with metal gates (Ni, for example), allowing them to benefit from the enhanced properties of low-doped channels while retaining a low threshold voltage.

The difficulty arises from the complex fabrication process of gate-all-around transistors, as both gates have to be aligned for functionality [88]. With lithography it is possible to precisely align gates to within a few nm. However, as transistors become

ever smaller and dive into the sub 10 nm ranges, a few nm of error will become more and more of a problem. A proposed solution for this is a self-aligned gate, made by epitaxial growth of SiGe and Si layers, which are then funneled and filled with gate material [89]. This manufacturing approach, based on the silicon-on-nothing process, coupled with the need for metal reinforced gates, is not ideal, but is capable of producing transistors with extremely small gate lengths. Gate-All-Around FETs are the most difficult of the three device designs that we have discussed [87].

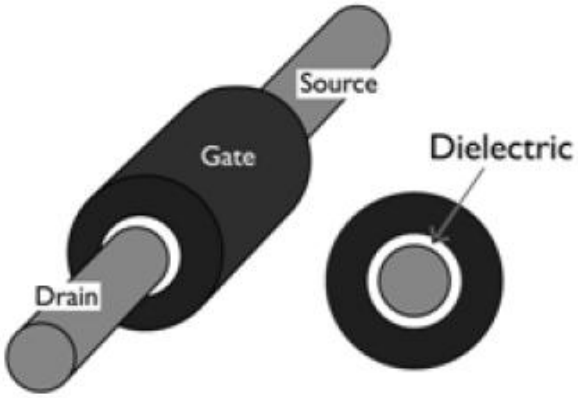


Figure II.8: Gate-All-Around FET structure

II.8 Problems solved by multi-gates FETs

Multi-gate FETs can potentially solve many of the problems with scaling down the size of transistors. These include the increased threshold leakage that comes with shorter channel length, the electron tunneling due to thinner layers of the insulating barriers, and the corner effects produced by smaller sized transistors.

The two problems that immediately impede progressively scaling down transistors are DIBL and unacceptable levels of heat dissipation. Multi-gate FETs attempt to remedy both of these problems. The main culprit behind both of these issues is off-state leakage. Multi-gate FETs directly increase the electrostatic control over the channel, simultaneously remedying both of these issues. While better electrostatic control allows for shorter channel length, it also improves the amount of heat generated by inherently reducing off-state leakage.

Secondary effects of these solutions are also present. Not only does better electrostatic control lead to less heat generation, it also equates to less power consumption. A significant portion of power consumed by computer processors is a direct result of off-state leakage. Aside from running more efficiently, the obvious

advantage to using less power is less heat production. Obviously, as less current is going through the device, less heat will be produced.

II.9 Limitations of multi-gates FETs

After examining current field-effect transistors, the inherent problems of their design are made clear. Multi-gate FETs are capable of solving nearly all of the immediate problems with scaling FETs down. However, the problem lies in the difficulty of manufacturing these devices. Advancements in nanolithography are necessary before FETs can reach sizes smaller than 10 nm.

Beyond the 10 nm range, it may not be possible to scale transistors much smaller. The quantum effects of the materials become too prevalent and lead to unpredictable behavior. It may be impossible to retain enough electrostatic control over the channel in order to distinguish between the on and off state.

II.10 Conclusion

Transistors utilizing III-V channel materials can offer high performance in terms of high speed of the circuits and low power. However, to take full advantage of high mobility/wide bandgap channel materials, novel device structures, such as DG or GAA FETs along with strain engineering will be needed, in order to achieve high drive currents while maintaining low off-state leakage. For III-V materials to become mainstream, important challenges, such as low parasitic resistance/capacitance, and heterogeneous integration on Si platform must be overcome.

Multi-gate-based design can collaborate to enable an enhanced scaling, performance, functionality, and flexibility. Since the device operation is governed by 3-D effects, there are complex coupling mechanisms along the longitudinal, lateral and vertical directions. A given size effect (length, width, or thickness) is modulated by the other dimensions. All device architectures (planar or vertical double gates, Ω or π topologies, 4-gates and gate-all-around transistors) have their merits and drawbacks. The winners will be selected with processing feasibility criteria.

Chapter 2 began with a critical overview of III-V-based FETs and mathematical description of *I-V* characteristics of both long channel and short channel devices. Also the concept of multi-gate technologies, problems solved by them and their limitations has been introduced. We discussed the successful development of multi-gate devices that can be used to further scale CMOS digital technology. These devices can provide

new and better characteristics across all logic, memory and analog device function. The challenges in making these devices to enter mainstream products are many. However, rapid strides in process, design and modeling in the last few years has delivered substantial progress. This research will investigate the multi gate structures to propose and model a new optimized design for GaN-FET-based circuit for future power switching and digital gate devices, which will be discussed in the remain of this thesis.

Chapter III
Evolutionary-computation techniques

III.1 Introduction

Throughout history, Nature has been a major source of inspiration and metaphors for scientific and technical development, which, in turn, has contributed to the better understanding of Nature itself. It is not difficult to identify the links between the ear and the microphone, the eye and the camera, the bat and the sonar system, the brain and artificial neural networks, and so forth. Similarly, the process of natural evolution has inspired a growing amount of research in artificial systems, which has been made possible by the increasing availability of modern computing power.

This Chapter seeks to draw attention to the potential of artificial evolution techniques in control engineering. It begins with a brief description of evolutionary computation as a whole in section III.2. It describes the proprieties of evolutionary algorithms, their uses and limitations. Section III.2.3 presents different evolutionary techniques, after which a particular family of methods, known as genetic algorithms, is introduced and discussed in more detail. The motivations for the work on multiobjective optimization which will follow are also identified.

III.2 Evolutionary computation

The term Evolutionary Computation (EC) is used to describe a broad class of computational methods inspired in the process of natural evolution. The interest such methods have attracted from research fields as diverse as biology, chemistry, economics, engineering, cognitive science and mathematics, among others, is twofold. Firstly, EC provides a means of modelling and simulating natural and economic processes, through which the original processes can be studied and/or analyzed. In addition to that, EC has also proved useful in addressing complex search and optimization problems effectively; extending the scope of optimization to areas it could not reach before [90].

Evolutionary computation methods, or Evolutionary Algorithms (EAs), emerged in the late 1960s. EAs mostly involve metaheuristic optimization algorithms such as genetic algorithms (GA) [91, 92], evolutionary programming (EP) [93], evolution strategys (ES) [94, 95], genetic programming (GP) [96, 97], learning classifier systems

(LCS) [98] and swarm intelligence (comprising ant colony optimization (ACO) [99] and particle swarm optimization (PSO) [100, 101]). Among them, genetic algorithms are perhaps the most widely known type of evolutionary algorithms used today.

III.2.1 Properties of Evolutionary Algorithms

Evolutionary Algorithms come in many different varieties, but in order to be classified as an EA, an algorithm must have certain basic properties. There are three integral properties shared amongst all EAs [102]:

1. Population: "Evolutionary algorithms utilize the collective learning process of a population of individuals." The population is essentially a group of possible solutions generated by the algorithm - all of which are evaluated and then the best are chosen.
2. Reproduction and Mutation: "Descendants of individuals are generated by randomized process intended to model *mutation* and *recombination*." Mutation happens when an individual erroneously self-replicates; this is done purposely and is important for ensuring diversity of individuals amongst a population. Recombination is the reproduction step, two or more individuals are combined in order to distribute their individual information. The recombination step is usually how new individuals are introduced into the population.
3. Evaluation: "By means of evaluating individuals in their environment, a measure of quality or fitness value can be assigned to individuals." This measurement is usually done by a fitness function; from an evolutionary standpoint, this represents the environment. A fitness function is the part of the algorithm that drives the algorithm. Without a form of evaluation, the differences between individuals would be indistinguishable.

The process for Evolutionary algorithms is diagrammed below. The population is initialized, mutation occurs (most likely not in the first iteration), each individual in the population's fitness is evaluated, then crossover and repeat the cycle until stopping conditions are met. The cycle of steps is simplistic, however it is not trivial.

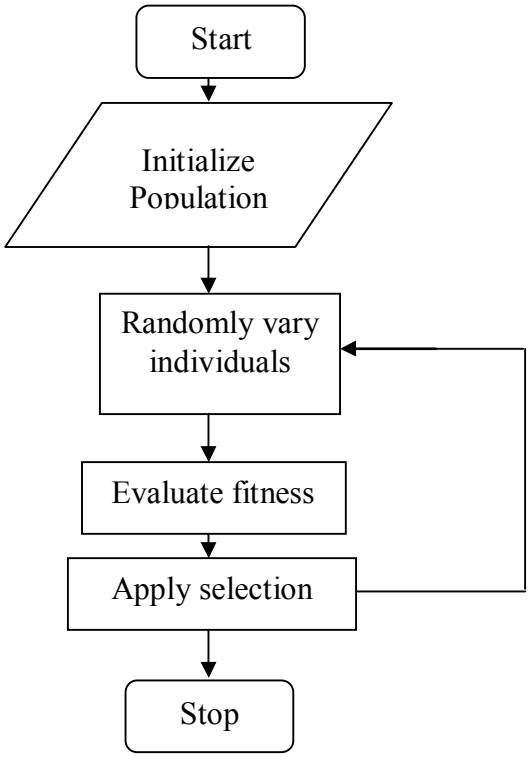


Figure III.1: Evolutionary Algorithm Flowchart [103]

III.2.2 Evolutionary Algorithm Uses and Limitations

There are many questions a developer should ask when implementing an EA; for instance: how should one represent the individuals of the population? What should the population size be? How should the population be updated after selection is applied? How should mutation affect an individual? When should the algorithm stop? The answers to these questions are different for certain type of EAs, and are also dependent on the type of problem being solved.

Before addressing the above questions concerning implementation details of EAs, there is a simpler question that needs to be answered: Why Evolutionary Algorithms? EAs are essentially a form of search. So, what sets it apart from other approaches when considering how to solve a problem? Some advantages include: "simplicity of approach, its robust response to changing circumstances, and its flexibility."[103] Holland argued that the power of EAs (more specifically GAs) comes from their ability to solve problems in an "implicitly parallel fashion."[104] Part of the flexibility of EAs is the wide variety of problems that can be solved. If a problem can be formulated as a functional optimization problem, then it can be solved by EAs. In addition, EAs have the ability to solve problems that have not been solved. "Fogel (1995) declared artificial intelligence as 'They solve problems, but they do not solve the problem of how to solve

problems.' In contrast, evolutionary computation provides a method for solving the problem of how to solve problems."[103]

EAs are not the answer to every problem, because they have some problems of their own. Some optimization problems lead EAs to false solutions, when the algorithm finds a locally optimal solution that meets the stopping criteria. Locally optimal solutions represent roots (local maximum or minimum points in the search space), and to an EA, "one root is as good as another."[105] Highly nonlinear functions are also difficult for EAs to optimize, partly due to a greater occurrence of locally optimal solutions. "Typical approaches to highly nonlinear problems involve either linearizing the problem in a very confined region or restricting the optimization to a small region. In short, we cheat."[105] Another limiting factor of EAs is the representation of an individual's genome. For example, if it is chosen to be a fixed length, then that is a limiting factor for the solution, if the optimum solution does not fall within the representation's range of solutions, then the optimal solution will not be found. Another disadvantage of EAs is setting one up to solve a problem. A great amount of understanding of a problem is required to know how to represent a solution, tests its fitness and have an effective termination condition [106].

III.2.3 Evolutionary techniques

- Evolutionary Programming

Evolutionary programming (EP), developed by Fogel et al. [93], traditionally has used representations that are tailored to the problem domain. For example, in real-valued optimization problems, the individuals within the population are real-valued vectors. Similarly, ordered lists are used for traveling salesman problems, and graphs for applications with finite-state machines. EP is often used as an optimizer, although it arose from the desire to generate machine intelligence.

After initialization, all P individuals are selected to be parents, and then are mutated, producing P children. These children are evaluated and P survivors are chosen from the $2P$ individuals, using a probabilistic tournament selection. The best individual always survives, ensuring that once an optimum is found it cannot be lost. This is referred to as "elitism." The form of mutation is based on the representation used, and is often adaptive. For example, when using a real-valued vector, each variable within an individual may have an adaptive mutation rate that is normally distributed with a zero

expectation. Recombination is not generally performed since the forms of mutation used are quite flexible and can produce perturbations similar to recombination, if desired.

The theoretical foundations for this algorithm stem from a proof of the global convergence (with probability 1) for EP [107]. This result is derived by defining a Markov chain over the discrete state space that is obtained using the numbers represented on a digital computer. By combining all possible populations that contain the grid point having fitness closest to the true global optimum, an absorbing state is defined in which the process will ultimately be trapped, due to elitism.

- Evolution Strategies

Evolution strategies (ESs) were developed by Rechenberg (1973) [94], using selection, mutation, and a population of size one. Schwefel [108] introduced recombination and populations with more than one individual, and provided a nice comparison of ESs with more traditional optimization techniques. Due to initial interest in hydrodynamic optimization problems, evolution strategies typically use real-valued, vector representations.

After initialization and evaluation, individuals are selected uniformly randomly to be parents. In the standard recombinative ES, pairs of parents produce children via recombination, and the children are further perturbed via mutation. The number of children created is greater than the number of parents *P*. Survival is deterministic and is implemented in one of two methods. The first method allows the *P* best children to survive, and replaces the parents with these children. This is referred to as *(P, ∂)* survival, where *P* corresponds to the population size and A refers to the number of children created. The second method is referred to as *(P + ∂)* survival, which allows the *P* best children and parents to survive. The *(P + ∂)* method is elitist, while the *(P, ∂)* method is not. Like EP, considerable effort has focused on adapting mutation as the algorithm runs by allowing each variable within an individual to have an adaptive mutation rate that is normally distributed with a zero expectation. Unlike EP, however, recombination does play an important role in evolution strategies, especially in adapting mutation.

Most of the theory for ESs is concerned with convergence velocity, i.e., trying to maximize the rate at which the ES converges to the optimum.

- Genetic Programming

Genetic Programming (GP) is a related technique popularized by John Koza [96] in which computer programs, rather than function parameters, are optimized. Genetic programming often uses tree-based internal data structures to represent the computer programs for adaptation instead of the list structures typical of genetic algorithms.

- Particle swarm optimization

Particle swarm optimization (PSO) [100] is a popular problem solving technique in the swarm intelligence paradigm. It was first introduced by Kennedy and Eberhart in 1995. They developed simple methods which could efficiently optimize continuous nonlinear mathematical functions. Borrowing ideas from artificial life, social psychology and swarming theory [100, 101], PSO simulates swarms such as flocks of birds and schools of fish searching for food.

Also, PSO is related to evolutionary computation (EC), but it is somewhat different [109, 100]. Similar to many EC techniques, PSO initializes a problem state to a population of randomly distributed solutions. Unlike many other ECs however, PSO "evolves" solutions based on individual experience and group experience, rather than using evolutionary operators (e.g. the crossover and the mutation operators in genetic algorithms). It assumes that socially shared information helps its population evolve. In other words, the population iteratively updates and searches for optima with the shared information.

- Ant colony optimization

Marco Dorigo invented ant colony optimization (ACO) by modeling insect ants' behavior to solve discrete optimization problems, such as the traveling salesman problem [110]. Artificial ants have been tested on other combinatorial problems such as quadratic assignment problems, graph coloring, job-shop scheduling, sequential ordering, network routing, swarm based robotic problems [111, 112] and constraint satisfaction problems [113]. The idea is that a colony of ants collaboratively finds shortest paths between their nest and a food source without a coordinator or leadership [112]. These ants "communicate" through a chemical substance called *pheromone*. In ACO, this pheromone represents the information shared among the fellow ants. Essentially, each individual ant leaves pheromone on the way it goes by ant picks up pheromone left by the other ants. Because this substance gets weaker over a distance

and gradually evaporates over time, the amount of pheromone implies how frequently and recently ants have been through the same path. Stronger pheromone may indicate that a path is shorter or the chances of being successful are higher.

In the algorithm, ants randomly wander the search space at first. Once pheromone accumulates on several trails, individual ants detect it and choose a path among the candidate trails. This decision making will be favorable to those with stronger pheromone deposit. Eventually, these ants will converge to an optimized path and find a solution.

III.3 Genetic algorithms

Genetic algorithms (GAs), developed by Holland [114], have traditionally used a more domain-independent representation, namely, binary strings. However, many recent applications of GAs have focused on other representations, such as graphs (neural networks), Lisp expressions, ordered lists, and real-valued vectors.

Genetic algorithms are stochastic search algorithms inspired by the principles of natural selection and natural genetics. A population of candidate solutions, or individuals, is maintained, and individuals made to compete with each other for survival. Once evaluated, stronger individuals are given a greater chance of contributing to the production of new individuals (the offspring) than weaker ones, which may not even contribute at all. Offspring are produced through *recombination*, whereby they inherit features from each of the parents, and through *mutation*, which can confer some truly innovative features as well. In the next selection step, offspring are made to compete with each other, and possibly also with their parents. Improvement in the population arises as a consequence of the repeated selection of the best parents, which are in turn more likely to produce good offspring, and the consequent elimination of low-performers [90].

III.3.1 How Genetic Algorithms are Different from Traditional Methods?

Genetic algorithms are different from more normal optimization and search procedures, like direct and indirect calculus-based methods, enumerative schemes, random search algorithms etc, in four ways [115]:

A. It works on coding of the parameter set, not the parameters themselves.
B. It searches from a population of points, not a single point.

C. It uses objective function information, not the derivative or other auxiliary knowledge.
D. It uses probabilistic transition rules, not deterministic rules.

Genetic algorithms require the natural parameter set of the optimization problem to be coded as a finite-length string over some finite alphabet. In many optimization methods, we move gingerly from a single point in the decision space to the next using some transitional rule to determine the next point. The point-to-point method is dangerous because it is perfect prescription for locating false peak in multi-modal search spaces. By contrast, genetic algorithm works from a rich database of points simultaneously, climbing many peaks in parallel; thus, probability of finding a false peak is reduced over that go point-to-point.

Many search techniques require much auxiliary information in order to work properly. In contrast, genetic algorithm requires only objective function values associated with individual string. Unlike other methods, genetic algorithms use random choice as a tool to guide a search toward regions of the search space with likely improvement. These four differences contribute towards genetic algorithm's robustness and resulting advantage over other more commonly used techniques.

III.3.2 How Genetic Algorithms Work?

Genetic algorithms are implemented as a computer simulation in which a population of abstract representations (called chromosomes or the genotype or the genome) of candidate solutions (called individuals, creatures, or phenotypes) to an optimization problem evolves toward better solutions. Traditionally, solutions are represented in binary as strings of 0s and 1s, but other encoding are also possible. The evolution usually starts from a population of randomly generated individuals and happens in generations. In each generation, the fitness of every individual in the population is evaluated, multiple individuals are stochastically selected from the current population (based on their fitness), and modified (recombined and possibly randomly mutated) to form a new population. The new population is then used in the next iteration of the algorithm. Commonly, the algorithm terminates when either a maximum number of generations has been produced, or a satisfactory fitness level has been reached for the population. If the algorithm has terminated due to a maximum number

of generations, a satisfactory solution may or may not have been reached. A typical genetic algorithm requires two things to be defined:

- a genetic representation of the solution domain.
- a fitness function to evaluate the solution domain.

A standard representation of the solution is as an array of bits. Arrays of other types and structures can be used in essentially the same way. The main property that makes these genetic representations convenient is that their parts are easily aligned due to their fixed size that facilitates simple crossover operation. Variable length representations may also be used, but crossover implementation is more complex in this case.

The fitness function is defined over the genetic representation and measures the quality of the represented solution. The fitness function is always problem dependent. For instance, in the knapsack problem we want to maximize the total value of objects that we can put in a knapsack of some fixed capacity. A representation of a solution might be an array of bits, where each bit represents a different object, and the value of the bit (0 or 1) represents whether or not the object is in the knapsack. Not every such representation is valid, as the size of objects may exceed the capacity of the knapsack. The fitness of the solution is the sum of values of all objects in the knapsack if the representation is valid or 0 otherwise. In some problems, it is hard or even impossible to define the fitness expression; in these cases, interactive genetic algorithms are used.

Once we have the genetic representation and the fitness function defined, GA proceeds to initialize a population of solutions randomly, and then improve it through repetitive application of mutation, crossover and selection operators.

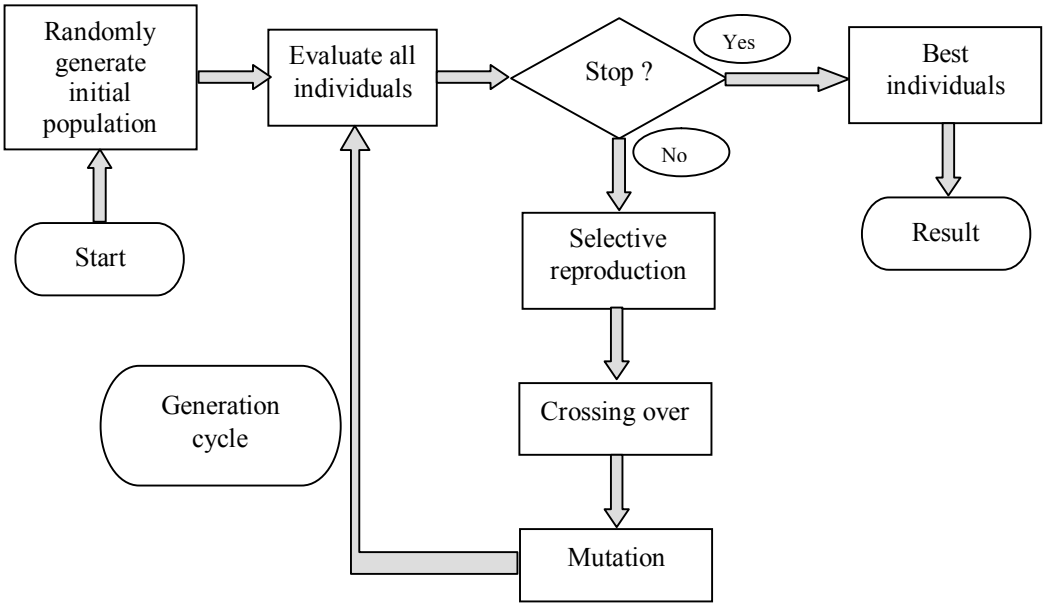


Figure III.2: Flow Diagram of Genetic Algorithm [116]

III.3.3 Basic steps of genetic algorithms

- Initialization of the population

A set of candidate solutions are called population. At the beginning of the algorithm, to initialize the population, a predefined number of solutions are generated randomly.

- Selection

After the initial population is constructed, it is time to the process of choosing parents (chromosomes) for breeding, namely selection of parents. In genetic algorithm, selection is designed to use fitness function as a discriminator of the quality of solutions represented by the chromosomes in a population. Those with higher fitness value have a greater chance of being selected than those with lower fitness value.

There are various selection methods in genetic algorithm. The standard selection method used is Roulette Wheel or in other words, Fitness Proportional selection. In this kind of selection method, expected number of times that a chromosome will be selected for breeding is calculated as chromosome's fitness divided by the average fitness of the population. To implement this method, each chromosome is placed as a slice of a circular roulette wheel, the size of the slice is proportional to the chromosome's fitness. If there are *N* chromosomes in the population, the wheel is rotated *N* times. On each

rotation, the chromosome shown by the wheel's marker is selected to be in the pool of parents for the next generation. So the selection is end up with *N* chromosomes, keeping initial number of chromosomes in the population. Higher fitness value of chromosome implies the larger slice on the roulette wheel, therefore the probability of being selected is higher. Note that one chromosome can be chosen more than once.

Tournament Selection is another method for deciding which chromosome will be chosen. In this method, two chromosomes are chosen randomly in the population and then the one with the highest fitness between these two is selected as the parent. The two chromosomes are the return the original population and can be selected again.

- Recombination

After selection, chosen chromosomes are recombined to create new members of next generation. New members are expected to be better than their predecessors since selection for recombination gives more chance to the ones with higher fitness to be chosen. There are two main recombination operators in genetic algorithm: crossover and mutation.

- Crossover

The idea of the crossover operation is mixing genetic material from two selected parent chromosomes to produce child chromosomes. If chromosomes are represented in bit-strings, this is done as follows. First of all a crossover probability is defined. A random number in the interval [0, 1] is generated and compared with the crossover probability. If the crossover probability is greater than or equal to the random number then the crossover operator is applied. If the random number is greater than the crossover probability then crossover operator is not applied. Therefore both parents remain unchanged, so the children chromosomes are exact copies of their parents. The value of the crossover probability has great importance here [92].

There are many methods used in designing crossover operator in literature. Although they can be changed by problem type, the most common used crossover operators are as follows:

- ***N*-point Crossover**: One-point and two-point crossovers are the simplest and widely used crossover methods. In one-point crossover, a number less than the length of chromosome is selected randomly and represents crossover point. Then, the genetic material before the crossover point remains unchanged while the genetic material after

the crossover point is exchanged between the parents. The idea of one-point crossover can be generalized to *N*-point crossover by using *N* crossover points rather than just one. For instance, in two-point crossover, two crossover points are selected randomly and the genetic material between crossover points is swapped. An example of two-point crossover method is given in Figure III.3.

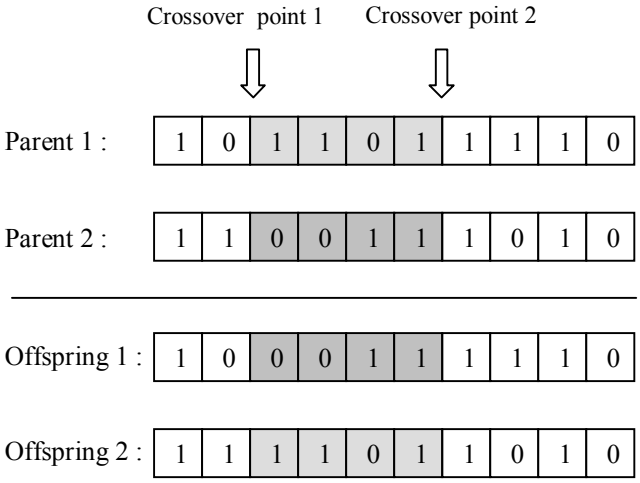


Figure III.3: Two-point Crossover

- Uniform Crossover: In uniform crossover each allele has the chance of exchanging with the gene of the other parent with the probability of predefined *swapping probability.* Most of the time 0.5 is taken as swapping probability value.

- Mutation

In genetic algorithms, most chromosomes in the population seem like each other after a number of generations. What this means is that, no crucial changes in the population, therefore in the search space do not occur. To overcome this problem and add diversity to the population mutation operator is used. Mutation operator has the effect of creating a new chromosome which cannot be created by the ordinary crossover operator.

After crossover is applied and the offsprings are formed, they have a chance of being mutated. Mutation operators changes one or more gene values in a single chromosome. For the chromosomes represented in binary strings, the mutation operator works as follows. A number in the interval [0, 1] is generated randomly and compared to a predetermined mutation rate. Mutation rates used in literature are usually very small

(e.g. 0.001). If the random number is greater than the mutation rate, mutation is not applied. If the mutation rate is greater than or equal to the random number, then the gene value is changed artificially from 0 to 1 or 1 to 0. (See Figure III.4)

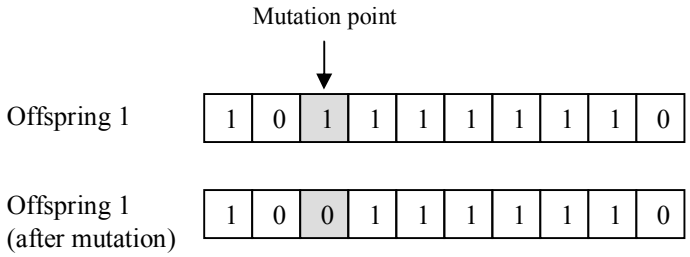


Figure III.4: Mutation Operator

- Replacement

After the new offsprings are created with crossover and mutation operators, it is time to form up the successor generation. Recall that parent chromosomes were selected according to their fitness, so it is expected that the offsprings increase the fitness of the population generation by generation. Through replacement, genetic algorithm decides whether offspring will survive or will become exist. Some of the most common replacement techniques are explained below.

- Complete Replacement

This technique deletes all the members of the predecessor population and replaces them with the same number of new chromosomes that have just been created.

- Steady-state

In this technique, n old members are chosen in the population and replaced with "n" new members. The choice of the number "n" and the decision of which members to delete from the current population are important aspects of genetic algorithm.

- Replacement with elitism

This technique is same as complete replacement except that this time one or two chromosomes with the highest fitness are chosen to next generation. By this way, good solutions are preventing from become extinct.

III.4 Multi-objective optimization

Optimization problems are usually posed as single objective optimization problems: A single function *f* is to be minimized or maximized. Naturally occurring optimization problems often consist of several aspects that are to be optimized simultaneously. It is possible to perform optimization on these multi-objective optimization problems (MOOP) without reducing them to a single objective problem.

Multi-objective problems are problems with two or more, usually conflicting, objectives.

The main difference from single-objective optimization is that a multi-objective problem does not have one single optimal solution, but instead has a set of optimal solutions, where each represents a trade-off between objectives.

A way to avoid the complexities of multi-objective optimization is to convert the multi-objective problem into a single-objective problem by assigning weights to the different objectives, calculating a single fitness value. The major problem with this weighted sum approach is that it is *subjective*, as it ultimately leaves it to a *decision maker* (DM) to assign weights according to the subjective importance of the corresponding objectives. The approach further assumes that the DM has a *priori* knowledge of the importance of the different objectives, which is often hard or impossible to come by. The *objective* approach uses *Pareto compliant* ranking of solutions, as explained in the following section. This approach favours solutions which are better in a true, multi-objective sense.

III.4.1 Main concepts of multi-objective optimization

The primary concept of multi-objective optimization, is the multi-objective problem having several functions to be optimized (maximized or minimized) by the solution x, along with different constraints to satisfy, as seen in Equation 1.

$$\begin{aligned} \min imize / \max imize \quad & f_m(x), && m = 1,2,.....M; \\ subject\ to \quad & g_j(x) \geq 0, && j = 1,2,.....J; \\ & h_k(x) = 0, && k = 1,2,.....K; \\ & x_i^L \leq x_i \leq x_i^U, && i = 1,2,.....N; \end{aligned} \tag{1}$$

x is a vector of decision variables: $x_i = (x_1, x_2, ...x_N)^T$ where each decision variable $x_i \in \Re$ is bounded by the lower bound x_i^L and the upper bound x_i^U. These bounds

constitute the decision variable space or simply the decision space *D*, and the *M* objective functions $f_m(x)$ define a mapping from *D* to the objective space *Z*. The subjective mapping is between the n-dimensional solution vectors $x \in D$ and the m-dimensional objective vectors $f_m(x) \in Z$, such that each $x \in D$ corresponds to one point $y \in Z$, as illustrated in figure III.5.

The problem may be constrained, so Equation 1 also shows *J* inequality and *K* equality constraints. Solutions satisfying these constraints are feasible, and belong to the feasible part of the decision space; $S_D \subset D$ which the constraint functions map to the feasible part of objective space $S_Z \subset Z$.

The transition from single-objective to multi-objective optimization problems introduces a challenge in comparison of solutions, since performance is then a vector of objective values instead of a single scalar. The concept of *Pareto dominance* addresses this issue, enabling comparison of solutions. We say that a solution *x dominates* solution *y*, written $x \prec y$, if and only if the following two conditions hold: 1) The solution *x* is no worse than solution *y* in all objectives. 2) The solution *x* is better than *y* on at least one objective. Formally, assuming minimization on all objectives:

$$f_m(x) \leq f_m(y) \forall \wedge \exists i : f_i(x) < f_i(y) \qquad (2)$$

From the definition of dominance, several other important definitions can be derived. When optimizing, we are interested in locating the *non-dominated set* of solutions. Among a set of solutions *P*, the non-dominated set of solutions *P'* are those that are not dominated by any other member of the set *P*.

Correspondingly, we define the *globally Pareto-optimal* set as the non-dominated set of the entire feasible search space $S \in D$. This is also referred to simply as the Pareto-optimal set, and our goal using multi-objective optimizers is to approximate this set. In objective space, the mapping from the Pareto-optimal set is denoted the *true Pareto-optimal front* or simply the true Pareto front [117].

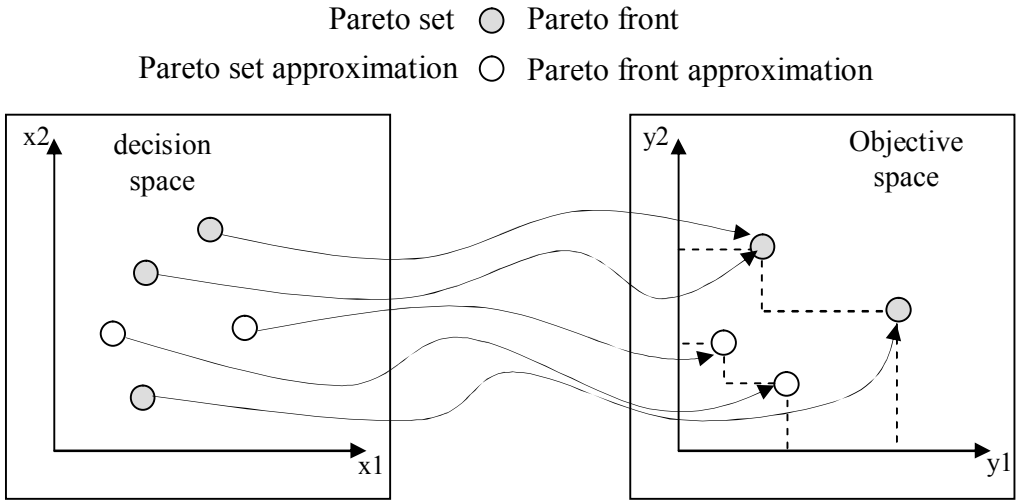


Figure III.5: Mapping from decision space to objective space - assuming maximization

III.4.2 Multi-objective optimization using evolutionary algorithms

One way to perform multi-objective optimization is by using an evolutionary algorithm (EA). Evolutionary algorithms are optimizers inspired by Darwenian evolution and with this the concept of survival of the fittest. In an EA, solutions to a given problem are considered individuals of a population, where the fitness of individuals is given by how good they solve the problem at hand. In the population individuals may mate to create offspring, which makes parents and offspring compete for inclusion in the next generation. As only the most fit will survive this fight, the full population is improving iteratively in each passing generation [118].

More formally, the strength of EAs comes from their use of a set of solutions, not only improving on a single solution. This makes it possible to combine several (good) solutions, when creating a new one. An EA is actually a stochastic metaheuristic, i.e. a general optimization method, basing itself on probabilistic operators. Thus, contrary to deterministic algorithms, EAs may produce different results from different runs.

The greatest difference between single-objective EAs and multi-objective EAs (MOEAs), is that for single-objective optimization, it is simple to return the most optimal solution in a population, as scalar based evaluation automatically implies a total order on solutions. For MOEAs, the situation is very different. Due to the higher dimensionality of the objective space, all resulting individuals of the population may be incomparable to each other, each representing an optimal trade-off between objectives. That is, the result of running a MOEA is typically a set of non-dominated solutions.

From this result set, it is up to the decision maker to find out which solution(s) to realise. The full process is illustrated in figure III.6 [118].

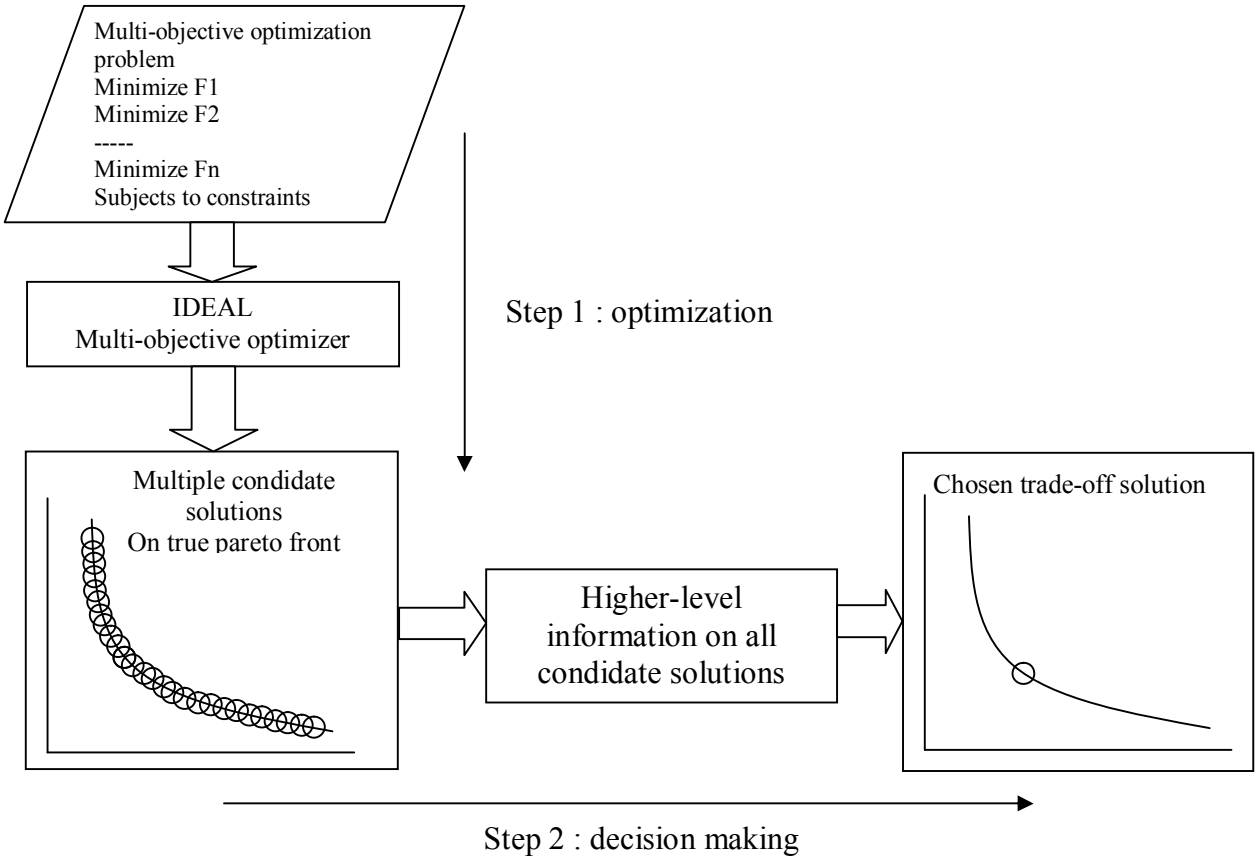


Figure III.6: Multi-objective optimization process

III.4.3 Goals of multi-objective evolutionary algorithms

As stated above, the goal of a multi-objective evolutionary algorithm is to approximate the Pareto-optimal set of solutions. However, this goal is often subdivided into the following three goals for the resulting population of a MOEA:

1. **Closeness** towards the true Pareto-front
2. An even **distribution** among solutions
3. A high **spread** of solutions

First, we want all of our solutions to be as optimal as possible by making them get as close to the true Pareto front as possible, where closeness is measured as Euclidian distance in objective space. MOEAs select the most dominating (or most non-dominated) individuals for survival to drive the population towards the true Pareto front, since these must be closest to it. Optimally, all returned solutions from a MOEA lie on the true Pareto front.

The second goal of MOEAs is to cover as much of the Pareto front as possible, and this goal is very specific to multi-objective optimization. Having an even distribution of solutions on the Pareto front ensures a diverse set of trade-offs between objectives. Having a set of solutions all equidistant to their nearest neighbour provides the decision maker with an overview of the Pareto front, while also making the final selection possible, based on the range of trade-offs between objectives represented by the population

The third goal is very connected to the second. Having a high spread means to have a high distance between the extreme solutions in objective space, and as before, this is to ensure coverage of the Pareto front. Ensuring population diversity is most often done by applying a density or crowding measure which penalise individuals that are close to each other in objective space. Such measure also ensures a high spread, since it will force the full population to spread as far as possible.

From an application point of view, the first goal is by far the most important, since it directly determines how optimal the returned solutions are. The second goal is important, but not crucial, since most often only a few solutions from the final population will be chosen for further investigation. Finally, the third goal is practically irrelevant, since extreme solutions are rarely, if ever, implemented in reality.

To pursue the three goals, traditional MOEAs employ two mechanisms directly meant to promote Pareto-front convergence and a good solution distribution. The first mechanism is elitism, which ensures that solutions closest to the true Pareto front will never be eliminated from the population under evolution, i.e. the number of non-dominated solutions in the population can only increase. The second is a measure of crowding or density among solutions, a secondary fitness which is often incorporated into the Pareto-rank to form a single, final fitness [117].

III.5 Conclusion

The evolutionary approach of artificial intelligence is based on the computation models of natural selection and genetic known as evolutionary computation. Evolutionary computation combines genetic algorithms, evolution strategies and genetic programming.

Genetic algorithms are a very powerful tool. However, coding the problem as a bit string may change the nature of the problem being investigated. There is always a danger that the coded representation represents a problem that is different from the one

the researcher wants to solve. The need to solve optimization problems arises in almost every field and in particular, is a dominant theme in the engineering world. Many optimization problems from the engineering world are very complex in nature and quite difficult to solve by conventional optimization techniques. Genetic algorithms have received considerable attention for complex problems and have been applied successfully in the area of industrial engineering.

This chapter is an attempt to identify common concepts and general building blocks used in evolutionary multi-objective optimization. All of these techniques have advantages and disadvantages, and therefore the selection of the techniques integrated in an MOEA strongly depends on the problem to be solved. Despite the variety of available methods, the field of multi-objective evolutionary computation is still quite young and there are many open research problems. Therefore, this research will investigate the MOEA to solve several engineering problems and especially the use of multi-objective genetic algorithm techniques for solving and finding the optimized design of the III-V-based FETs in order to improve the device electrical behavior for both analog and digital circuit applications, which is the aim of the later chapters.

Chapter IV

Multi-gate-based design to improve the scaling capability of GaN-FETs

IV.1 Introduction

In high-tech digital circuitry, the submicron GaN-MESFETs are widely used because of their superior noise immunity, enhanced radiation hardness, immunity to hot carrier degradation, high thermal conductivity, simplicity of fabrication and less mobility degradation [10,13,119,120]. Although GaN-MESFETs have good performance for high power circuit applications, potential ways to improve them for high speed digital circuit and low leakage current applications is still worth investigating. Several GaN-MESFET structures have been reported to have reached this goal and optimized over the last few years [12, 13,120,121]. A direct way to improve the high frequency and scaling capabilities of the GaN-MESFET is the reduction of its gate length [122]. However, with the reduction in channel length, control of short-channel effects (SCEs) and drain current in subthreshold regime is one of the biggest challenges in further downscaling of the technology [123,124].

The presence of short-channel effects makes the device operating in subthreshold domain more difficult and challenging. To minimize short-channel-effects and improve subthreshold electrical behaviors, a new design and improvement of conventional GaN-MESFETs become important. In this chapter, new designs of GaN-MESFET called Double Gate (DG) GaN-MESFET and Gate All Around (GAA) GaN-MESFET and their 2-D analytical and numerical analysis, respectively, are proposed in order to improve the SCEs for future power switching and digital gate devices.

This chapter is organized in tow parts. In the first part, we describe a new deep submicron DG GaN-MESFET design and its 2-D subthreshold analytical model in order to suppress the short-channel-effects (SCEs) for deep submicron MESFET-based circuits. In the second one, we propose a new GaN-MESFET design, called the Gate All Around (GAA) GaN-MESFET, and its 2-D subthreshold behavior numerical analysis in order to suppress the short-channel-effects (SCEs) for deep submicron MESFET-based circuits.

Part (I): Modeling of subthreshold behaviour for deep submicron DG GaN MESFET

IV.I.1 Subthreshold behaviour of DG GaN MESFET

To increase device speed at small gate lengths, and thereby reducing the accompanying parasitic and SCEs become an important design consideration. In this context, the main objective of the present work is to propose an accurate analytical two-dimensional analysis, comprising 2-D channel potential, threshold voltage and drain induced barrier lowering effect (DIBL) in order to improve the SCEs and the scaling capability of the device for the future high speed digital circuit applications. To analyze the short channel effects behavior in a short gate length DG GaN-MESFET, the 2D Poisson's equation satisfying different boundary conditions has been analytically solved to develop the 2D electrostatic potential distribution in the active region (GaN layer). The analytical model explains the dependence of threshold voltage and DIBL according to the channel length and channel thickness. The subthreshold parameters of both designs have been analysed and compared in order to show the performances provided by the proposed structure. Our analytical analysis demonstrates that the (DG) GaN-MESFET structure exhibits significantly improved performance in terms of threshold voltage roll-off, DIBL and subthreshold swing which make (DG) GaN-MESFET a promising candidate for future GaN-MESFET-based circuits. The closed form analytical expressions for channel potential and threshold voltage are derived and the results so obtained are verified using ATLAS 2D device simulator [125]. The resulting subthreshold characteristics show good agreement with the simulation results.

IV.I.2 Model development

For a deep sub micron gate length MESFET, the solution of 2D Poisson's equation satisfying suitable boundary conditions is required to model the short channel effects. A cross-sectional view of the proposed (DG) GaN-MESFET is shown in Figure IV.1. The structure is symmetric, with double metal gates. $N_{D/S}$ represents the doping level of the drain/source region, respectively. The channel region is bounded by source and drain spacing at x= 0 and L, respectively, where L is the gate length. At y=0 and y=a, it is bounded by the interface of gate metal and n-GaN active region, where 'a' represents the thickness of the active region. We assume that the structure is homogeneous along

the z direction. Hence, we obtain an invariance of the electrical parameters in the z direction (infinite boundary conditions), so that the problem is studied in a (x, y)-domain (Figure IV.1). All computations have been done at room temperature.

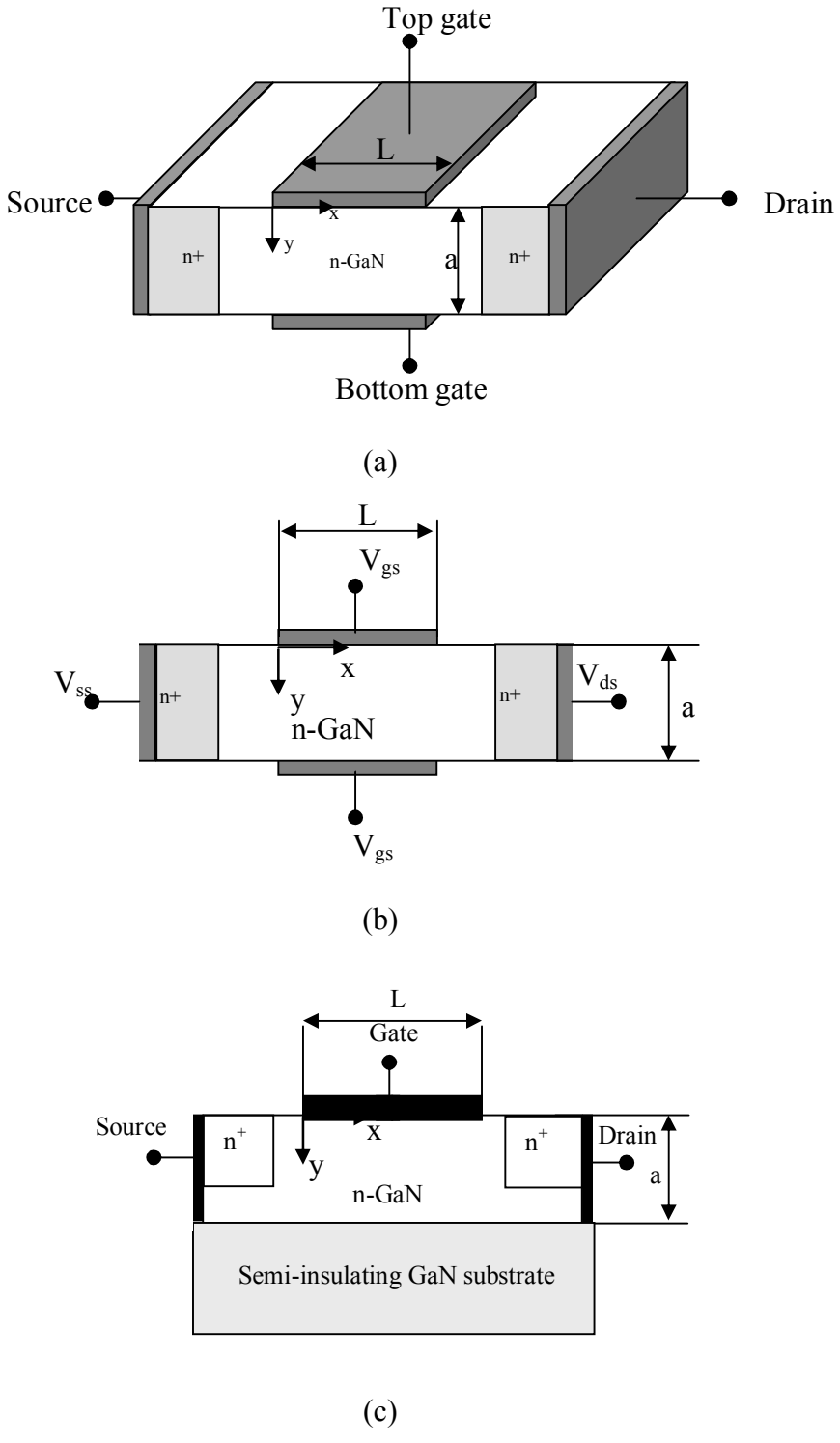


Figure IV.1: GaN-MESFET: (a) DG 3-D structure, (b) DG cross-sectional view through the channel c) SG cross-sectional view through the channel.

IV.I.2.1 Two-dimensional potential analysis

According to Figure IV.1(b), the 2D Poisson's equation for the active region is given by

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = -\frac{q}{\varepsilon_s} N_d \qquad \text{(IV.1)}$$

$\psi(x,y)$ is the electrostatic potential, ε_s is the dielectric permittivity of GaN semiconductor, q is the electron charge, N_d represents the doping concentration in the active region. The boundary conditions for $\psi(x,y)$ are found by satisfying the continuity of the potential at the (Gate metal/GaN) interfaces and at the source/drain sides as:

$$\psi(x,0) = V_0 = V_{bi} - V_{gs} \qquad \text{(IV.2a)}$$

$$\psi(x,a) = V_0 \qquad \text{(IV.2b)}$$

$$\psi(0,y) = V_{bi} - V_{bs} \qquad \text{(IV.2c)}$$

$$\psi(L,y) = V_{bi} - V_{bs} + V_{ds} \qquad \text{(IV.2d)}$$

where V_{bi} is the schottky-barrier built-in potential, V_{gs} is the applied gate-source voltage, V_{bs} is the substrate bias, V_{ds} is the applied drain-source voltage.

In order to find an analytical solution of (IV.1), we apply the superposition principle [12,13], and we write the potential $\psi(x,y)$ as the sum of two terms: $\psi_{1D}(y)$, which is the solution of the 1-D Poisson's equation in the direction perpendicular to the channel, and $\psi_{2D}(x,y)$, which is the solution of the residual 2-D differential equation:

$$\psi(x,y) = \psi_{1D}(y) + \psi_{2D}(x,y) \qquad \text{(IV.3)}$$

Therefore, $\psi_{1D}(y)$ is the solution of:

$$\frac{d^2 \psi_{1D}}{dy^2} = -\frac{q}{\varepsilon_s} N_d \qquad \text{(IV.4)}$$

The boundary conditions of $\psi_{1D}(y)$ are:

$$\psi_{1D}(y)\big|_{y=0,\ and\ y=a} = V_0 \qquad \text{(IV.5)}$$

Substituting (IV.5) in (IV.4), the solution of 1D Poisson's equation is

$$\psi_{1D}(y) = V_0 - \frac{qN_d y^2}{2\varepsilon_s} + \frac{qN_d\, a\, y}{2\varepsilon_s} \qquad \text{(IV.6)}$$

$\psi_{2D}(x,y)$ is the solution of the residual 2-D Poisson's Equation:

$$\frac{\partial^2 \psi_{2D}}{\partial x^2} + \frac{\partial^2 \psi_{2D}}{\partial y^2} = 0 \qquad \text{(IV.7)}$$

The boundary conditions for $\psi_{2D}(x,y)$ are derived from the channel potential $\psi(x,y)$, through (IV.3) and (IV.6) as

$$\psi_{2D}(x,y)\big|_{y=0,\,and\ y=a} = 0 \qquad \text{(IV.8a)}$$

$$\psi_{2D}(0,y) = V_{bi} - V_{bs} - \psi_{1D}(y) \qquad \text{(IV.8b)}$$

$$\psi_{2D}(0,y) = V_{bi} - V_{bs} + V_{ds} - \psi_{1D}(y) \qquad \text{(IV.8c)}$$

The application of the standard technique, of variables separation method [126], allows producing a Fourier series solution. Thus the resulting expression for $\psi(x,y)$ is

$$\psi(x,y) = \psi_{1D}(y) + \sum_{n=1}^{\infty} \frac{\sin(k_n y)}{\sinh(k_n L)} \left[A_n \sinh\left(k_n (L-x)\right) + B_n \sinh(k_n x) \right] \qquad \text{(IV.9)}$$

with

$$k_n = \frac{(2n+1)\pi}{a}$$

$$A_n = (V_{bi} - V_0)\frac{4}{(2n+1)\pi} - \frac{4qN_d}{\varepsilon_s a k_n^3}$$

$$B_n = (V_{bi} - V_0 + V_{ds})\frac{4}{(2n+1)\pi} - \frac{4qN_d}{\varepsilon_s a k_n^3}$$

IV.I.2.2 Threshold voltage model

For submicron MESFETs, short-channel effects such as threshold voltage roll-off and DIBL have an important impact on the device characteristics. The threshold voltage can be defined as the gate voltage which capably accomplishes the minimum potential to maintain the fully depleted channel region. Based on the developed potential expression (IV.9), the threshold voltage can be derived using the condition of the minimum channel potential. Refer to Eq.(IV.9) and set the derivative of $\psi_c(x) = \psi(x,y)\big|_{y=const}$ equals to zero [127]:

$$\frac{d\psi_c(x)}{dx}\Big|_{x=x_{\min}} = 0 \qquad \text{(IV.10)}$$

The position of the minimum channel potential $x_{\min}$ can be found iteratively by

$$\sum_{n=1}^{\infty}\frac{\sin(k_n a/6)}{\sinh(k_n L)}k_n\left[A_n\cosh\left(k_n(L-x_{\min})\right)-B_n\cosh(k_n x_{\min})\right]=0 \qquad \text{(IV.11)}$$

Since the Fourier series coefficients decay rapidly, the first terms, A_1 and B_1, are sufficient to express the Fourier series in Eq.(IV.11), hence $x_{\min}$ can be simply obtained as

$$x_{\min}=\frac{1}{2k_1}\ln\left[\frac{A_1\exp(k_1L)-B_1}{B_1-A_1\exp(-k_1L)}\right] \qquad \text{(IV.12)}$$

After $x_{\min}$ is found, the minimum channel potential can be obtained from (IV.12) and (IV.9) as

$$\psi_{\min}=V_0-\frac{qN_d a^2}{72\varepsilon_s}+\frac{qN_d\,a^2}{12\varepsilon_s}+\sum_{n=1}^{\infty}\frac{\sin(k_n a/6)}{\sinh(k_n L)}\left[A_n\sinh\left(k_n(L-x_{\min})\right)+B_n\sinh(k_n x_{\min})\right]$$

$$\psi_{\min}\approx V_0-\frac{qN_d a^2}{72\varepsilon_s}+\frac{qN_d\,a^2}{12\varepsilon_s}+\frac{\sin(k_1 a/6)}{\sinh(k_1 L)}\left[A_1\sinh\left(k_1(L-x_{\min})\right)+B_1\sinh(k_1 x_{\min})\right]$$

(IV.13)

In accordance with Eqs. (IV.13) and (IV.9), and after some mathematical manipulations, we can define a simple compact threshold voltage model for short channel double-gate MESFETs as

$$V_{th}=V_{th}^0-A_1\sec h(k_1L/2) \qquad \text{(IV.14)}$$

where V_{th}^0 represents the threshold voltage for long channel devices given by

$$V_{th}^0=V_{bi}-\frac{qN_d a^2}{2\varepsilon_s} \qquad \text{(IV.15)}$$

The term $A_1\sec h(k_1L/2)$ represents the threshold voltage degradation parameter due to the short-channel-effects. It should be noted that this parameter can be neglected if channel length L is much larger than active GaN thickness (a). Therefore, in the case of long DG channel GaN-MESFET, the threshold voltage in Eq. (IV.14) can be simplified as $V_{th}=V_{th}^0=V_{bi}-\frac{qN_d a^2}{2\varepsilon_s}$.

IV.I.2.3 Subthreshold swing model

Subthreshold swing, defined as the change of gate voltage needed for an order-of-magnitude change in the subthreshold drain current, is expressed [13,122,123] as

$$S = \frac{\partial V_{gs}}{\partial \log I_{DS}} \approx V_{th} \ln 10 \left[\frac{\partial \psi_{\min}}{\partial V_{gs}} \right]^{-1} \quad \text{(IV.16)}$$

where I_{DS} represents the subthreshold drain current, and V_{th} is the thermal voltage. Since $\psi_{\min}$ has been defined previously, S can be easily obtained after some mathematical manipulations. So, a new compact subthreshold swing model for short channel double-gate MESFETs can be defined as

$$S = V_{th} \ln 10 \left[1 + \Delta S \right]^{-1} \quad \text{(IV.17)}$$

where the term ΔS represents the subthreshold swing degradation parameter due to the short-channel-effects given as

$$\Delta S = \frac{\sin(ky)}{\sinh(kL)} \left[\begin{array}{l} \frac{4}{3\pi} \left[\sinh(k(L - x_{\min})) + \sinh(kx_{\min}) \right] + \\ \frac{2}{3\pi} \frac{(B - A)(\exp(kL) - \exp(-kL))}{(\exp(kL) + \exp(-kL)) - B^2 - A^2} \times \\ \left[\frac{1}{A} \cosh(kx_{\min}) - \frac{1}{B} \cosh(k(L - x_{\min})) \right] \end{array} \right] \quad \text{(IV.18)}$$

From Eq.IV.18, we can see that for long channel devices $\Delta S \approx 0$.

IV.I.3 Results and discussion

Figure IV.2 compares the threshold voltage roll-off versus channel length for the (DG) GaN-MESFET and the conventional GaN-MESFET. It can be observed that the variation of threshold voltage roll-off with channel length is less pronounced in the case of the (DG) GaN-MESFET when compared to the conventional GaN-MESFET. This improved short-channel behavior in the case of double-gate-design can be understood from Figure IV.3, which shows the channel potential, for y=a/6, plots for the (DG) GaN-MESFET and the conventional GaN-MESFET for different channel lengths. We notice that for the conventional GaN-MESFET, as the channel length is reduced, the minimum channel potential is increased due to the interaction between the source and drain regions which causes the decreasing of the threshold voltage. Moreover, in the conventional single gate GaN-MESFET, the gate is the primary terminal that turns on and off the device, while the substrate or the buried contact (in SOI MESFETs design) fulfill a secondary tuning function. However, for (DG) GaN-MESFET design, there is a shift in the potential profile which screens the region near the source end from the

variations in drain voltage and thus ensures a reduction in threshold voltage roll-off effect in comparison with conventional single gate GaN-MESFETs as the channel length is reduced.

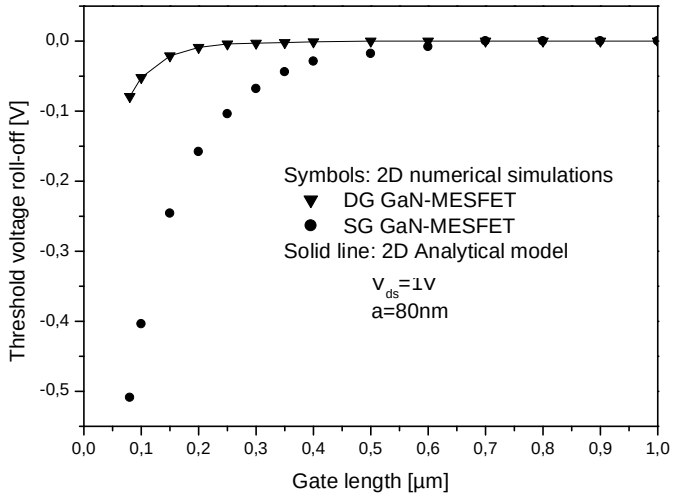


Figure IV.2: Threshold voltage roll-off versus channel length of (DG) GaN-MESFET and conventional GaN-MESFET. Device parameters used for calculating are $V_{gs} = -2V$, $a = 80nm$, $\phi_M = 4.68eV$, $V_{bi} = 1.1V$, $N_d = 3.10^{17} cm^{-3}$, $V_{ds} = 1V$.

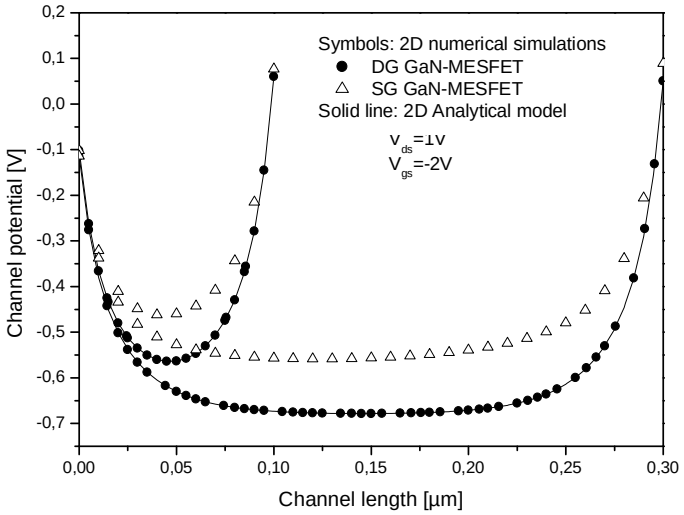


Figure IV.3: Potential variation along the channel of the (DG) GaN-MESFET and conventional GaN-MESFET for different channel lengths. Device parameters used for calculating are $V_{ds} = 1V$,

$V_{gs} = -2V$, $a = 80nm$, $\phi_M = 4.68eV$, $V_{bi} = 1.1V$, $N_d = 3.10^{17} cm^{-3}$

The DIBL effect can be demonstrated by plotting the channel potential as a function of normalized position along the channel. Figure IV.4 shows that as channel length is reduced, the minimum channel potential increases and therefore the channel barrier reduced. Moreover, the drain bias also has an important effect on the DIBL behavior as shown in Figure IV.4, where the increase of the drain bias will result an elevation of the minimum channel potential. Therefore, the channel potential is considerably reduced. This reduction of channel potential may cause the severe subthreshold leakage current. Figure IV.5 shows the variation of DIBL with channel length for both GaN-MESFETs structures. The DIBL is obtained from the difference between the threshold voltage at high drain–source voltage value (2V) and the threshold voltage value at low drain–source voltage value (1V). From Figure IV.5, it can be shown that DIBL effect is lowest for DG GaN-MESFET design as compared to the conventional single gate structure which indicates the fact that the incorporation of multigate design leads to an improvement of short-channel-effects. Morevor, it is interesting to notice that the DIBL effect becomes more pronounced with shrinking the channel length below 100nm for (DG) GaN-MESFET and 500nm for conventional single gate GaN-MESFET, with the DIBL effect becoming less severe for thinner active region layers in the case of DG design due to the better gate control of the active region. Figure IV.6 represents the variation of the calculated subthreshold swing factor with channel length for different active region thicknesses for both structures. It can be shown that the thinner GaN film has a smaller subthreshold swing than the thicker one for both structures. In addition, the (DG) GaN-MESFET exhibits a better subthreshold swing behavior when the channel lengths are reduced to deep submicron scale, where the ideal subthreshold swing value can be reached for L=150nm. It reveals that the degradation of subthreshold swing in deep submicron scale can be alleviated by the use of the thin GaN film and the proposed multigate design. Therefore, the proposed design provides excellent immunity against the short-channel-effects and enhancement in subthreshold swing compared to the conventional devices. Figure IV.7 represents the electric scheme of the analyzed DG GaN-MESFET design in subthreshold regime without parasitic resistances.

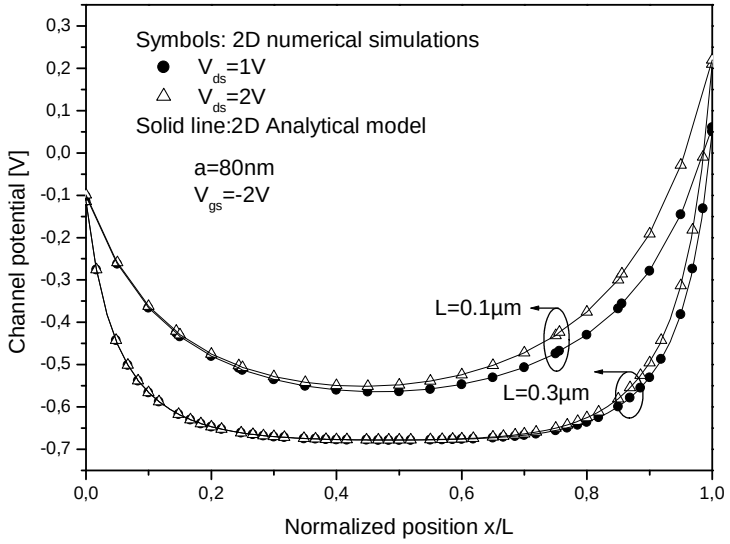


Figure IV.4: Channel potential versus normalized channel position for different drain biases and channel lengths. Device parameters used for calculating are $V_{gs} = -2V$, $a = 80nm$, $\phi_M = 4.68eV$, $V_{bi} = 1.1V$, $N_d = 3.10^{17} cm^{-3}$

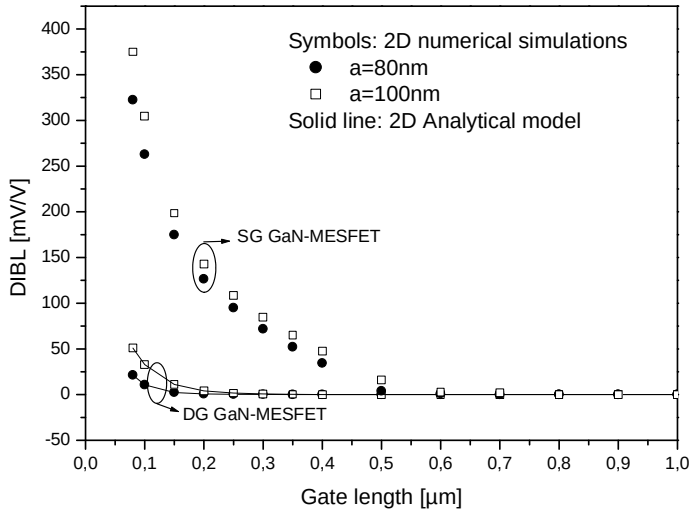


Figure IV.5: Drain induced barrier lowering, DIBL, coefficient as function of channel length for different active region thicknesses.

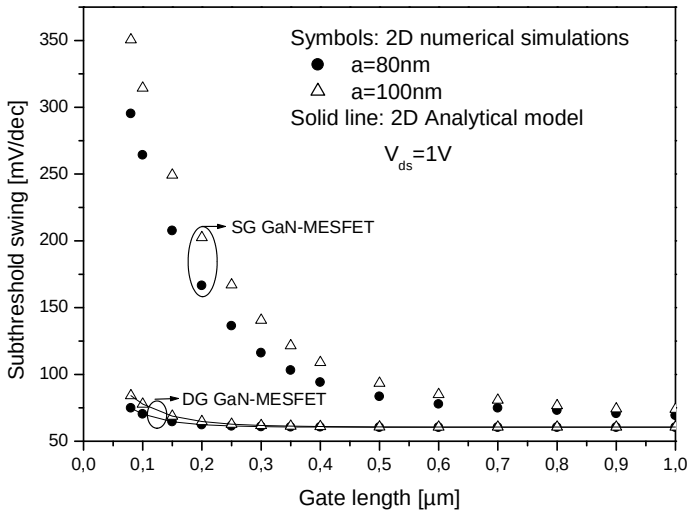


Figure IV.6: Subthreshold swing factor as function of channel length for different active region thicknesses. Device parameters used for calculating are $\phi_M = 4.68eV, V_{bi} = 1.1V, N_d = 3.10^{17} cm^{-3}, V_{ds} = 1V$.

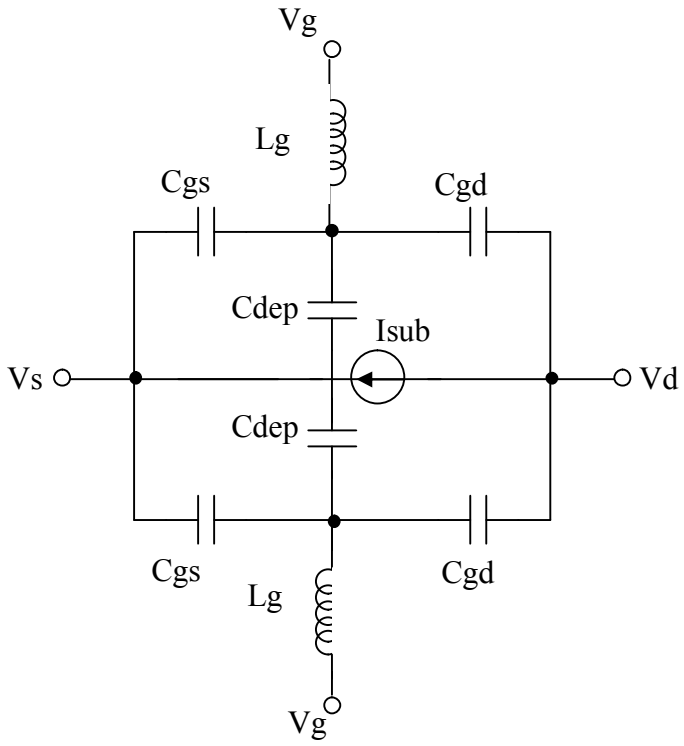


Figure IV.7: Electric scheme of the DG GaN-MESFET without parasitic resistances

IV.I.4 Conclusion

In this work, a new deep submicron multigate GaN-MESFET design and its 2-D subthreshold analytical model have been proposed, investigated and expected to suppress the short-channel-effects (SCEs) for deep submicron FET-based circuits. It has been shown that the incorporation of the multigate design aspect exhibits an improvement in the screening of the channel potential variation, and an enhancement of the short-channel-effects. The law of scaling capability of the proposed structure was compared to the conventional single-gate case, illustrating the improved subthreshold behavior of the DG GaN-MESFET over conventional GaN-MESFETs. The obtained results have been verified and validated using 2D numerical simulations. As device dimensions penetrate into the deep submicron regime, the improved obtained performances make the proposed multigate GaN-MESFET a better choice for future deep submicron FET-based circuits for future electronic switching and digital gate devices.

Part (II): Numerical analysis of subthreshold behaviour for deep submicron GAA GaN MESFET

IV.II.1 Subthreshold behaviour of GAA GaN MESFET

As the channel length rapidly shrinks down to the deep submicron domain, the Short Channel Effects (SCEs), such as the threshold voltage roll-off, the DIBL and the subthreshold swing degradation, cannot be neglected for deep submicron channel lengths, and make the device operating in subthreshold regime more difficult and challenging. To minimize short-channel-effects and improve subthreshold electrical performances, a new architecture and improvement of conventional planar GaN-MESFETs become indispensable.

In the present work, a new design of GaN-MESFET called GAA GaN-MESFET and its 2-D numerical analysis are proposed, investigated and expected to suppress the short-channel-effects (SCEs) and improve the subthreshold behavior for deep submicron GaN-MESFET-based applications. The numerical analysis investigates the dependence of threshold voltage, DIBL and subthreshold swing according to the channel length and channel thickness. The subthreshold parameters of both architectures (GAA and planar) have been analysed and compared in order to show the performances provided by the proposed design. Our numerical results demonstrate that the GAA GaN-MESFET design exhibits significantly improved performances in terms of threshold voltage roll-off, DIBL and subthreshold swing, which make GAA GaN-MESFET a promising candidate for deep submicron GaN-MESFET-based circuits.

IV.II.2 Numerical analysis

Figure IV.8 shows the cross section of the symmetrical GAA GaN-MESFET considered in this work. The channel is undoped, the n^+ source and drain are highly doped, and all simulations have been done at room temperature. By surrounding the channel completely (Fig. IV.8), the gate gains increased electrostatic control of the channel and short-channel effects can be drastically suppressed.

The channel region (active region) is bounded by source and drain spacing at z= 0 and L, respectively, where L is the gate length. At r=0 and r=a/2, it is bounded by the interface of gate metal (work function $\phi_M = 4.68eV$) and n-GaN active region, where ‘a’ represents the thickness (diameter) of the active region.

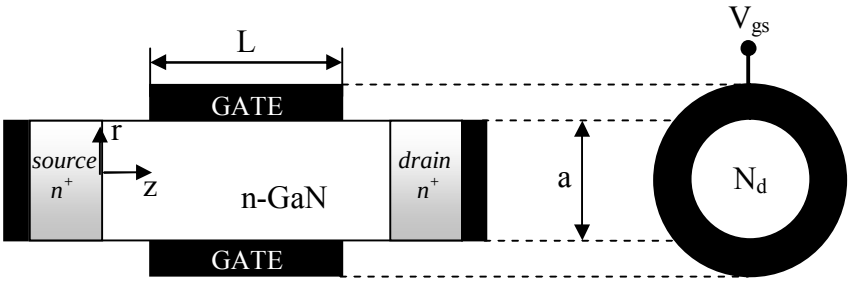


Figure IV.8: Cross-sectional view through the channel of the proposed GAA GaN-MESFET

Refer to Figure IV.8 by accounting for the angular symmetry of the GAA GaN-MESFET; the channel electrostatics potential is governed by the cylindrical 2D Poisson equation:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi}{\partial r}\right)+\frac{\partial^2 \psi}{\partial z^2}=-\frac{q}{\varepsilon_s}N_d \qquad \text{(IV.19)}$$

$\psi(z,r)$ is the electrostatic potential, ε_s is the dielectric permittivity of GaN semiconductor, q is the electron charge, N_d represents the doping concentration in the active region. The boundary conditions for $\psi(z,r)$ are found by satisfying the continuity of the potential at the (Gate metal/GaN) interfaces and at the source/drain sides as:

$$\psi(z,a/2)=V_0 \qquad \text{(IV.20b)}$$

$$\psi(0,r)=V_{bi}-V_{bs} \qquad \text{(IV.20c)}$$

$$\psi(L,r)=V_{bi}-V_{bs}+V_{ds} \qquad \text{(IV.20d)}$$

with $V_0=V_{bi}-V_{gs}$

where V_{bi} is the schottky-barrier built-in potential, V_{gs} is the applied gate-source voltage, V_{bs} is the substrate bias, V_{ds} is the applied drain-source voltage.

The numerical analysis is performed using 2D ATLAS simulator [125] to compare the subthreshold characteristics of the proposed GAA GaN-MESFET design with conventional planar single gate GaN-MESFET [13] on the basis of threshold voltage variation with gate length, DIBL, and subthreshold slope. The DIBL is calculated as the

difference between the linear threshold voltage, for V_{ds} = 1V, and the saturation threshold voltage, V_{ds} = 3V, at a constant drain current.

IV.II.3 Scaling capability of GAA GaN-MESFET

The threshold voltage roll-off is a consequence of the charge sharing effect and typically considered one of the main indications of the short channel effects. Figure IV.9 shows the threshold voltage roll-off due to SCEs as a function of channel length at the bias condition of V_{ds} = 1V. It is observed that the threshold voltage roll-off in the proposed design doesn't differ considerably from that of the conventional planar device for longer channel length. However, this difference becomes more apparent for very short channel length devices (less than 0.35 µm). This observation can be explained by the effect of the increased electrostatic control of the channel provided by the gate around architecture. However, in the conventional planar GaN-MESFET, the gate is the primary terminal that turns on and off the device; while the substrate (bulk MESFETs design) or the buried contact (SOI MESFETs design) fulfill a secondary tuning function. Figure IV.10 shows the DIBL as a function of the channel length for both devices (GAA and conventional planar designs). The DIBL is obtained from the difference between the threshold voltage at high drain-source voltage value (3V) and the threshold voltage value at low drain-source voltage (1V).

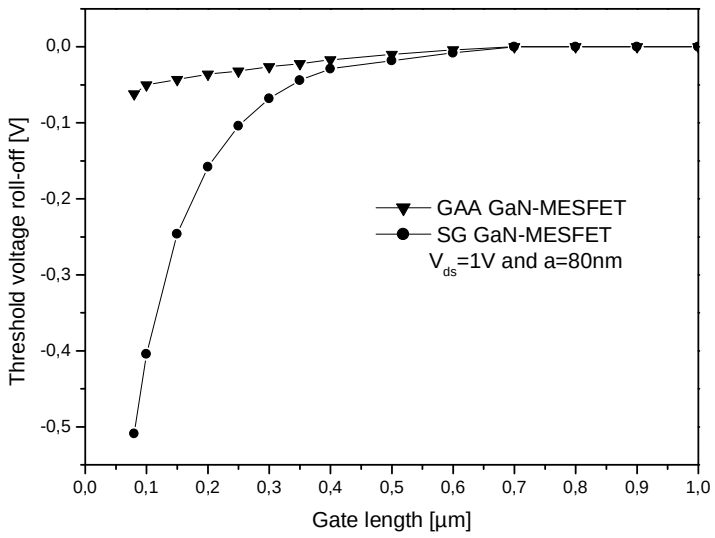


Figure IV.9: Threshold voltage roll-off versus channel length of GAA GaN-MESFET and conventional planar GaN-MESFET. Device parameters used for calculating are $a = 80nm$, $\phi_M = 4.68eV$, $V_{bi} = 1.1V$, $N_d = 3.10^{17} cm^{-3}$, $V_{ds} = 1V$.

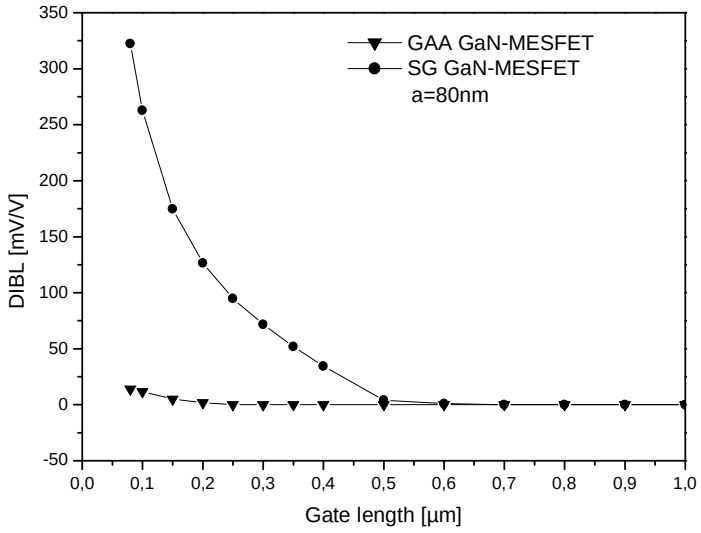


Figure IV.10: Drain induced barrier lowering, DIBL, coefficient as function of channel length for both designs (GAA and planar structure)

It is observed that the DIBL effect is more pronounced in very short channel length (deep submicron device) in the case of conventional planar MESFETs. Contrary, the recorded DIBL effect shows lowest values in the GAA MESFET design as compared to conventional planar structure which indicates the fact that the incorporation of the multigate aspect leads to an improvement of short-channel-effects for deep submicron devices.

Figure IV.11 plots the subthreshold swing as a function the device dimensions calculated from our numerical analysis. It can be noticed that the subthreshold swing increases rapidly as the device length reduced to L=0.3 µm in the case of conventional planar MESFETs, and reaches the ideal subthreshold swing value (60mV/dec) for L=0.9µm. However, the GAA GaN-MESFET exhibits a better subthreshold swing behavior when the channel lengths reduced to deep submicron scale, where the ideal subthreshold swing value can be reached for L=0.15µm. Therefore, the proposed design provides excellent immunity against the short-channel-effects and enhancement in subthreshold swing compared to the conventional devices. The control capability of the channel region is deeply depend to the device diameter (channel thickness). From Figure IV.12, It can be seen that the subthreshold swing decreases rapidly as the device diameter is reduced to 0.1µm, and reaches the ideal subthreshold swing value when a<0.08µm. The most important conclusion is that the GAA GaN-MESFET can satisfy

the same subthreshold swing value as conventional planar GaN-MESFET with a channel length 83**%** shorter than that given by conventional planar GaN-MESFET (Fig. IV.11) with also a lower threshold roll-off and DIBL values.

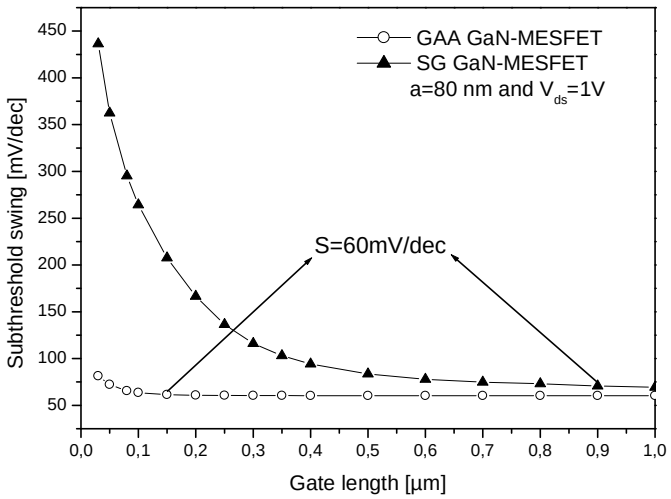


Figure IV.11: Subthreshold swing factor as function of channel length for both architectures. Device parameters used for calculating are $\phi_M = 4.68eV, V_{bi} = 1.1V, N_d = 3.10^{17} cm^{-3}, V_{ds} = 1V$

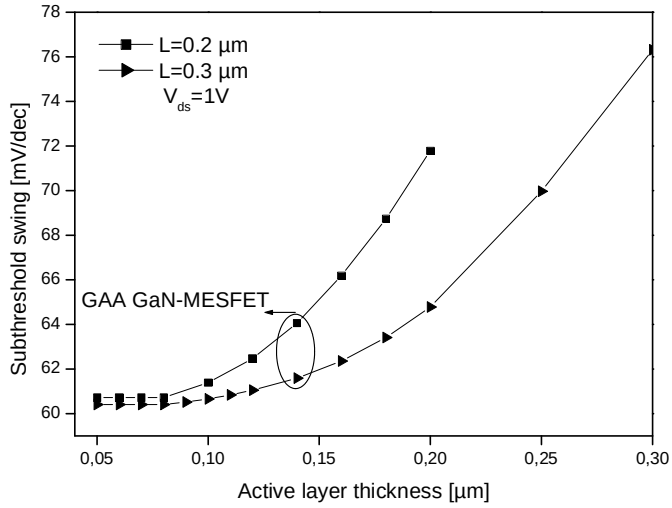


Figure IV.12: Subthreshold swing factor as function of channel thickness (diameter) for different channel lengths. Device parameters used for calculating are $\phi_M = 4.68eV, V_{bi} = 1.1V, N_d = 3.10^{17} cm^{-3}, V_{ds} = 1V$.

Table IV.1 shows a comparison between the three structures (conventional, DG and GAA GaN MESFET) by using the same variables design, where the GAA structure illustrates better performance in terms of threshold voltage roll-off, DIBL and subthreshold swing factor.

Quantity	Conventional GaN MESFET	Double gate GaN MESFET	Gate all around GaN MESFET
Threshold voltage roll-off (V)	-0.5	-0.079	-0.062
DIBL (mV/V)	322.4	21.29	14
Subthreshold swing (mV/dec)	295.22	74.8	65.53

Table IV.1: Comparison between the three structures; conventional, DG and GAA GaN MESFET

IV.II.4 Conclusion

In this work, a new GaN-MESFET design, called the Gate All Around (GAA) Gallium Nitride (GaN)-MESFET (GAA GaN-MESFET), and its 2-D subthreshold behavior numerical analysis have been proposed, investigated and expected to suppress the short-channel-effects (SCEs) for deep submicron FET-based circuits. The performances of the proposed design were compared to the conventional planar GaN-MESFET, illustrating the superior performance of the proposed device with respect to the conventional planar GaN-MESFET in terms of threshold roll-off, DIBL and subthreshold swing performances. The obtained results make the proposed GAA GaN-MESFET a very promising candidate for future deep submicron FET-based devices.

Chapter V

Multi-gate Engineering approach to improve the III-V-based FETs performances

V.1 Introduction

III-V based metal semiconductor field effect transistors (MESFETs) have demonstrated excellent superior noise immunity, enhanced radiation hardness, high thermal conductivity and simplicity of fabrication and gain performance at microwave frequency and they are used quite often in circuit amplifiers for communication and power applications [10-12]. In today's world, high frequency communication and power applications are possible because of the superior electrical properties offered by III-V based MESFETs both in analog as well as in digital applications. Although III-V based MESFETs have good performances for high frequency and speed circuit applications, potential ways to enhance them for high frequency, high power and microwave applications is still worth investigating. Numerous III-V based MESFET structures have been reported and investigated to have reached this goal and optimized over the last few years [10-13].

The main objective of this chapter is to propose a new optimized Dual-Material-gate (DM) III-V MESFET-based design using Multi-Objective Genetic Algorithms (MOGAs) and Multi-gate Engineering aspect to improve the SCEs and the scaling capability of the device for the future high speed digital and analog circuit applications. We will present the applicability of multi-objective genetic algorithms optimization (MOGAs) approach to optimize the subthreshold behavior of (DM) GaN-MESFETs and the analog electrical behavior of (DM) GaAs-MESFETs for high speed submicron digital and analog applications, respectively.

This chapter is organized in tow parts. In the first part, we describe the concept of dual-material gate design and its 2-D subthreshold analytical model in order to suppress the short-channel-effects and hot carrier effect for deep submicron GaN-MESFET-based circuits. In addition, a MOGA-based approach will be proposed to maximize the subthreshold electrical performance of the investigated DM GaN-MESFET. In the second part, we investigate the performance of the proposed design. This latter will be applied to the GaAs-MESFET structure to study and improve the analog electrical

behavior by developing new analytical models, which describe the device behavior for analog applications. Moreover, MOGAs-based approach will be proposed to optimize the electrical performance of DM GaAs-MESFET for submicron MESFET-based analog circuit design.

Part (I): Modeling and optimization of subthreshold performances

V.I.1 Subthreshold regime

The subthreshold regime of operation of the MESFETs is very important for analyzing the operation of all MESFET-based digital circuits since it represents one of the two stationary stages of the digital circuits. A direct way to improve the high speed behavior and scaling capabilities of the GaN-MESFET is the reduction of its gate length. However, with the reduction in channel length, control of short-channel effects (SCEs) and drain current in subthreshold regime is one of the biggest challenges in further downscaling of the technology. To increase device speed at small gate lengths, and thereby reducing the accompanying parasitic and SCEs become an important design consideration. The proposed design is similar to that of a conventional single material gate (SM) GaN-MESFET with the exception that the gate of the DM GaN-MESFET structure consists of two materials. The first step of the proposed approach consists of accurate compact modeling of subthreshold parameters for submicron Dual-Material-gate (DM) GaN-MESFET. The different compact models can be used in our study as objective functions, which are given as function of input design variables. The design of optimal submicron (DM) GaN-MESFETs will require new insights into the underlying physics, especially two dimensional analysis of the electric field and electrostatic potential in short channel and thin GaN films.

Design optimization, adopted in this work, is the process of finding the maximum/minimum of the subthreshold parameters called the objective functions and must also satisfy a certain set of specified requirements within constraints [11]. In this work, an accurate analytical two-dimensional model, comprising 2-D channel potential, threshold voltage, drain induced barrier lowering effect (DIBL) and parasitic resistances, is presented in order to explain the advantages of the proposed DM GaN-MESFET design over the conventional single material gate (SM) GaN-MESFET with the same geometric specifications that allow us to utilize the benefits of the

incorporation of the dual-material-gate aspect on the immunity of the proposed design against the short-channel- effects. Our analytical modeling and MOGA-based optimization demonstrate that the proposed (DM) GaN-MESFET structure exhibits significantly improved performances in terms of threshold voltage roll-off, DIBL, subthreshold swing and parasitic resistances which make the proposed design as a promising candidate for future GaN-MESFET-based circuits. The closed form analytical expressions for channel potential and threshold voltage are derived and the results so obtained are verified using ATLAS 2D device simulator [125].

V.I.2 Computation Methodology

Schematic cross-sectional view of the proposed DM GaN-MESFET is presented in Figure V.1. The gate consists of dual materials M1 and M2 of lengths L_1 and L_2, respectively. $N_{D/S}$ represents the doping level of the drain/source region, respectively. The channel region is bounded by source and drain spacing at x= 0 and L, respectively, where L is the gate length. At *y=0* and y=a, it is bounded by the interface of gate metal and n-GaN active region and the bulk, respectively.

For deep submicron devices, the solution of 2D Poisson's equation satisfying suitable boundary conditions is required to model the short channel effects. Refer to Figure V.1, the 2D Poisson's equation for the active region is given by:

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = -\frac{q}{\varepsilon_s} N_d \qquad \text{(V.1)}$$

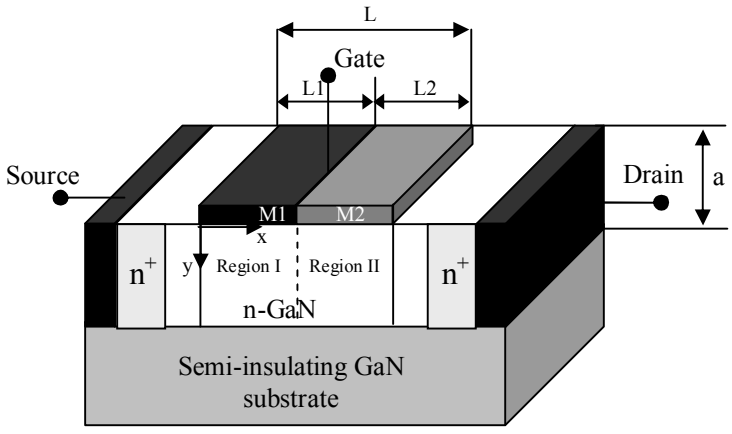


Figure V.1: Cross-sectional view of the proposed DM GaN-MESFET

$\psi(x,y)$ is the electrostatic potential, ε_s is the dielectric permittivity of GaN semiconductor, q is the electron charge, N_d represents the doping concentration in the active region. The boundary conditions for $\psi(x,y)$ are found by satisfying the continuity of the potential at the (Gate metal/GaN) interfaces and at the source/drain sides as:

$$\psi(x,0) = V_0 \tag{V.2a}$$

$$\frac{\partial\psi(x,a)}{\partial y} = 0 \tag{V.2b}$$

$$\psi(0,y) = V_{bi} - V_{bs} \tag{V.2c}$$

$$\psi(L,y) = V_{bi} - V_{bs} + V_{ds} \tag{V.2d}$$

with $V_0 = V_{bi} - V_{gs}$

where V_{bi} is the schottky-barrier built-in potential, V_{gs} is the applied gate-source voltage, V_{bs} is the substrate bias, V_{ds} is the applied drain-source voltage.

In order to find an analytical solution of (V.1), we apply the superposition principle [126], and we write the potential $\psi(x,y)$ as the sum of two terms: $\psi_{1D}(y)$, which is the solution of the 1-D Poisson's equation in the direction perpendicular to the channel, and $\psi_{2D}(x,y)$, which is the solution of the residual 2-D differential equation:

$$\psi(x,y) = \psi_{1D}(y) + \psi_{2D}(x,y) \tag{V.3}$$

Therefore, $\psi_{1D}(y)$ is the solution of:

$$\frac{d^2\psi_{1D}}{dy^2} = -\frac{q}{\varepsilon_s}N_d \tag{V.4}$$

The boundary conditions of $\psi_{1D}(y)$ are:

$$\psi_{1D}(y)\big|_{y=0} = V_0 \tag{V.5}$$

Using (V.5) in (V.4), the solution of 1D Poisson's equation is

$$\psi_{1D}(y) = V_0 - \frac{qN_d y^2}{2\varepsilon_s} + \frac{qN_d\, a\, y}{\varepsilon_s} \tag{V.6}$$

$\psi_{2D}(x,y)$ is the solution of the residual 2-D Poisson's Equation:

$$\frac{\partial^2\psi_{2D}}{\partial x^2} + \frac{\partial^2\psi_{2D}}{\partial y^2} = 0 \tag{V.7}$$

The boundary conditions for $\psi_{2D}(x,y)$ are derived from the boundary conditions for $\psi(x,y)$, through (V.3) and (V.6) as

$$\psi_{2D}(x,0)=0 \tag{V.8a}$$

$$\frac{\partial\psi_{2D}(x,a)}{\partial y}=0 \tag{V.8b}$$

$$\psi_{2D}(0,y)=V_{bi}-V_{bs}-\psi_{1D}(y) \tag{V.8c}$$

$$\psi_{2D}(L,y)=V_{bi}-V_{bs}+V_{ds}-\psi_{1D}(y) \tag{V.8d}$$

Applying the standard technique of separation of variables [126] produces a Fourier series solution. Thus the resulting expression for $\psi(x,y)$ is

$$\psi(x,y)=\psi_{1D}(y)+\sum_{n=1}^{\infty}\frac{\sin(k_n y)}{\sinh(k_n L)}\left[A_n\sinh\left(k_n(L-x)\right)+B_n\sinh(k_n x)\right] \tag{V.9}$$

The constants of (V.9), for the case of SM GaN MESFET where the gate consists of only one material, can be found from the boundary conditions (V.2a)-(V.2d) as,

$$k_n=\frac{(2n+1)\pi}{2a},\quad A_n=(V_{bi}-V_0)\frac{4}{(2n+1)\pi}-\frac{2qN_d}{\varepsilon_s a k_n^3}\ and\ B_n=(V_{bi}-V_0+V_{ds})\frac{4}{(2n+1)\pi}-\frac{2qN_d}{\varepsilon_s a k_n^3}$$

In a SM GaN MESFET, the gate consists of only one material, but in the proposed design (DM), we have two different materials with work functions ϕ_{M1} and ϕ_{M2}, respectively. Therefore, the schottky-barrier built-in potential V_{bi} at the gate, for each region, would be different and they are given as

$$V_{01}=V_{bi1}-V_{gs} \tag{V.10a}$$

$$V_{02}=V_{bi2}-V_{gs} \tag{V.10b}$$

where V_{bi1} and V_{bi2} are the schottky-barrier built-in potential for both regions, respectively.

The Poisson's equation is solved separately under the two gate materials using the boundary condition which satisfies the continuity of the channel potential and the electric flux at the interface of two dissimilar gate materials of the gate. Therefore, we have

$$\psi_1(x,y)\big|_{x=L_1}=\psi_2(x,y)\big|_{x=L_1}=V_p \tag{V.11a}$$

$$\left.\frac{d\psi_1(x,y)}{dx}\right|_{x=L_1}=\left.\frac{d\psi_2(x,y)}{dx}\right|_{x=L_1} \tag{V.11b}$$

Based on the boundary conditions given in (V.11a) and (V.11b), the interfacial potential (V_p) can be given as

$$V_p = \frac{\cosh(k_1 L_1).(\lambda V_{01} + \gamma) + A_1 + \frac{\sinh(k_1 L_1)}{\sinh[k_1 (L - L_1)]}\left[\cosh[k_1 (L - L_1)].(\lambda V_{02} + \gamma) + D_1\right]}{\lambda.\left[\cosh(k_1 L_1) + \sinh(k_1 L_1).\coth[k_1 (L - L_1)]\right]}$$

(11c)

with $\lambda = \frac{4}{3\pi}$ and $\gamma = \frac{2qN_d}{\varepsilon_s a\, k_1^3}$

From (V.9) and the boundary conditions (V.2a)-(V.2d), (V.11a) and (V.11b), the 2D channel potential including the dual-gate aspect can be given as

$$\psi_1(x,y) = \psi_{1D,1}(y) + \sum_{n=1}^{\infty} \frac{\sin(k_n y)}{\sinh(k_n L_1)}\left[A_n \sinh\left(k_n (L_1 - x)\right) + B_n \sinh(k_n x)\right] \qquad \text{(V.12a)}$$

with

$$\psi_{1D,1}(y) = V_{01} - \frac{qN_d y^2}{2\varepsilon_s} + \frac{qN_d\, a\, y}{\varepsilon_s}$$

$$k_n = \frac{(2n+1)\pi}{2a}, \quad A_n = (V_{bi1} - V_{01})\frac{4}{(2n+1)\pi} - \frac{2qN_d}{\varepsilon_s a\, k_n^3}, \quad B_n = (V_p - V_{01})\frac{4}{(2n+1)\pi} - \frac{2qN_d}{\varepsilon_s a\, k_n^3}$$

$$\psi_2(x,y) = \psi_{1D,2}(y) + \sum_{n=1}^{\infty} \frac{\sin(k_n y)}{\sinh(k_n (L - L_1))}\left[C_n \sinh\left(k_n (L - x)\right) + D_n \sinh(k_n (x - L_1))\right]$$

(V.12b)

with

$$\psi_{1D,2}(y) = V_{02} - \frac{qN_d y^2}{2\varepsilon_s} + \frac{qN_d\, a\, y}{\varepsilon_s}$$

$$k_n = \frac{(2n+1)\pi}{2a},\ C_n = (V_p - V_{02})\frac{4}{(2n+1)\pi} - \frac{2qN_d}{\varepsilon_s a\, k_n^3},\ D_n = (V_{bi2} + V_{ds} - V_{02})\frac{4}{(2n+1)\pi} - \frac{2qN_d}{\varepsilon_s a\, k_n^3}$$

where $\psi_{1D,1}(y)$ *and* $\psi_{1D,2}(y)$ represent the 1D solutions of Poisson's equation for both gate material regions, respectively.

The electric-field distribution along the channel length can be obtained by differentiating the channel potential given by (V.12a) and (V.12b) and can be written as

for $0 \le x \le L_1$ (under M1)

$$E_1(x) = \left.\frac{d\psi_1(x,y)}{dx}\right|_y = \sum_{n=1}^{\infty} \frac{\sin(k_n y)}{\sinh(k_n L_1)} \left[-k_n A_n \cosh\left(k_n (L_1 - x)\right) + k_n B_n \cosh(k_n x)\right] \quad \text{(V.13a)}$$

for $L_1 \le x \le L$ (under M2)

$$\begin{aligned} E_2(x) &= \left.\frac{d\psi_2(x,y)}{dx}\right|_y \\ &= \sum_{n=1}^{\infty} \frac{\sin(k_n y)}{\sinh(k_n (L - L_1))} \left[-k_n C_n \cosh\left(k_n (L - x)\right) + k_n D_n \cosh(k_n (x - L_1))\right] \end{aligned} \quad \text{(V.13b)}$$

The above two equations are quite useful in determining how the drain side electric field is modified by the proposed design.

V.I.2.1 Threshold voltage model

The threshold voltage can be defined as the gate voltage which capably accomplishes the minimum potential to maintain the fully depleted channel region. Based on the developed potential expression (V.12), the threshold voltage can be derived using the condition of the minimum channel potential. Refer to Eq (V.12) and set the derivative of $\psi_c(x) = \psi(x,y)\big|_{y=const}$ equal to zero [3]: $\left.\frac{d\psi_c(x)}{dx}\right|_{x=x_{\min}} = 0$. It is to note that the minimum channel potential position is located in the first region (Figure V.2).

The position of the minimum channel potential $x_{\min}$ can be found iteratively from

$$\sum_{n=1}^{\infty} \frac{\sin(k_n a/8)}{\sinh(k_n L_1)} k_n \left[A_n \cosh\left(k_n (L_1 - x_{min1})\right) - B_n \cosh(k_n x_{min1})\right] = 0 \quad \text{(V.14)}$$

Since the Fourier series coefficients decay rapidly, the first terms, A_1 and B_1, are sufficient to express the Fourier series in Eq.(V.14), hence the x_{min1} can be simply obtained as

$$x_{min1} = \frac{1}{2k_1} \ln\left[\frac{A_1 \exp(k_1 L_1) - B_1}{B_1 - A_1 \exp(-k_1 L_1)}\right] \quad \text{(V.15)}$$

After $x_{\min 1}$ is solved, the minimum channel potential can be obtained from (V.12) and (V.15) as:

$$\psi_{min1} \approx V_{01} + \frac{15\,qN_d\,a^2}{128\varepsilon_s} + \frac{\sin(k_1 a/8)}{\sinh(k_1 L_1)}\left[A_1 \sinh\left(k_1(L_1 - x_{min1})\right) + B_1 \sinh(k_1 x_{min1})\right] \quad \text{(V.16)}$$

In accordance with Eqs (V.12) and (V.15), and after some mathematical manipulations, we can define a simple compact threshold voltage model for short channel DM GaN- MESFETs as

$$V_{th} = V_{th0} - A_1 . \frac{\sin(k_1 a/8)}{\sinh(k_1 L_1)}\left[\sinh[k_1(L_1 - \frac{L}{2})] + \alpha \sinh(k_1 L/2)\right] \quad \text{(V.17)}$$

with $\alpha = \dfrac{\cosh(k_1 L_1) + \cosh[k_1(L_1 - L)]}{1 + \cosh(k_1 L)}$

where V_{th0} represents the threshold voltage for long channel devices given by

$$V_{th0} = V_{bi} - \frac{qN_d a^2}{2\varepsilon_s} \quad \text{(V.18)}$$

V.I.2.2 Subthreshold swing model

Based on the assumption that the subthreshold swing *S* depends mainly on the carrier concentration at the minimum potential located at a the depth *y* of the active region, an analytical expression for *S* can be derived as

$$S \approx V_t \ln 10\left[\frac{\partial \psi_{min}}{\partial V_{gs}}\right]^{-1} = V_t \ln 10\left[1 + \Delta S\right]^{-1} \quad \text{(V.19)}$$

where V_t is the thermal voltage and ΔS represents the subthreshold swing degradation parameter due to the short-channel-effects given as

$$\Delta S = \frac{\sin(k_1 y)}{\sinh(k_1 L_1)}\left[\begin{array}{l} \chi.\sinh(k_1 x_{min1}) - \dfrac{4}{3\pi}\sinh[k_1(L_1 - x_{min1})] + \\ \dfrac{\sinh(k_1 L_1)(\frac{4}{3\pi}B_1 + \chi.A_1)}{2\cosh(k_1 L_1) - B_1^2 - A_1^2} \times \\ \left[\dfrac{1}{B_1}\cosh[k_1(L_1 - x_{min1})] - \dfrac{1}{A_1}\cosh(k_1 x_{min1})\right] \end{array}\right] \quad \text{(V.20)}$$

with

$$\chi = \frac{\frac{4}{3\pi}\left[\cosh(k_1 L_1) - 1 + \dfrac{\sinh(k_1 L_1)}{\sinh[k_1(L - L_1)]}\left[\cosh[k_1(L - L_1)] - 1\right]\right]}{\cosh(k_1 L_1) + \sinh(k_1 L_1).\coth[k_1(L - L_1)]}$$

V.I.2.3 Subthreshold current model

Following the subthreshold current model proposed by S. Jit et al [128] for short-channel Si-MESFETs, the current in the subthreshold regime can be described as

$$I_{ds-sun} = I_0 \exp\left(\frac{V_{gs} - V_{th0} - \Delta V_{th} + \Gamma V_{ds}}{V_t (1+\Delta S)^{-1}}\right) \quad \text{(V.21)}$$

where ΔV_{th} is the change in the threshold voltage of the short-channel device due to DIBL at $V_{ds} = 0V$; Γ represents an empirical parameter which measures the influence of the drain potential on the threshold voltage [128]; and I_0 is the drain current for low V_{ds} and at $V_{gs} = V_{th0} + \Delta V_{th}$ [128].

V.I.2.4 MESFET parasitic resistances model

In order to fully benefit from the expected performance of the coming technology nodes, all the parasitic components have to be reduced as much as possible. In particular, the parasitic device resistances, which are the drain resistance in series with the source one, will have to be drastically decreased as we will reduce the device length. the MESFET parasitic resistance can be given [129] by

$$R_{Par} = R_s + R_D \quad \text{(V.22)}$$

with $R_S = \frac{L_{gs}}{qN_d Wa\mu_n}$, $R_D = \frac{L_{gd}}{qN_d Wa\mu_n}$.

where R_s and R_D represent the source and drain resistances, respectively, L_{gs} and L_{ds} represent the gate-source and gate-drain lengths, respectively, and μ_n represents the low electron mobility for the GaN material.

V.I.3 Results and discussion

Figure V.2 shows the calculated channel potential for a channel length of 200nm ($L_1 = L_2 = 100nm$) at the channel depth y = a/8. It is clear seen that DM GaN-MESFET exhibits a step function in the channel potential along the channel. This step function profile ensures screening of the channel region under the material on the source side (M1) from drain voltage variations. This means that the drain voltage has very little effect on the subthreshold current, and therefore, the DIBL effect can be reduced in this case. Figure V.3 shows the calculated electric field along the channel length for the DM GaN-MESFET and the predicted values for the SM GaN-MESFET for the same channel

length. Due to the discontinuity in the channel potential of the DM GaN-MESFET, the peak electric field at the drain is reduced substantially, by approximately 20%, when compared with that of the SM GaN-MESFET that leads to a reduced hot carrier effect. This effect is considered as the main failure parameter which affects the device performances for high-speed circuit applications.

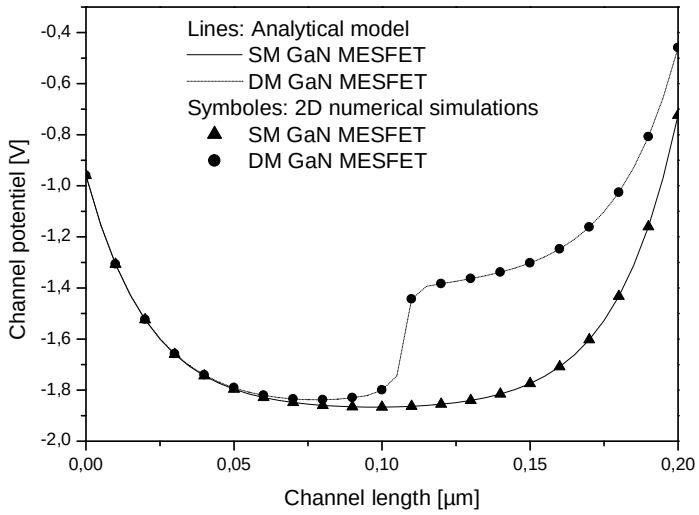


Figure V.2: Potential variation along the channel of the DM GaN-MESFET and conventional SM GaN-MESFET. Device parameters used for calculating are $V_{ds} = 1V$ $V_{gs} = -1V, a = 100nm, \phi_{M1} = 5.1eV, \phi_{M2} = 4.68eV,\ V_{bi1} = 1.6V, V_{bi2} = 1.1V\ N_d = 3.10^{17}\ cm^{-3}$

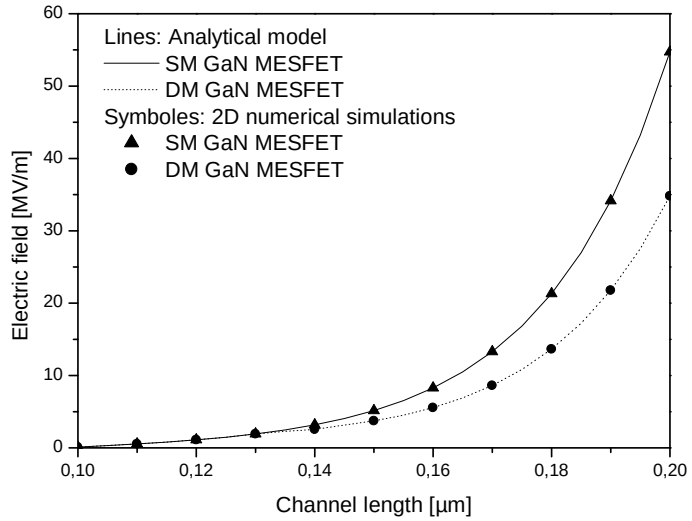


Figure V.3: Electric-field variation along the channel of DM and SM GaN-MESFETs for a channel length L=0.2µm ($L_1 = L_2 = 0.1\mu m$).

In Figure V.4, the threshold voltage roll-off of the proposed design (DM) as a function of a channel length at the bias condition of $V_{ds} = 1V$ is compared with that of the conventional SM GaN-MESFET. It is shown that the model calculations are in good agreement with the simulation results for a wide range of channel lengths. It is observed that the threshold voltage roll-off in the conventional device doesn't differ considerably from that of the DM design for longer channel lengths. However, this difference becomes more apparent for very short channel length devices (less than 250 nm). This is due to the increase in the L_1 / L_2 ratio for the decreasing channel lengths and the portion of the larger work function gate in increased as the channel length reduced. This improvement in the threshold voltage roll-off behavior, for the proposed design, can be explained by the impact of the step function profile on the channel minimum potential computations.

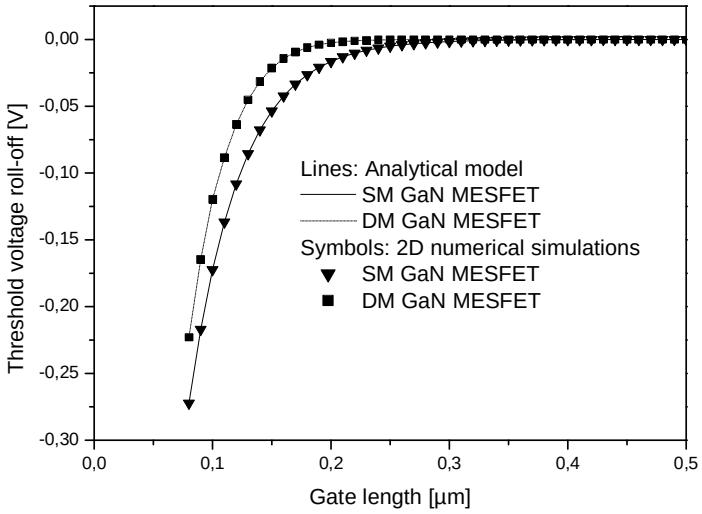


Figure V.4: Threshold voltage roll-off versus channel length of DM GaN-MESFET and conventional SM GaN-MESFET. Device parameters used for calculating are $V_{gs} = -0.5V, a = 100nm, \phi_{M1} = 5.1eV, \phi_{M2} = 4.68eV, V_{bi1} = 1.6V, V_{bi2} = 1.1V\ N_d = 3.10^{17}\ cm^{-3}$ $V_{ds} = 1V$.

Figure V.5 represents the variation of the calculated subthreshold swing factor with channel length for different work function values for both structures. It can be observed that the DM GaN-MESFET exhibits a better subthreshold swing behavior when the channel lengths reduced to deep submicron scale. It reveals that the degradation of subthreshold swing in deep submicron scale can be alleviated by the use

of the proposed DM design. Therefore, the proposed design provides excellent immunity against the short-channel-effects and the hot carrier effect. In addition, an enhancement in subthreshold swing compared to the conventional devices can be found. We can see that the proposed analytical models provide a good agreement for a very wide interval of dimensional and electrical parameters for deep submicron DM GaN-MESFETs in comparison with 2D numerical simulations. Therefore, the developed analytical models can be used as objective functions in our MOGAs-based optimization approach.

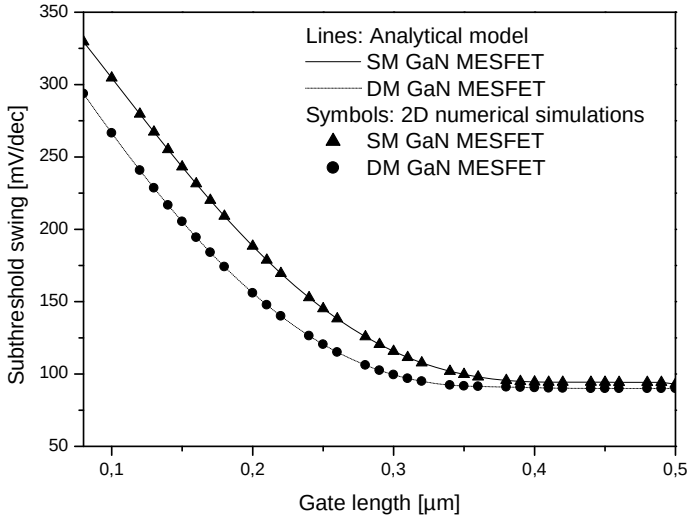


Figure V.5: Subthreshold swing factor as function of channel length for both designs. Device parameters used for calculating are
$\phi_{M1} = 5.1eV, V_{bi1} = 1.6V,\ \phi_{M2} = 4.68eV, V_{bi} = 1.1V, N_d = 3.10^{17}\, cm^{-3}, V_{ds} = 1V,.$

For the implementation of the MOGAs, tournament selection is employed which selects each parent by choosing individuals at random, and then choosing the best individual out of that set to be a parent. Scattered crossover creates a random binary vector. It then selects the genes where the vector is unity from the first parent, and the genes where the vector is zero from the second parent, and combines the genes to form the child. An optimization process was performed for 50 population size and maximum number of generations equal to 300, for which stabilization of the fitness function was obtained. Based on the assumption that the threshold voltage and the DIBL effect are linearly correlated, suggesting that the degradation of these parameters has the same origin and perfectly controlled by the channel length. Hence, the optimization of the threshold voltage leads to the optimization of the DIBL. Therefore, the optimization of

the subthreshold electrical performances of the DM GaN-MESFETs can be reduced to four objective functions. Therefore, four objectives are considered in this study, i.e. subthreshold swing degradation coefficient ΔS, subthreshold current, threshold voltage roll-off and device parasitic resistances. So, the obtained design can provide the best subthreshold electrical performances by satisfying of the following objective functions:

- Minimization of the subthreshold current: $I_{ds-sub}(X)$
- Minimization of the subthreshold swing degradation coefficient: $\Delta S(X)$
- Minimization of the threshold voltage roll-off: $\Delta V_{th}(X)$
- Minimization of the MESFET parasitic resistance: R_{Par}.

where X represents the input normalized variables vector which is given as $X = (V_{bi1}, V_{bi2}, a, L, L_1, N_d, L_{gs}, L_{gd})$. The constraints to be satisfied are:

- $g_1(x): x \in [x_{i\,min}, x_{i\,max}]$, $x_i \in X$ (each design variable is confined within a given range)

- $g_2(x): L_1 < L$

- $g_3(x): \phi_{M1} > \phi_{M2}$

The overall objective function is obtained by given weightage based on 'weighted sum approach method' as follows:

$$F(X) = w_1.I_{ds-sub}(X) + w_2.\Delta S(X) + w_3.\Delta V_{th}(X) + w_4.R_{Par}(X) \qquad \text{(V.23)}$$

where w_i (i=1-4) are weight functions satisfy $\sum_i w_i = 1$ [130]. The choice of weighting factors is arbitrarily made by the user and it is not usually justified. Changing these weighting factors (w_i) changes the optimal solution. In our study, the subthreshold swing, subthreshold current, threshold voltage roll-off and device equivalent resistance are equally important. Hence, w_i (i=1-4) can be assigned equal values as 0.25.

Start with a randomly generated population of 'n' 1-bit chromosomes (candidate solutions to the problems):

- Calculate the overall objective function of each of the chromosome 'X' in the population.
- Create 'n' offspring from current population using the three MOGA operators namely selection, crossover and mutation.
- Replace the current population with the updated one.
- Repeat the above steps until the termination criteria is reached.

The MOGAs parameters were varied and the associated optimization error was recorded. Figure V.6 shows the variation of overall objective function as function of generation number where the minimum objective function can be reached for 15000 iterations.

The steady decrease in the subthreshold parameters of the best solution in each generation until it reaches a best possible value can be attributed to the selection procedure used namely tournament wheel selection. Final optimized DM GaN-MESFET parameters are summarized in Table V.1.

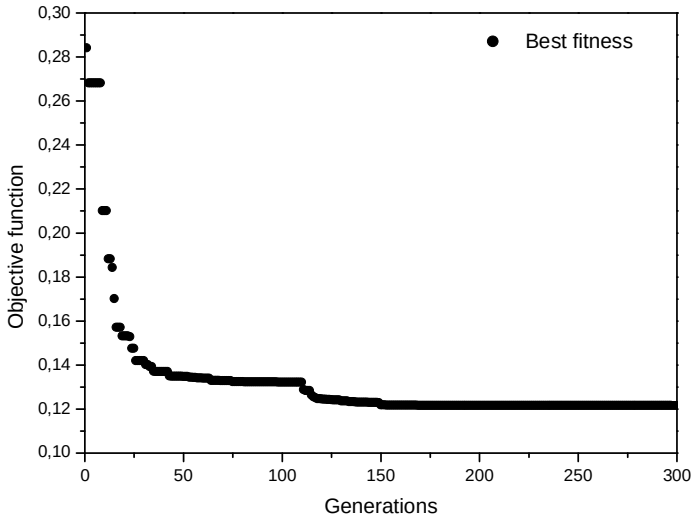


Figure V.6: Variations of normalized overall objective function with generations

Symbol	Quantity	Optimized design
Design variables:		
V_{bi1} V_{bi2}	Schottky-barrier built-in potential for both regions	1.3V 1.2V
L	Channel length	0.2µm
$L1$	Channel length for first region	0.15µm
a	Thickness for active region	0.08µm
N_d	Doping concentration in the active region	5×10^{17} cm^{-3}
L_{gs}	Source/gate spacing	0.08µm
L_{gd}	Drain/gate spacing	0.08µm
Objective functions:		
$\text{œ}V_{th}$ S $I_{ds\text{-}sub}$ R_{Par}	Threshold voltage roll-off Subthreshold swing Subthreshold current Parasitic resistance	5.3×10^{-3} V 95.35 mV/dec 1.61×10^{-11} A 873.04 Ω

Table V.1: Optimized DM GaN- MESFET Design Parameters

V.I.4 Conclusion

In this work, the concept of dual-material gate design and its 2-D subthreshold analytical model have been proposed, investigated and expected to suppress the short-channel-effects and hot carrier effect for deep submicron GaN-MESFET-based circuits. It has been shown that the incorporation of the dual-material design aspect exhibits an improvement in the screening of the channel potential variation. Moreover, the peak electric field at the drain end is reduced, minimizing the hot carrier effect. The law of scaling capability of the proposed design was compared to the conventional single-material case, illustrating the improved subthreshold behavior of the DM GaN-MESFET over conventional GaN-MESFETs. The model results have been compared with the simulation results obtained from the ATLAS device simulation software where a good agreement is observed between them. In addition, a MOGA-based approach is proposed to maximize the subthreshold electrical performances of the investigated DM GaN-MESFET. The developed algorithm has successfully searched the minimum possible of subthreshold parameters values and the input design parameters that can yield those specific values. The proposed approach would be useful for device engineer to predict the desirable characteristics of DM GaN-MESFETs before actual fabrication.

Part (II): Modeling and optimization of Saturation regime performances

V.II.1 Saturation regime

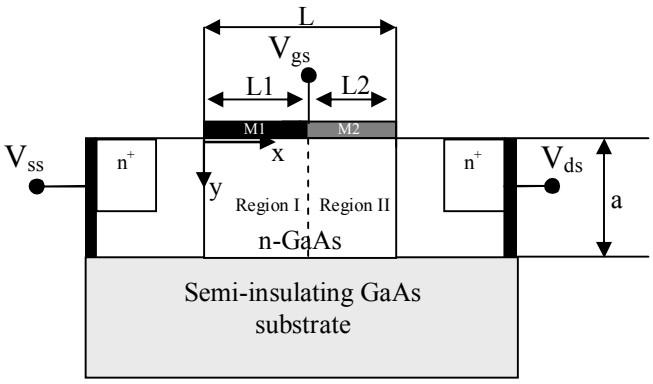
From applications and the fundamental research point of view, short channel length, submicron, GaAs-MESFETs have been focus of interest. In high-tech analog circuitry these devices are used due to their superior frequency and gain properties. However, with the reduction in channel length, control of parasitic resistances, drain current in saturation regime and the small signal parameters is one of the biggest challenges in further downscaling of the GaAs-MESFETs-based technology. Only a little works on the improvement and optimization of the GaAs-MESFETs characteristics have been reported so far in the literature. Most of the works on GaAs-MESFETs mainly deal with the modeling of 2D potential distribution, threshold voltage and empirical characteristics of the single gate devices [131–133]. The proposed (DM) GaAs-MESFET design is similar to that of a conventional single material gate (SM) GaAs-MESFET with the exception that the gate of the DM GaAs-MESFET structure consists of two materials. The first step of the proposed approach consists of accurate compact modeling of drain current, small signal parameters and parasitic resistances for submicron Dual-Material-gate (DM) GaAs-MESFET. The different compact models will be used in this work as objective functions, which are given as function of input design variables.

Design optimization, adopted in this work, is the process of finding the maximum/minimum of the channel resistances and small signal parameters called the objective functions and must also satisfy a certain set of specified requirements within constraints [130,132,133]. This work proposes a new solution technique based on MOGAs to find the set of Pareto-optimal solutions for multi-objective (DM) GaAs-MESFETs design problem. To deal with multi-objective and enable the decision maker for evaluating a greater number of alternative solutions, an analytical drain current model, comprising dual-material gate effect, is presented in order to explain the advantages provided by the DM GaAs-MESFET design, over the conventional single material gate (SM) GaAs-MESFET, and implemented in the proposed optimization procedure. Our analytical modeling and MOGA-based optimization approach demonstrate that the proposed optimization technique exhibits significantly improved

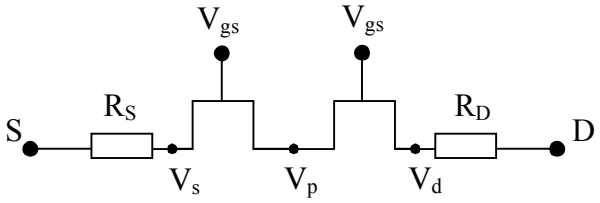
performances of the device in terms of small signal parameters and parasitic resistances which make the proposed design as a promising candidate for future GaAs-MESFET-based analog circuits. Finally, the validity of the model is shown by comparing the analytical results with the commercially available ATLAS device simulator [125].

V.II.2 Models formulation

A schematic cross section of a DM GaAs-MESFET and the definition of the geometrical and electrical characteristics are shown in Figure V.7. As shown in the figure, a is the GaAs film thickness, L is the channel length, L_1 is the length of the first region and $N_{D/S}$ represents the doping level of the drain/source region respectively. Using an equivalent circuit analogy, a DM GaAs-MESFET device can be represented as a series combination of two GaAs-MESFETs with different material-gate work functions as shown in Figure V.7b.



(a)



(b)

Figure V.7: (a) Cross-sectional view of the analyzed DM GaAs-MESFET (b) equivalent circuit representation for a drain current modeling.

In submicron GaAs-MESFETs, quite often, there is a finite density of interface states and the ideal device pinch-off is usually not observed [134]. The Schottky interfacial layer, which is a probable cause of the threshold voltage shift, is assumed to be of finite thickness that can hold potential across it and, on the other words, it is transparent enough to allow the flow of electrons [134]. Devices with interfacial layers exhibit relatively higher gate leakage and consequently the effect of gate potential to control the channel thickness is poor. The loss of finite amount of gate voltage due to the interfacial layer has not been incorporated in most models presented in literature [134]. They assumed an ideal Schottky interface of a GaAs-MESFET and as a result these models are not accurate enough to simulate Current-Voltage characteristics of a device having finite Schottky barrier interfacial layer. In this study, a comprehensive drain current model is proposed which is an extension to N.M. Memon model capable to simulate drain current behavior of Single Material Gate (SM) GaAs-MESFETs irrespective of the Schottky barrier response [134].

Based on the drain current model proposed by Memon et al for a Single Material Gate (SM) GaAs-MESFET, the analytical expression of the drain current, including the interface states effects, can be given as

$$I_{ds} = I_{dss}\left(1 - \frac{V_{eff}}{V_{th} + \Delta V_{th} + \gamma V_{ds}}\right)^2 tanh(\alpha V_{ds})(1 + \lambda V_{ds}) \qquad \text{(V.24)}$$

where I_{dss} is the saturation drain current, V_{ds} is the applied drain voltage, V_{th} represents the threshold voltage, ΔV_{th} is the threshold voltage shift caused by the interface state effects, V_{eff} represents the effective applied gate voltage given [134] by $V_{eff} = \frac{V_{gs} - V_{bi}}{1 + \eta e^{V_{gs} - V_{bi}}}$, with V_{bi} represents the schottky-barrier built-in potential, which mainly depends on material gate work function, and η represents a constant which simulates quality of schottky barrier. In Eq. (V.24) there are four fitting parameters which describe the short-channel effects on the electrical characteristics [134].

In a SM GaAs MESFET, the gate consists of only one material, but in the proposed design (DM), we have two different materials with work functions ϕ_{M1} and ϕ_{M2}, respectively. Therefore, the schottky-barrier built-in potential V_{bi} at the gate, for

each region, would be different. From the equivalent circuit in Fig.V.7, $V_{ds} = V_p + V_{dp}$ is obtained. Therefore, the drain current for each transistor can be derived using Eq. V.24 and the boundary condition which satisfies the continuity of the channel potential and the drain current at the interface of two dissimilar gate-materials of the gate. Therefore, we have:

$$I_{ds} = I_{ds1} = I_{ds2} \tag{V.25a}$$

$$I_{ds1}(V_p) = I_{dss1}\left(1 - \frac{V_{eff\,1}}{V_{th1} + \Delta V_{th1} + \gamma V_p}\right)^2 tanh(\alpha V_p)(1 + \lambda V_p) \tag{V.25b}$$

$$I_{ds2}(V_p) = I_{dss2}\left(1 - \frac{V_{eff\,2}}{V_{th2} + \Delta V_{th2} + \gamma(V_{ds} - V_p)}\right)^2 tanh(\alpha(V_{ds} - V_p))(1 + \lambda(V_{ds} - V_p)) \tag{V.25c}$$

where the threshold voltage and shift in threshold due to submicron geometry of the both devices are defined, respectively, as:

For the first region:

$$V_{th1} = \frac{qNa^2}{2\varepsilon} - \phi_{bi1} \tag{V.26a}$$

$$\Delta V_{th1} = \frac{4a}{3L_1} V_{th1} \tag{V.26b}$$

For the second region:

$$V_{th2} = \frac{qNa^2}{2\varepsilon} - \phi_{bi2} \tag{V.26a}$$

$$\Delta V_{th2} = \frac{4a}{3(L - L_1)} V_{th2} \tag{V.26b}$$

Based on the boundary conditions and the drain current expression for each region (given in (V.25)), the interfacial potential (V_p) can be calculated numerically, and therefore, a new drain current model which includes the dual-material gate aspect can be obtained.

The values of the small signal parameters (transconductance, g_m, and out conductance, g_d) are derived by differentiating I_{ds}, given in Equation (V.25), with respect to V_{gs} and V_{ds} respectively.

$$g_m = 2I_{dss1}\left[1-\frac{V_{eff\,1}}{V_{th1}+\Delta V_{th1}+\gamma V_p}\right]\times\left[\frac{V_{eff\,1}}{V_{gs}-V_{bi1}}\left(1-\eta V_{eff\,1}e^{V_{gs}-V_{bi1}}\right)\right] \times\left[\frac{-1}{V_{th1}+\Delta V_{th1}+\gamma V_p}\right]\times\left[tanh(\alpha V_p)(1+\lambda V_p)\right] \quad \text{(V.27a)}$$

$$g_d = 2I_{dss1}\left[1-\frac{V_{eff\,1}}{V_{th1}+\Delta V_{th1}+\gamma V_p}\right]\times\left[1-\frac{\gamma V_{eff\,1}}{\left(V_{th1}+\Delta V_{th1}+\gamma V_p\right)^2}\right]\times tanh(\alpha V_p)(1+\lambda V_p) + I_{dss1}\left[1-\frac{V_{eff\,1}}{V_{th1}+\Delta V_{th1}+\gamma V_p}\right]^2\times\left[1-tanh^2(\alpha V_p)\right](1+\lambda V_p) + \lambda I_{dss1}\left[1-\frac{V_{eff\,1}}{V_{th1}+\Delta V_{th1}+\gamma V_p}\right]^2\times tanh(\alpha V_p) \quad \text{(V.27b)}$$

In order to fully benefit from the expected performance of the coming technology nodes, all the parasitic components have to be reduced as much as possible. In particular, the parasitic device resistances, which are the drain resistance in series with the source one, will have to be drastically decreased as we will reduce the device length. In addition, the channel resistance can be considered as the most important parameter which affects the device power consumption. Hence, the minimisation of this parameter should be taken into account by the circuits designer.

The equivalent MESFET resistance can be represented as a series combination of two parasitic resistances and output resistance as

$$R_{eq} = R_{Par} + g_d^{-1} = R_s + R_D + g_d^{-1} \quad \text{(V.28)}$$

with $R_S = \frac{L_{gs}}{qN_dWa\mu_n}$, $R_D = \frac{L_{gd}}{qN_dWa\mu_n}$.

where R_s and R_D represent the source and drain resistances, respectively, L_{gs} and L_{ds} represent the gate-source and gate-drain lengths, respectively, and μ_n represents the low electron mobility for the GaAs material [129].

V.II.3 Results and discussion

In order to investigate the effectiveness of the proposed DM GaAs-MESFET design, the DM and SM structures are studied, compared and results are presented. Further the DM device results are compared with the simulated results of ATLAS 2D

device simulator [125]. Figure V.8 shows the calculated output characteristics for a channel length of a $0.2\times200\mu m^2$ ($L_1 = 0.1\mu m$) DM GaAs-MESFET compared with that of the conventional SM GaAs-MESFET. The device parameters for both designs, DM and SM, are: $N_d = 5\times10^{17}cm^{-3}$; $a = 0.1\mu m$; $V_{bi1} = 1.3V$; $V_{bi2} = 0.21V$. It is shown that the model calculations are in good agreement with the simulation results for a wide range of channel lengths. It can be observed that the DM GaAs-MESFET exhibits a better drain current behavior in the saturation regime. Due to the discontinuity in the channel potential of the DM GaAs-MESFET, the peak electric field at the drain is reduced substantially when compared with that of the SM GaAs-MESFET that leads to a reduced hot carrier and electron saturation velocity effects in the channel. These effects are considered as the main failure parameters which affect the device performances for analog circuits applications. The obtained results for both designs, SM and DM, show that the proposed structure offers significant improvement especially at low applied gate voltage. Therefore, as device dimensions penetrate into the submicron regime, the improved obtained performances make DM GaAs-MESFET a better choice for future submicron MESFET-based devices. Figure V.9 plots the variation of the saturation drain current, $I_{dsat,DM}$, as function of metal gate work function near the drain end, ϕ_{M2}, for a fixed $V_{gs} = 0V, V_{ds} = 6V$, $\phi_{M1} = 5.3eV$ *and* $L_1 = 0.1\mu m$. It is clear shown that as gate metal work function near the drain end increases, $I_{sat,DM}$, decreases; this is due to the increase in the threshold voltage. This also implies that higher value of ϕ_{M2} results in higher threshold voltage that is unsuitable and poses a trade off with power supply requirements.

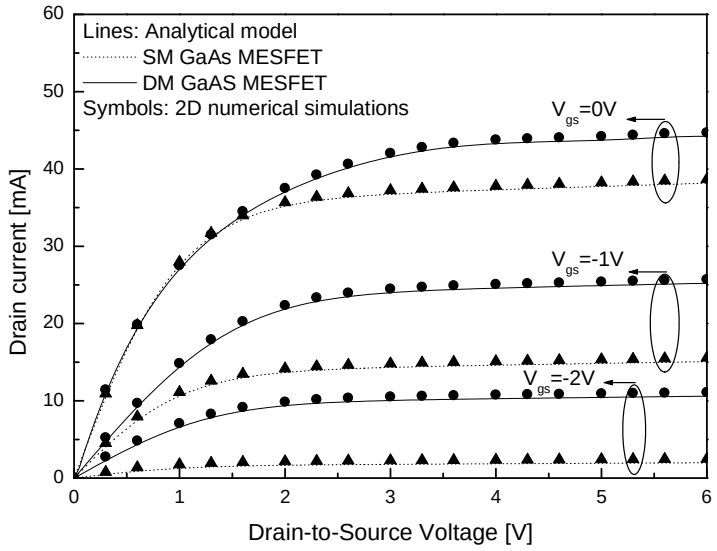


Figure V.8: Output characteristics for a channel length of a $0.2\times 200\mu m^2$ ($L_1 = 0.1\mu m$) DG GaAs-MESFET compared with that of the conventional SM GaAs-MESFET. Device parameters used for calculating are $a = 0.1\mu m, \phi_{M1} = 5.3eV, \phi_{M2} = 4.28eV, V_{bi1} = 1.3V, V_{bi2} = 0.21V$ $N_d = 5.10^{17} cm^{-3}$.

Figure V.10 (a) shows the variation of the transconductance as a function of increasing work function of the metal gate near the drain end at fixed , ϕ_{M2}, for a fixed $V_{gs} = 0V, V_{ds} = 4V$, $\phi_{M1} = 5.3eV$ *and* $L_1 = 0.1\mu m$. It is shown that as the ϕ_{M2} is increased the g_m keeps on decreasing due to a reduced gate overdrive. This effect can be explained by the effect of the increasing in the work function of the metal near the drain on the increasing of the threshold voltage. Figure V.10 (b) plots the variation of output conductance, g_d, with the increase in the work function of the gate metal near the drain end. It is clear shown that g_d is increased with the increase in ϕ_{M2}. This is due to the fact that with the increase in ϕ_{M2}, the region near the drain is screened from any variations in the drain bias. This reduces the influence of drain bias on the drain current in the saturation regime.

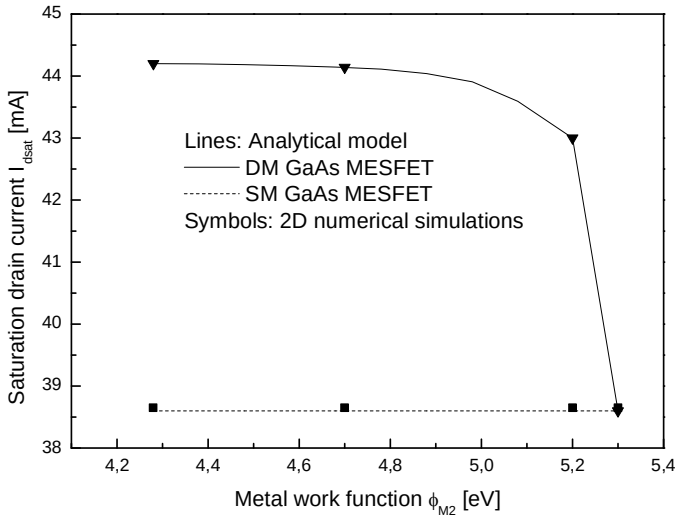
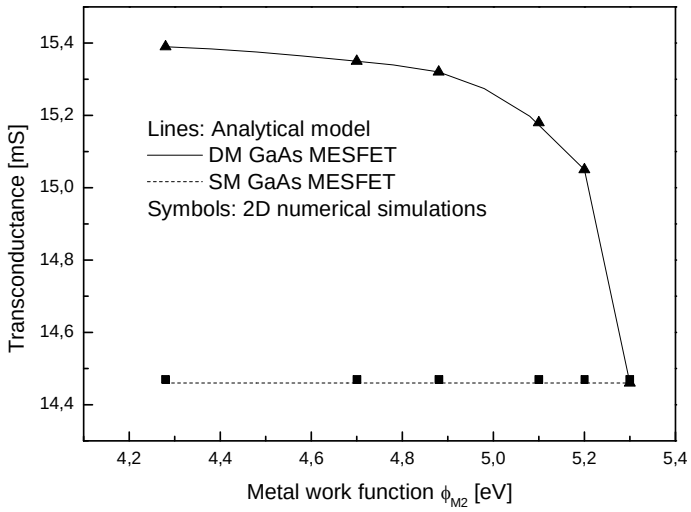
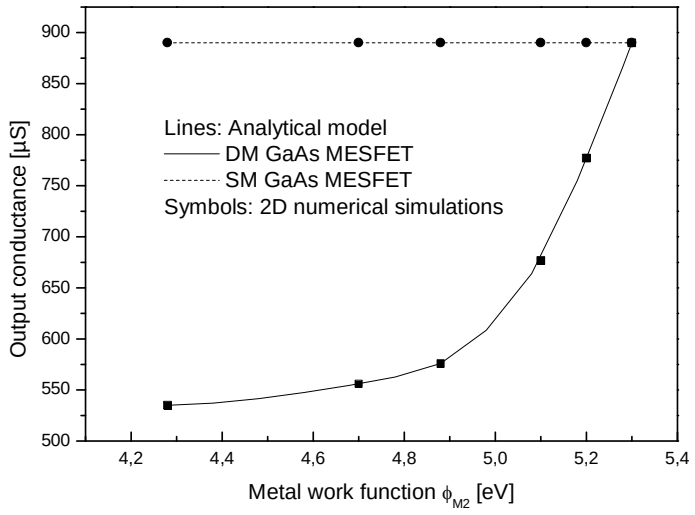


Figure V.9: variation of the saturation drain current, I_{dsat}, as function of metal gate work function near the drain end, ϕ_{M2}, for a fixed $V_{gs} = 0V, V_{ds} = 6V,\ \phi_{M1} = 5.3eV$ and $L_1 = 0.1\mu m$.



(a)



(b)

Figure V.10: (a) Variation of the transconductance as a function of increasing work function of the metal gate work function for a fixed $V_{gs} = -0.5V, V_{ds} = 4V$, $\phi_{M1} = 5.3eV$ *and* $L_1 = 0.1\mu m$. *(b) Variation of the output conductance with the increase in the work function of the gate metal near the drain end.*

V.II.3.1 MOGA s-based optimization

During the last decade, there has been a growing interest using genetic algorithm to solve and optimize a variety of single and multi-objective problems in the field of engineering [130,133,135]. Evolutionary algorithms have been shown to solve nonlinear and multivariable problems by exploring all regions of state space and exponentially exploiting promising areas through genetic operators like: selection, crossover and mutation, which will be applied to individuals in populations [130,133,135]. In this work, we proposed a new approach based on MOGAs computation to optimize the electrical performances of DM GaAs-MESFET for analog circuits applications. In our multi-objective optimization problem, multi-objective functions need to be optimized simultaneously. The proposed approach was designed to generate Pareto-optimal solutions considering the random weight approach in which weights are randomly determined for each step of evolutionary process. This approach explores the entire solution space in order to avoid local optima and thus gives a uniform chance to search all possible Pareto solutions along frontier.

For the implementation of the MOGAs, tournament selection is employed which selects each parent by choosing individuals at random, and then choosing the best

individual out of that set to be a parent. Scattered crossover creates a random binary vector. It then selects the genes where the vector is unity from the first parent, and the genes where the vector is zero from the second parent, and combines the genes to form the child. An optimization process was performed for 90 population size. Three objective functions, which affect the device analog behavior, are considered in this study, i.e. transconductance coefficient g_m, output conductance g_d and drain-to-source resistance. Therefore, the obtained design can provide the best analog electrical performances, small signal parameters and equivalent device resistance, by satisfying of the following objective functions:

– Maximization of the transconductance coefficient g_m.
– Minimization of output conductance g_d.
– Minimization of drain-to-source resistance R_{eq}.

The input normalized electrical and dimensional variables vector, which will be optimized using our approach, is given as $X = (V_{bi1}, V_{bi2}, a, L, L_1, N_d, L_{gs}, L_{gd})$.

The constraints to be satisfied are:

- $g_1(x): x \in [x_{i\,min}, x_{i\,max}]$, $x_i \in X$ (each design variable is confined within a given range).
- $g_2(x): L_1 < L$.
- $g_3(x): \phi_{M1} > \phi_{M2}$.

Figure V.11 shows the surface representing the Pareto front. Each point represents the values of the three objective functions obtained by given input design parameters. The multi-objective GA solutions clearly define the Pareto's region in which there is no dominated solution so that each proposed solution may be considered as good as the others. Three selected points are shown in this figure and the corresponding design parameters, for each point, are shown in Table V.2.

The decision maker, provided with the information on the non-dominated solutions forming the Pareto set, may firstly decide acceptable small signal parameters and/or device resistance, thus correspondingly setting the input design vector to lower the output conductance and device resistance and maximize the transconductance. From Figure V.11, it is clearly shown that the three presented possible solutions in the pareto front can be considered as an important guideline tool for the device designers. Moreover, we can notice that the first solution presents the advantage of having both the maximum transconductance and minimum output conductance, which are important

parameters for analog circuits design, and the third one has the minimum channel resistance, which is the most important parameter for reducing the device power consumption for analog circuit applications.

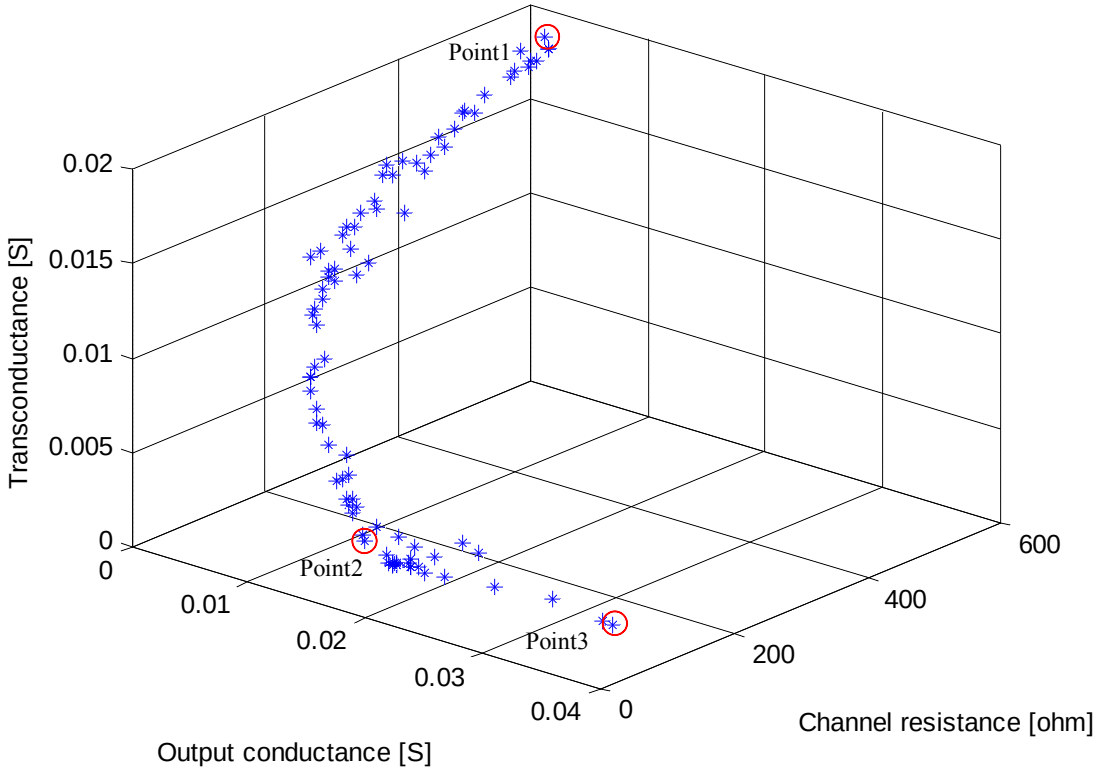


Figure V.11: Pareto-optimal solutions of the analyzed DM GaAs- MESFET

Pareto parameters			
Quantity	Point1	Point2	Point3
Schottky-barrier built-in potential for region I, V_{bi1} (V)	1.03	1.1622	1.299
Schottky-barrier built-in potential for region II, V_{bi2} (V)	0.8999	0.3431	0.3427
Channel length, L (µm)	0.2466	0.1568	0.1504
Channel length for first region, $L1$ (µm)	0.0817	0.1170	0.1199
Thickness for active region, a (µm)	0.1002	0.1193	0.1002
Doping concentration in the active region, N_d (cm^{-3})	5.311×10^{17}	6.8019×10^{17}	5.0959×10^{17}
Source/gate spacing, L_{gs} (µm)	0.0873	0.0838	0.0806
Drain/gate spacing, L_{gd} (µm)	0.0849	0.0892	0.0823
Objective functions			
Transconductance, g_m (mS)	18.8	2.4	2.8
Output conductance, g_d (mS)	0.7	16.3	39.4
Channel resistance, R (Ω)	588.3	63.92	28.89

Table V.2: Optimized DM GaAs-MESFET Design Parameters

In order to show the impact of our approach on the design of GaAs-MESFET-based circuits, we propose to investigate the analog behavior, gain and cut-off frequency, of a single DM GaAs-MESFET voltage amplifier circuit. Figure V.12 shows the voltage gain, $G_v = |g_m / g_d|$, and cut-off frequency, $f_T \approx g_m / 2\pi C_{gs}$, variations as function of the work function of the metal gate near the drain end, ϕ_{M2}, for $L_1 = L/2$. Because of an increase in the transconductance and a decrease in the output conductance, the voltage gain and of the cut-off frequency of the DM GaAs-MESFET voltage amplifier are much higher when compared with that of the SM GaAs-MESFET circuit. From Table V.3, it is observed that a great improvement in the circuit performances, the gain and the cut-off frequency, can be obtained by introducing our MOGAs-based approach in the submicron GaAs-MESFET-based circuits design.

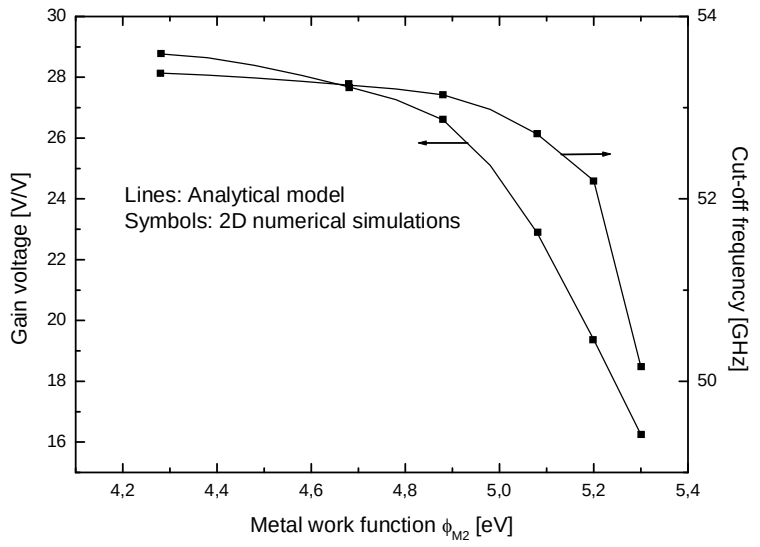


Figure V.12: variation of voltage gain and cut-off frequency as function of metal gate work function near the drain end, ϕ_{M2}, for a fixed $\phi_{M1} = 5.3eV$ and $L_1 = 0.1\mu m$.

Quantity	Optimized design Dual material (Point1)	Single material
Schottky-barrier built-in potential for region I, V_{bi1} (V)	1.03	1.3
Schottky-barrier built-in potential for region II, V_{bi2} (V)	0.8999	---
Channel length, L (µm)	0.2466	0.25
Channel length for first region, $L1$ (µm)	0.0817	---
Thickness for active region, a (µm)	0.1002	0.1
Doping concentration in the active region, N_d (cm^{-3})	5.311×10^{17}	5×10^{17}
Source/gate spacing, L_{gs} (µm)	0.0873	0.08
Drain/gate spacing, L_{gd} (µm)	0.0849	0.08
Gain voltage, G (V/V)	26.85	9.52
Cut-off frequency, f_T (GHz)	53	50.28

Table V.3: Comparison between the optimized DM GaAs-MESFET voltage amplifier design parameters and SM GaAs-MESFET.

V.II.4 Conclusion

In this work, the concept of Dual-Material Gate has been applied to the GaAs-MESFET structure and the features exhibited by the resulting new device have been investigated and analyzed by developing new analytical models, which describe the device behavior for analog applications. It has been demonstrated that Dual-Material Gate design offers superior characteristics in terms of drain current and transconductance enhancement and reduced output conductance. Moreover, new MOGAs-based approach is proposed to optimize the electrical performances of DM GaAs-MESFET for submicron MESFET-based analog circuits design. The proposed approach has successfully searched the best possible transistor performances and the input design parameters that can yield those specific performances. It is to note that our approach can be extended by including other parameters like: parasitic capacitances and pinch-off value. This MOGAs-based design approach not only benefits the modeling and optimization of GaAs-MESFETs but also can be extended for other real world applications. The similar methodology can be used to study the sensor devices and high electrons mobility transistors (HEMTs).

Conclusions and future work

The emerging technologies such as carbon nanotubes, graphene, and spintronics have stirred up considerable scientific interest, but will unlikely be incorporated into the future digital ICs because they lack the scaling and integration capabilities and infrastructure necessary to viably contend for cost effective IC manufacturing. The only promising solution is III-V based FETs, in forms of MOSFETs or MESFETs, due to the extensive materials, device processing, heterostructure, band gap engineering and integration technologies acquired in the past 45 years. However, despite the established infrastructures and the widespread usage of III-V devices in wireless communications and optoelectronics, some fundamental problems with scaling of low-power III-V based FETs remain to be resolved, specifically in the development of high quality and robust dielectric/semiconductor interface with very low interface trap density.

The promising recent results of III-V-based FETs developed at various institutions and laboratories provide a roadmap toward future high-speed low-power logic digital ICs with better performance than Si based FETs of the same gate length. Other important parameters that need to be improved are the enhancement of I_{ON}/I_{OFF} ratio by including new gate and high-k dielectrics on the III-V surface with a low interface trap density, and heterogeneous integration of III-V FETs on Si substrates.

In this thesis, an extensive work is carried out in the field of III-V MESFETs modeling. For the first time, it covers the modeling of subthreshold performance for deep submicron DG GaN MESFET where an analytical analysis was developed, investigated and expected to improve the subthreshold behaviour for deep submicron MESFET-based circuits. It also describes a 2-D numerical analysis of GAA GaN MESFET design in order to improve the subthreshold behaviour. It has been shown that the incorporation of the multigate design aspect exhibits an improvement in the screening of the channel potential variation, and an enhancement of the short-channel-effects. The results found of the proposed structures were compared to the conventional single-gate case, illustrating the improved subthreshold behavior of the DG and the GAA GaN-MESFET over the conventional GaN-MESFETs. On the other hand, the concept of dual-material gate III-V MESFET design has been proposed, investigated

and expected to improve the SCEs and the scaling capability of the device for the future high speed digital and analog circuit applications. In addition, a multi-objective genetic algorithms optimization (MOGAs) approaches are proposed to optimize the proposed designs in term of subthreshold and analog performances for high speed submicron digital applications and to search for optimal electrical and dimensional parameters to obtain better electrical performance of the device for analog and digital circuit applications. The obtained results from our analytical investigation have been compared to the 2D numerical simulations using SILVACO simulator tool, where a very good agreement is observed. The obtained results make the proposed designs promising candidates for future integrated III-V-based devices.

The project could be extended by further improvements of both subthreshold regime and electrical behavior in saturation regime when a device continues downscaling from submicron to deep submicron domain by developing new mathematics tools which include other effects such as dynamical bulk and interface traps, and quantum transport effects. Also, as new materials are being used for fabrication of FET-based devices and can provide an enhancement in performances; further work could be done by simulating FETs with new materials such as graphene. However, graphene-FETs can possibly supplement or replace current FET-based devices. These new devices can provide new transistor generations with very high speed commutations and low power consumption.

The investigation of the performance of III-V materials leads to study other optical devices such as III-V-based solar cells, which can produce better performance and efficiency over the conventional solar cells.

The evolutionary technique MOGAs presented in this work can offer possibilities for determining quantitative information on optimized designs. However, future research can investigate the use of a PSO and quantum PSO-multi-objective approach, which may produce better results for more complex systems.

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