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Entitled:

Contribution to the modeling and improvement of the nanoscale multigate transistors: Application to the nanoscale circuits design

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Thèse

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Par

Toufik BENDIB

Thème:

Contribution à la modélisation et amélioration des transistors à grilles multiple: Application à la conception des circuits nanométriques

Devant le jury:

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بسم الله الرحمن الرحيم

DEDICATION

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The text of Chapter 4, in part, is a reprint of the material as it appears in "Electrical performance optimization of nanoscale double-gate MOSFETs using multiobjective genetic algorithms" by T. Bendib and F. Djeffal, IEEE Transactions on Electron Devices, 2011. The dissertation author was the primary investigator and author of this paper.

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The text of Chapter 5, in part, is a reprint of the material as it appears in "Subthreshold behavior optimization of nanoscale graded channel gate stack double gate (GCGSDG) MOSFET using multi-objective genetic algorithms" by T. Bendib, F. Djeffal, and D. Arar, Journal of computational electronics, Springer, 2011. The dissertation author was the primary investigator and author of this paper.

The text of Chapter 5, in part, is a reprint of the material as it appears in "An optimized junctionless GAA MOSFET design based on multiobjective computation for high-performance ultra-low power devices" by T. Bendib, F. Djeffal, and M. Meguellati, Journal of Semiconductors, IOP Publishing, 2014. The dissertation author was the primary investigator and author of this paper.

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ABSTRACT OF THE DISSERTATION

Contribution to the modeling and improvement of the nanoscale multigate transistors: Application to the nanoscale circuits design

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As bulk CMOS scaling is approaching the limit that is imposed by gate-tunneling leakage current, dopant fluctuation, band-to-band tunneling, etc., multi-gate MOSFET is becoming an intense subject of very large-scale integration (VLSI) research.Among a variety of non-classical MOSFETs, multiple-gate (MG) MOSFETs which are still based on Si have been proposed to scale down CMOS technology more aggressively because of better control of short-channel effects (SCEs).

This dissertation focuses on the design optimization and modeling of these categories of multiple-gate (MG) MOSFETs to improve device performances for nanoscale circuits design applications.

In this dissertation, we will first introduce the complete analytic models of drain current by assuming gradual channel approximation(GCA) to derive the Current-Voltage(I-V) characteristic of short channel Double Gate (DG) MOSFET with intrinsic silicon body using the effective electric field-charge density relationship. Thus, the mobility degradation effect

which mainly depend on the inversion charge distribution in the channel is incorporated in the model at high electric field. Moreover, the developed models should be able, including quantum effect (QE), to correctly represent the I-V characteristics of the nanoscale DG MOSFET, and effectively capture the electrical behavior of the device due to process variations. The proposed I-V model is continuously valid from the subthreshold to the quasi-linear regime operation and up to a well-defined drain saturation voltage and agrees with 2D Silvaco and nanoMOS2.5 numerical simulations. In addition, the proposed models have several advantages such as accuracy, simplicity and applicability for device with a wide range of dimension.

This work used a new soft computing approach, multiobjective genetic algorithm(MOGA), which allows investigation and simulation of the nanoscale (multigate) CMOS-based devices. The effects of device design parameters like silicon channel thickness, gate oxide thickness, and silicon channel length are studied and the output electrical parameters of the device such as OFF-sate current and subthreshold swing factor, threshold voltage rool-off, DIBL and small signal parameters are analyzed for a wide range of electrical and geometrical parameters. The key idea of the proposed approach is to optimize the electrical behavior of the DG MOSFET for subthreshold and saturation regime by satisfying of the following objective functions: Minimization of the OFF-current state:IOFF, Minimization of the subthreshold swing degradation coefficient, Minimization of the threshold voltage roll-off, Maximization of the transconductance function and Minimization of the output conductance function. The obtained results provide to the circuit designers several optimal solutions to choose the one that suites best his analog and/or digital application. The adopted designs can be exported to meet the targets for analog and digital applications simultaneously.

This work also develops subthreshold models for nanoscale multiple-gate MOSFET based on surface potential formalism. The analytical solutions of electrostatic potential and subthreshold current are validated by their agreement with 2D numerical simulation. These models allow the subthreshold swing, OFF-state current and scaling length to be formulated as objective functions, which are the pre-requisite of MOGA application.

This approach is applied to find optimal subthreshold parameters where superior electrical performances in subthreshold regime are provided by the proposed devices and offers ultra-low power consuming and high-speed commutation required for analog and digital application respectively. Moreover, in this work we deal with a new structure of MG transistors, which is the JLGAA MOSFET. This latter is considered as straightforward designs to eliminate some technological limitations for nanoscale applications, such as ultra-abrupt junctions, low cost fabrication.

Keywords: Nanoscale, Multigate, Quantum, Short channel, Analog, Digital, Optimization, Modeling, Soft computing, Genetic algorithm.

ملخص

على الرغم من بلوغ المركبات الالكترونية البعد الحدي الذي تفرضه كل من زيادة التيار الكهربائي النفقي ، التغير في الاشابة و التنقل عبر النفق بين نطاقي المخطط الطاقوي للمركب الالكتروني. في هذا السياق، تعتبر المركبات الالكترونية متعددة البوابات موضوع بحث مهم في مجال تصنيع المركبات الالكترونية النانومترية. هذا النوع من المركبات يساهم بشكل كبير في تطوير تكنولوجيا الالكترونيات الدقيقة بسبب تحسينها لخصائص القنوات القصيرة.

هذه الرسالة ترتكز أساسا على النمذجة التحليلية و اقتراح تصاميم جديدة أمثلية لهذا النوع من المركبات الالكترونية لتحسين الخصائص الكهربائية من أجل تطبيقات الدارة الالكترونية النانومترية.

في هذه الرسالة ، نقترح أولا النموذج التحليلي الكامل للتيار اعتمادا على فرضية تقريب القناة التدريجي لحساب الخاصية تيار-جهد للمركب الالكتروني النانومتري باستعمال العلاقة التي تربط الحقل الكهربائي بكثافة الشحنات. كذلك، تأثير التناقص لحركية الشحنات في القناة بفعل الحقل الكهربائي الشديد قد تم ادخاله في النموذج الرياضي من أجل تحسين فعالية هذا الأخير. النماذج التحليلية المطورة في هذه الرسالة يمكن لها أن تأخذ بعين الاعتبار التأثير الكمي و تسمح لنا بالعرض الصحيح للخصائص الكهربائية للمركب الالكتروني في المنطقة تحت الحدية، المنطقة الخطية و منطقة التشبع. من المهم الاشارة على أن النماذج التحليلية تم اقرارها بالتطابق مع النتائج الرقمية المحصل عليها باستعمال أنظمة المحاكاة التجارية (النانوموس2.5 و سيلفاكو). ومن أهم مزايا هذه النماذج المطورة، الدقة، سهولة التطبيق في مجال واسع النطاق.

في هذا العمل، استعملنا تقنية جديدة للحساب الذكي و هي الخوارزمية الجينية متعددة الأهداف التي تسمح بدراسة و محاكاة المركبات الالكترونية النانومترية متعددة البوابات. تأثير أبعاد هذه المركبات على خاصياتها الكهربائية تم دراستها بشكل دقيق. النماذج التحليلية المطورة في هذه الرسالة تم استعمالها كمداخل للخوارزمية الجينية متعددة الأهداف من أجل تحسين خصائص المركبات الالكترونية في كلتا المنطقتين تحت الحدية و منطقة التشبع في الوقت نفسه.

بالاضافة الى المساهمات المدرجة في هذه الرسالة، تطوير النماذج الرياضية للمركبات الالكترونية النانومترية متعددة البوابات في المنطقة تحت الحدية، حيث أنه تم التحقق من صحتها بمطابقة النتائج المحصل عليها مع النتائج الرقمية. هذه النماذج استعملت كمداخل للخوارزمية الجينية متعددة الأهداف من أجل الخروج بالخاصيات تحت حدية الأمثلية للمركبات الالكترونية النانومترية من أجل تقليل استهلاك الطاقة وتحسين سرعة التبديل المطلوبة في تطبيقات الدارة الالكترونية التشابهية و الرقمية.

في هذا العمل، تعاملنا مع نوع جديد للمركبات الالكترونية متعددة البوابات و هو مقحل ذو بوابة محيطية بدون وصلة، شكله البسيط يساهم في تجاوز القيود التكنولوجية للمركبات الالكترونية النانومترية و يسمح بتصنيعها بكلفة منخفضة.

Résumé

Comme la réduction des dispositif CMOS approche la limite qui est imposé par le courant de fuite de grille dû à l'effet de tunnel, la variation du dopant et l'effet tunnel bande à bande, etc..., MOSFET à grilles multiple devient un axe très intense de recherche de l'intégration à grande échelle (VLSI). Parmi une variété de MOSFET non-classiques, MOSFET à grilles multiple (MG) à base de Si ont été proposées pour réduire agressivement la technologie CMOS grâce à un meilleur contrôl des effets de canaux courts (SCEs). Cette thèse est consacré à l'optimisation et la modélisation de ces catégories MOSFETs à grilles multiple pour améliorer les performances des dispositifs pour la conception des circuits à l'échelle nanométrique.

Dans cette thèse, en premier lieu, on va introduire le modèle analytique du courant de drain en tenant en compte l'approximation du canal gradué (GCA) pour obtenir la caractéristique courant-tension (I-V) du transistor Double Gate (DG) MOSFET à canal court pour le cas d'un substrat de silicium intrinsèque. Ce modèle utilise la relation entre le champ électrique et la densité de charge et inclut l'effet de la dégradation de la mobilité, qui dépends de la distribution de la charge d'inversion, dans le modèle pour les champs électriques élevés. En outre, le modèle développé devrait êtres capable de représenter la caractéristique I-V correctement du transistor DG MOSFET à canal court en tenant compte les effets quantiques(QE), et de capturer avec éfficacité le comportement électrique du dispositif en prenant en compte les effets du processus de conception. Le modèle I-V proposé est en accord avec les simulations numériques (2D Silvaco et nanoMOS2.5) et valide pour tous les régimes de fonctionnement (sous le seuil, le régime quasi-linéaire et le régime de saturation). En plus, les modèles développés sont simples, précis, est adéquats pour de larges gammes de géométrie.

Ce travail a utilisé une nouvelle méthode de calcul intelligent (SC), algorithme génétique multi-objectifs (MOGA), qui permet l'étude et la simulation des dispositifs MG à l'échelle nanométrique. L' effets des paramètres de conception du dispositif, comme l'épaisseur du

canal de silicium, l'épaisseur d'oxyde de grille et la longueur du canal de silicium sont étudiées où les paramètres électriques qui représentent la sortie du dispositif, tels que le courant de fuite OFF-current, l'inverse de la pente sous seuil, la tension de seuil rool-off, DIBL et les paramètres petits signaux sont analysés pour une large gamme de paramètres électriques et géométriques.

L'idée clé de l'approche proposée est d'optimiser le comportement électrique du transistor DG MOSFET dans le régime sous-seuil et le régime de saturation simultanément en satisfaisant les fonctions objectifs suivantes: minimisation de OFF-current, minimisation de la dégradation de l'inverse de la pente sous seuil, minimisation de la tension de seuil roll-off, maximisation de la fonction "transconductance" et la minimisation de la fonction "output-conductance".

Ce travail développe aussi des modèles sous-seuils des MG MOSFET à l'échelle nanométrique en se basant sur l'analyse du potentiel de surface électrostatique. Les solutions analytiques du potentiel électrostatique et du courant sous seuil sont validées par leur accord avec la simulation numérique 2D. Ces modèles permettent : l'inverse de la pente sous seuil, OFF-current et le paramètre de la réduction du canal pour être formulés comme des fonctions objectifs, qui représentent le pré-requis du MOGA.

Cette approche est appliquée afin de trouver les paramètres sous-seuils optimaux qui fournissent des performances électriques supérieures dans le régime sous-seuil et offrent une faible consommation de puissance et une haute vitesse de commutation qui sont nécessaires pour les applications analogiques et numériques respectivement. En plus, dans ce travail, on traite une nouvelle structure de transistors à grilles multiples: le transistor à grille enrobée sans jonction JLGAA MOSFET, qui est considéré comme une simple conception des transistors MOSFETs. Ce dernier permet d'éliminer certaines limitations imposées par la technologie nanométrique, telles que les jonctions ultra-brutales et le cout de fabrication.

Mots-clés: Échelle nanométrique, Grilles Multiples, Quantique, Canal court, Analogique, Numérique, Optimisation, Modélisation, calucul intelligent, Algorithme génétique.

Chapter 1

Introduction and Dissertation Overview

Contents

1.1 Introduction to CMOS scaling

Although the original idea of field effect transistor (FET) was patented as early as 1930 by Lilenfeld [1]. The first metal-oxide-semiconductor field-effect transistor (MOSFET) on silicon substrate using SiO_2 as the gate insulator was fabricated by Khang and Atalla in 1960 [2]. After 3 years ago, the CMOS (complementary MOS) is invented by Wanlass and Sah [3], then integrated-circuits (ICs) have gone from having few transistors to hundreds of millions of transistors [4]. The scale down of CMOS device dimension in conventional bulk silicon CMOS technology has been a primary driver over the past three decades in order to attain continued improvement in ICs performance, reduction in size, higher compactness, lower cost, higher circuit speed, lower power dissipation, and better functionality. CMOS is considered as the crucial material base in the evolutionary progress leading to the powerful and versatile electronic systems such as computers and communication devices. The industry's ability to exponentially reduce the minimum feature sizes used to fabricate the integrated circuits ICS, has resulted exponential growth in the number of transistors and memory bits per chip popularly known as Moore's law [5], which describes the evolution of transistor density in integrated circuits [6–11]. It affirms that the number of transistors per chip will quadruple every three years or double every 18 months [12] as shown in Figure 1.1.

Figure 1.2 illustrates the scaling concept of silicon technology, in which the device dimensions and device voltages are scaled down and the doping concentration is scaled up by the same factor [13]. Then, according to basic electrostatics, the electric field configuration will be the same as the original device. A larger FET can then be scaled down to a smaller FET with similar behavior.

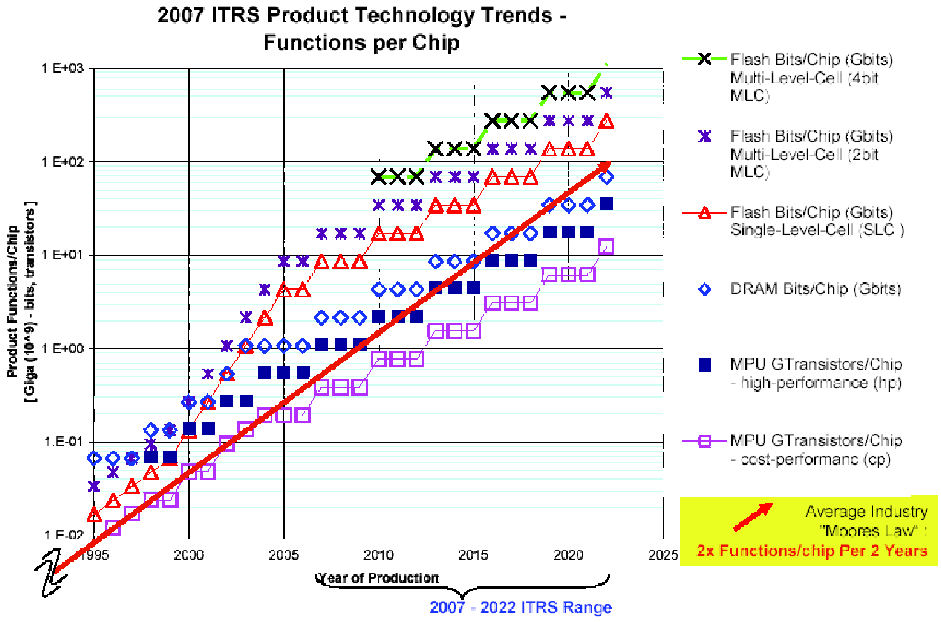


Figure 1.1: 2007 ITRS product technology trends: product functions/chip and industry average "Moore's Law" trends.

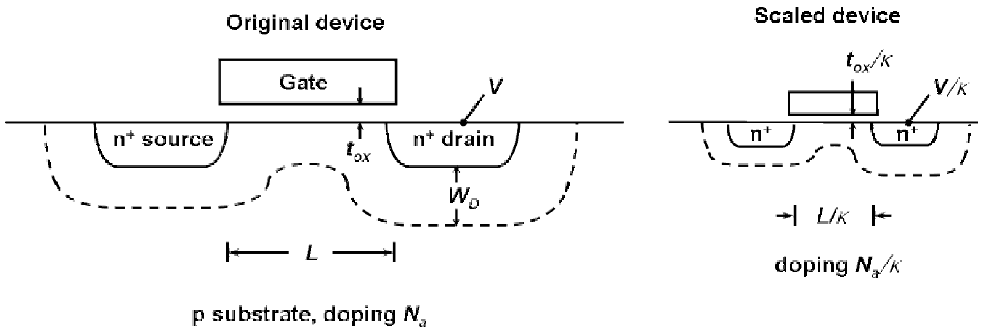


Figure 1.2: Scaling principle of silicon technology.

Table 1.1 shows the scaling rules for MOSFET devices and circuit parameters. It is shown that these scaling rules only give us a guideline to shrink down a device. They do not tell us how small we can make the devices [13]. For a given supply voltage and a given layer thickness, as the channel length decreases, the MOSFET current increases, and the intrinsic capacitance decreases. Therefore, the MOSFET switching speed is improved. However, the device channel length cannot be arbitrarily reduced because of short channel effects (SCEs) such as threshold voltage rolloff, subthreshold slope degradation and strong

drain induced barrier lowering (DIBL) effect.

Besides the scaling limit of channel length imposed by SCEs, there are other scaling limits imposed by the reduction of the vertical thickness of MOSFETs, the gate oxide thickness, which offers better control of the gate over the channel, improves the short-channel behavior and enhances the driving capability of MOSFETs. However, ultrathin gate oxide will lead to high gate leakage current due to direct tunneling. Details of those limits have been summarized in [14]. There are various approaches to avoid those scaling limits: continue scaling down the MOSFET without changing the oxide thickness; change the device structure such that the devices can be scaled further down while the short channel effect is still under control; change the gate insulator material with higher permittivity (high-K) instead of SiO_2 to increase the physical thickness while maintaining the same effective-oxide-thickness [14, 15]. In addition, the increase of random dopant fluctuation with shrinking device size affect the threshold voltage variation from device to device. These effects lead to unacceptable high leakage current and constitute the limiting factors of CMOS scaling at present [16].

Table 1.1: Scaling rules for MOSFET devices and circuit parameters

Physical parameter	Constant electric field scaling factor	Generalized scaling factor	Generalized selective scaling factor
Channel length, Insulator thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Wiring width, channel width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric field in device	1	ε	ε
Voltage	$1/\alpha$	ε/α	ε/α_d
On-current per device	$1/\alpha$	ε/α	ε/α_w
Doping	α	$\varepsilon\alpha$	$\varepsilon\alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^2$
capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate delay	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Power dissipation	$1/\alpha^2$	ε^2/α^2	$\varepsilon^2/\alpha_d\alpha_w$
Power density	1	ε^2	$\varepsilon^2\alpha_w/\alpha_d$

In table 1.1, α represents the dimensional parameter, ε is the electric field scaling prameter, α_d and α_w are separate dimensional scaling parameters for the selective scaling case. α_d is applied to the device vertical dimensions and gate length, α_w applies to the device width and the wiring.

To solve these scaling issues, two different paths can be followed. The introduction of new technologies and new materials into the conventional planar bulk MOSFET can be used as first path to allow further scaling and improve the performance of scaled transistors. Moreover, the adoption of new transistor architectures such as ultra-thin body FETs and multi-gate FETs to allow superior electrostatic control over the inversion channel. In order to study the circuit level benefits and reliability of these two CMOS scaling solutions, suitable understanding and modeling of the associated device physics and device behavior is needed.

1.2 Multi-Gate MOSFETs for Nano-Scaled ICs

As mentioned in section 1.1, CMOS has been scaled into the deep sub-100 nm regime [17,18], and is thought to be the dominant technology in the near future. As presented in Figure 1.3 , the physical gate length is estimated to be at least at or below 10 nm according to the 22-nm technology node [19]. However, CMOS scaling seems to be fundamentally limited due to several non-ideal effects which must be taken into account in nanoscale devices [14, 20, 21]. They are mainly well-known as,

- Short-channel effects including threshold voltage roll-off, drain-induced barrier lowering (DIBL), and subthreshold slope degradation
- Quantum mechanical effects leading to significant gate-tunneling leakage current, threshold voltage shift and gate capacitance degradation
- Random dopant fluctuation resulting threshold voltage variation
- Non-negligible parasitic components.

These effects lead to unacceptably high Off-current and degraded switching speed(swing factor and DIBL), therefore become limiting factors of further CMOS scaling at present [16].

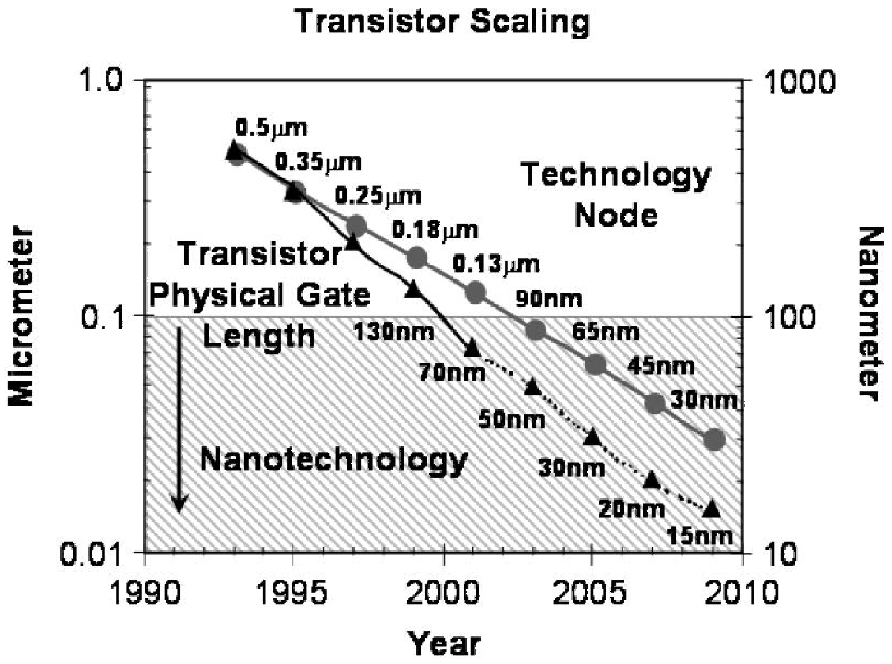


Figure 1.3: Scaling of transistor size (physical gate length) with technology node to sustain Moore's Law".

1.2.1 Multi-Gate MOSFETs: Structures and advantages

As a solution to overcome these undesirable effects, new FET architecture the Multi-gate (MG) FET has been proposed and investigated [22], including double-gate (DG), quadruple-gate, surrounding-gate (SG) [23], tri-gate [24], Pi-gate [25], Omega-gate [26] MOSFETs and FinFETs [27]. Different Multi-Gate MOSFET structures are shown in Figure 1.4, adopted from [25].

Besides the advantages of electrostatic integrity, MG MOSFETs also have some other potential promises. In MG MOSFETs, the SCEs are more controlled by the dimensions of silicon and oxide films in which the subthreshold slope (SS) degradation is not very noticeable where it is well known that the ideal SS by ignoring short-channel degradation is 60mV/Decade [28].

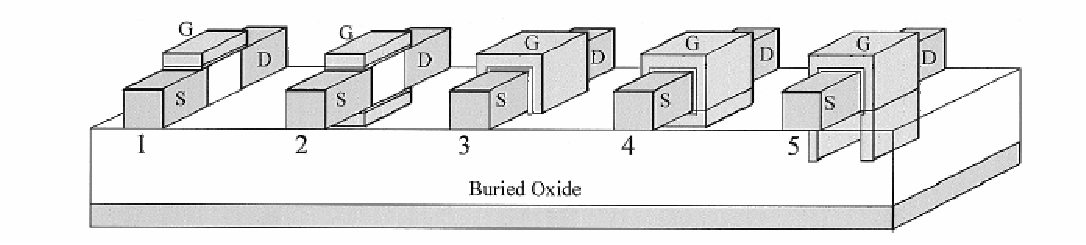


Figure 1.4: Ultra Thin Body (UTB) Silicon On Insolator (SOI) and Different Multi-Gate MOSFET Structures. (1:UTB SG SOI; 2:DG; 3:Tri-Gate; 4: Quadruple-Gate; 5:Ω-Gate).

In MG MOSFETs, as the silicon film is usually undoped or lightly doped, the mobility is better than bulk or Partially Depleted (PD)SOI MOSFETs because of the absence of strong impurity scattering, thus the threshold voltage variation caused by the dopant fluctuation will also be suppressed in MG MOSFETs. Moreover, MG-FETs can be considred as an extension to the ultra-thin (UT) body FETs or the fully-depleted (FD) SOI FETs but with more gates around the thin silicon body, where MG-FETs offer stronger electrostatic control of the inversion channel through the use of multiple gates. The channel length can be reduced to 5 times the film thickness without causing serious SCEs. Therefore, UTB-SOI with intrinsic channel and MG structures are regarded as the most promising by most research groups [23, 29, 30].

For instance, The gate controllability of the DG MOSFET is improved by both gates since the silicon film is fully depleted. In addition, The electric field lines from the source to the drain is blocked by the bottom gate electrode and therefore cannot reach the channel, thus the channel length can then be reduced to $2 \sim 3$ times the film thickness in the DG configuration.

Although, it is easy to be scaled down the DG MOSFET, but it is more difficult to fabricate a gate under single crystal channel. As an example, Selective Epitaxial with Lateral Over-growth (SELO) is a pattern for planar DG fabrication [31]. Another example is the Gate-All-Around (GAA) MOSFET fabricated in [32] and [33].

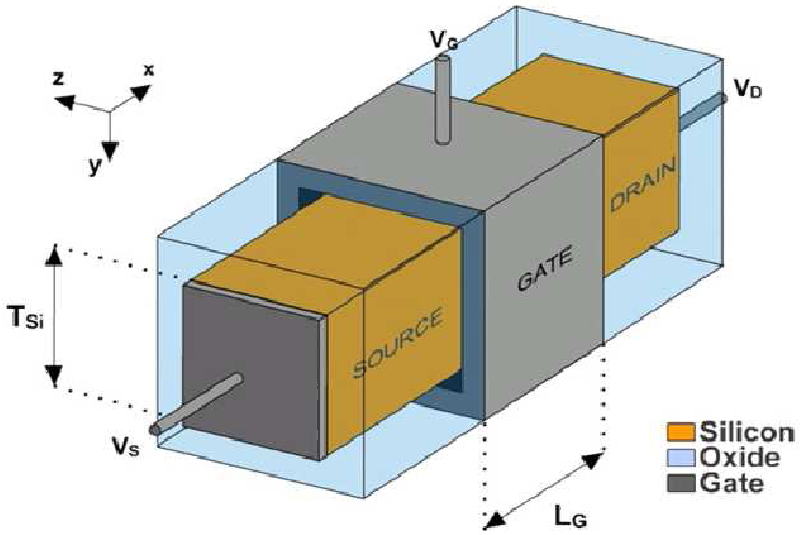


Figure 1.5: Three-dimensional schematic diagram of a QG MOSFET.

GAA MOSFET can provide the best controllability of SCEs which is usually fabricated using a Si nanowire structure, which is sometimes called nanowire transistor. Nanowire transistors have generated much research interest lately [34, 35], highlighting two types of geometry: one has rectangular (or square) shape, and is usually named quadruple-gate (QG) MOSFET; the other has circular shape, and is always called surrounding-gate (SG) MOSFET or Gate-All-Around (GAA). A 3-D schematic diagram of a QG MOSFET is illustrated in Figure 1.5 adopted from [36], whereas a typical cross sectional TEM photo for SG MOSFET is shown in Figure 1.6, adopted from [37].

Vertical DG MOSFET (Fin-FET) has also been fabricated by many research groups [38, 39]. The Fin-FET process easily provides two self-aligned gates, but this process requires a thinner fin with a width smaller than half of the gate length. Since the gate length is normally the smallest dimension in conventional MOSFET technology, the Fin-FET process has to acquire more expensive lithography equipments, thus it needs some special technologies to fabricate the silicon fin stably without lithography.

Tri-gate MOSFETs were proposed to solve this drawback [40]. Tri-gate MOSFETs use three gates coupling instead two gates coupling as in the DG MOSFET, hence they could overcome the tough fin width requirement. In addition, Tri-gate MOSFETs have

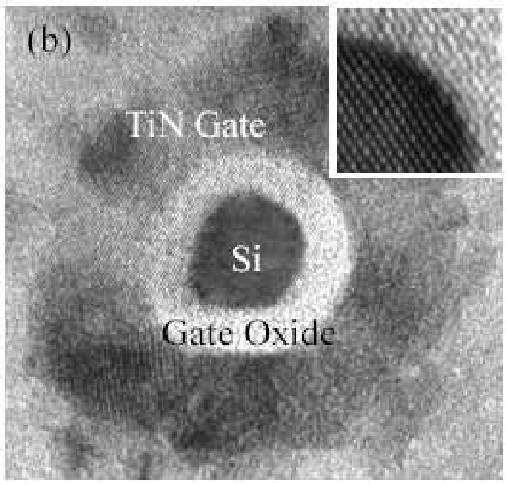


Figure 1.6: Cross sectional TEM photo of a typical SG MOSFET (circular nanowire transistor).

better characteristics than DG MOSFETs in terms of control of SCEs where the Fin width can be adjusted to be equal to the gate length in 30nm Tri-Gate MOSFET without causing serious SCEs [24]. However, Tri-gate MOSFETs suffer more from quantum-mechanical effects due to 2-D quantum confinement. Π-gate and Ω-gate MOSFETs are simple variations of TG MOSFETs. They can be classified into triple-plus-gate (TPG) MOSFETs because these devices are basically TG devices with an extension of the gate electrode below the active Si island, which increases current drive and can effectively improve the SCEs since the bottom channel is the bottleneck. The schematic diagram for Π-gate and Ω-gate MOSFET cross-sections is shown in Figure 1.7, adopted from [41].

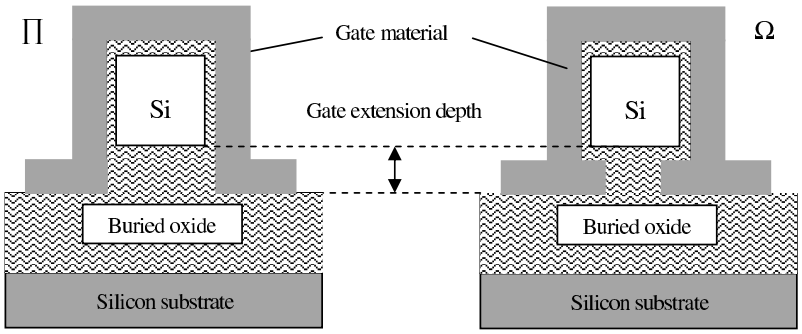


Figure 1.7: Schematic diagram of Π-gate and Ω-gate MOSFET cross-sections.

As discussed above, there is a clear lack of consensus as to which device approach would be the better design approach and therefore a potential candidate for replacing the conventional planar MOSFET. Each of the four multi-gate devices appears to offer some improvement in performance to the planar MOSFET. Each device however also remains to be optimized. The FinFET, for example, could be possibly tuned to outperform the TriGate device. In that case, the ease in fabrication offered by the TriGate transistor could then be offset by the performance advantage offered by the FinFET. On the other hand, given a certain fabrication technology and associated design rules, the TriGate transistor approach could result as the only viable alternative, possibly making the FinFET option impractical.

If the Ω-gate's fabrication is further perfected, it could offer a superior performance to the FinFET and TriGate MOSFETs. These arguments although speculative, hint at the uncertainties pending in the MG SOI device arena. What would be useful is a clear and systematic experimental study to investigate the behavior of the MG devices in greater detail and understand their performance limitations in the light of design tolerances. Considering the difficulty and the costs involved in undergoing such a thorough experimental investigation, a common simulation study comparing these devices would be desirable. Due to the dimensional nature of these devices in comparison with the conventional MOSFET, two and three-dimensional fabrication process and device simulations are needed to perform this comparison.

1.2.2 Double-Gate MOSFETs: Structures and Advantages

The most intensively studied MG MOSFETs are DG MOSFETs [42, 43]. The possible orientations of DG MOSFET on a silicon wafer are shown in Figures 1.8(a), 1.8(b), 1.8(c), adopted from [44]. The planar DG (Figure 1.8(a)) resembles the planar bulk MOSFET technology. It has less geometry effects such as "Corner effects" [45] and "Narrow width effects" [46]. In addition, the planar DG is free from "crystal plain orientation uncertainty" problems when directions of the devices vary. Another advantage of planar DG

MOSFET, is that the two gates are easy to be separately biased as the two gates are formed in different process steps. In fact, these above mentioned advantages are a great reason to study DG physical properties and improve their electrical performances for such application.

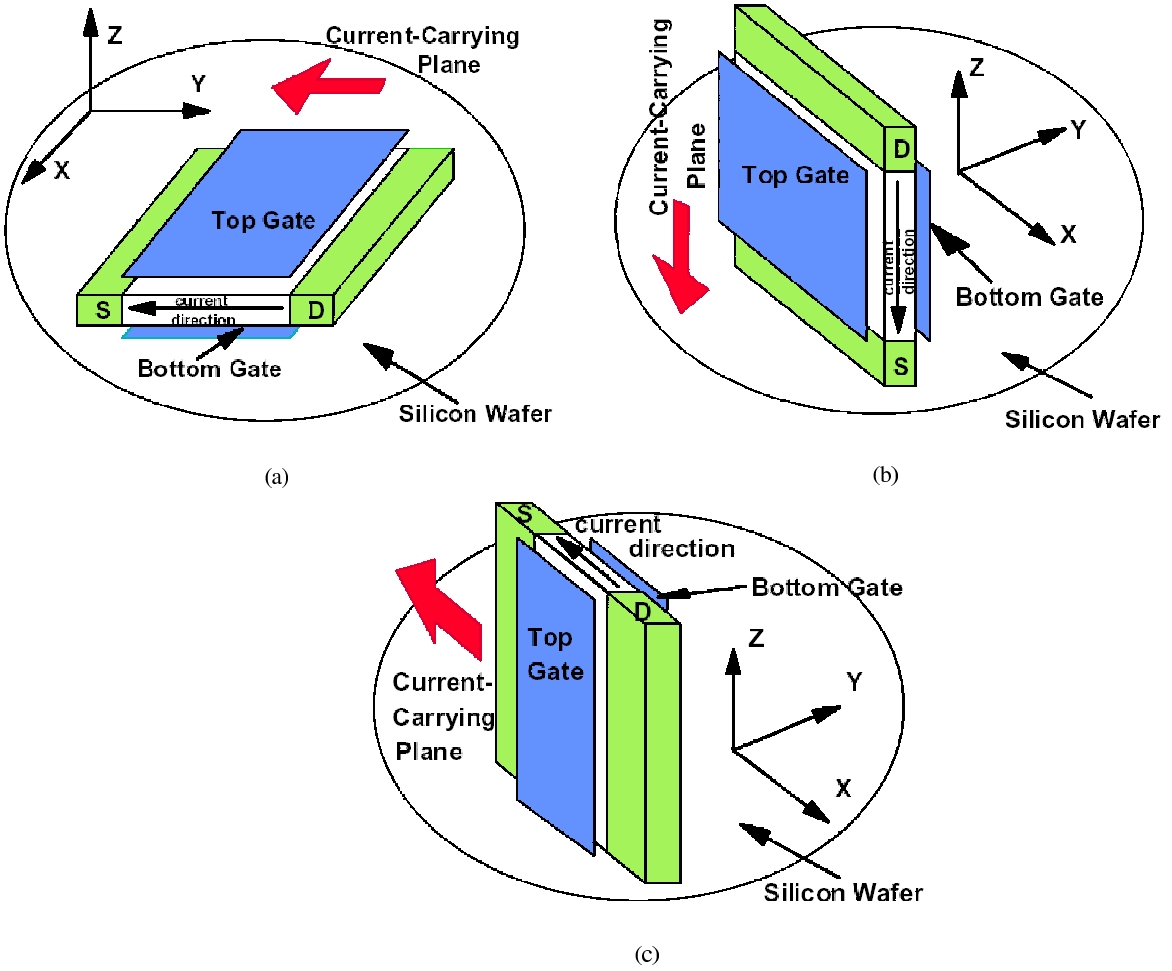


Figure 1.8: Different topologies of DG MOSFETs: (a) Planar type; (b) Vertical type; (c) Fin type.

The vertical DG (Figure 1.8(b)), has the channel in the vertical direction, it is most compact for DRAM application [47] with low leakage current, however it is topologically difficult for a CMOS logic application [44]. Moreover, it is very difficult to fabricate the vertical DG, especially due to the control of the vertical doping profile, and showing no potential advantages comparing to the FinFET.

Currently, the Fin type (Figure 1.8(c)) seems to be the most promising structure,

which is being studied by many groups [38, 39, 48, 49]. In FinFET DG MOSFET, the current flows horizontally through the fin channel, has the highest packing density for high speed logic applications, since the channel width, the longest dimension of a logic FET, is perpendicular to the plane of the wafer [44].

Among those above device, one of the most important device structures is planar DG MOSFET, which is selected for studying their electrical performances where the interest of this thesis is in device design and basic physical modeling. One of the greatest reason to deal with this kind of MG MOSFETs is the scaling capability to the shortest channel length for a given gate oxide thickness, (because the bottom gate can effectively screen the field penetration from the drain), hence suppress the short channel effects. We can cite these advantages as: (a)ideal 60mV/decade subthreshold slope [50]; (b)scaling by silicon film thickness without high doping; (c)setting of threshold voltage by gate work functions [51], (d) easy fabrication because of its planner structure, etc...

In this thesis, the focus will be put on the compact modeling for of planar DG MOSFET. Our group has worked on analytic surface potential and threshold voltage models for DG MOSFETs several years before [52]. One of the contributions of this thesis is to extend the DG model according to the charge concentration evaluation including short channel and quantum effects. Then, the developed accurate analytical models, for subthreshold and saturation regimes, will be used to improve the electrical performances of the DG MOSFETs for nanoscale applications. Efforts will also be focused on making the physics-based model more versatile and computationally efficient using soft computing approaches.

1.2.3 Advantages of Gate All Around MOSFETs

As discussed above, the UTB SOI MOSFETs can be fabricated in different forms it may be a single or double gate, a cylindrical gate or quadruple gate MOSFET. GAA MOSFET devices presented in section 1.2.1 with undoped channel has been applied for different applications. It is suitable for digital applications and have found places

in varieties of applications like base-band analog applications, memory applications etc. The GAA MOSFETs are considered to be among the most prominent multigate CMOS devices for future generation Nano-scale IC technology due to their important advantages cited as:

- Better scalability than the double-gate MOSFETs (i.e., better control of SCE).The reason behind that the surrounding gate creates an electrical sheltering action for lateral electrical fields creating due to the charges in the source and drain. The superior scalability of the device could make the GAA MOSFET suitable for future generation CMOS technology with gate-length scaled below 25nm.

- Better switching characteristics where an ideal Subthreshold swing of 60mV/Decade could be expected in a GAA gate MOSFET. This may provide higher ON-to-OFF current ratio than that of the bulk MOSFET thereby providing better switching characteristics.

- Higher drive current since the current flow across all surrounding surface of the silicon body (not only just from the top edge as well as bottom edge in the ultra-thin body SOI DG MOSFET), the ON-state drive current can practically be greater of that of the double-gate device.

- Higher transconductance and greater linearity of GAA MOSFETs can be achieved by increasing the doping level in the channel region of device. It may be mentioned that the doped GAA MOSFETs are important for many analog and RF applications.

In fact, our research group has focused on the analytical analysis of GAA MOSFETs including hot-carrier effects in order to study the scaling limits of GAA MOSFET several years ago [53]. In this thesis, our research is focused on investigation of new kind of GAA MOSFET called Junctionless (JL) GAA MOSFET which exhibits better performance with respect to GAA mosfet in term of fabrication process. Effort will also be focused on development of new subthreshold swing and scaling length models in order to illustrate the

scaling capability of the JLGAA for ultra-low power nanoscale CMOS-based applications over GAA MOSFET design.

1.3 Compact modeling: State of the art

A compact model provides a link between process technology and circuit design. It mathematical describes the complex device physics in a transistor where it retains the fine balance between accuracy and simplicity. An accurate model based on physic allows the process engineer and circuit designer to make projection beyond the available silicon data (scalability) for scaled dimensions and also enable fast circuit and device co-optimization. The simplifications in the physics allow mathematical approximations and by consequence enable very fast analysis of device/circuit behavior in comparison with the much slower numerical simulators. Thus, it is necessary to develop a compact model for MG MOSFETs for technology circuit development in the short term and for product design in the longer term.

One of the biggest challenge is modeling MG FETs is the need to model several flavors of MG FETs. The silicon body can be controlled by either two gates, three gates or four gates. The gates can all be electrically interconnected or they can be independently biased. Multigate FETs can be built on SOI or bulk silicon. It is important to obtain a flexible model which can model all the type of Multigate FETs without making the model computationally intense. Figure 1.9 shows the development cycle of the compact model

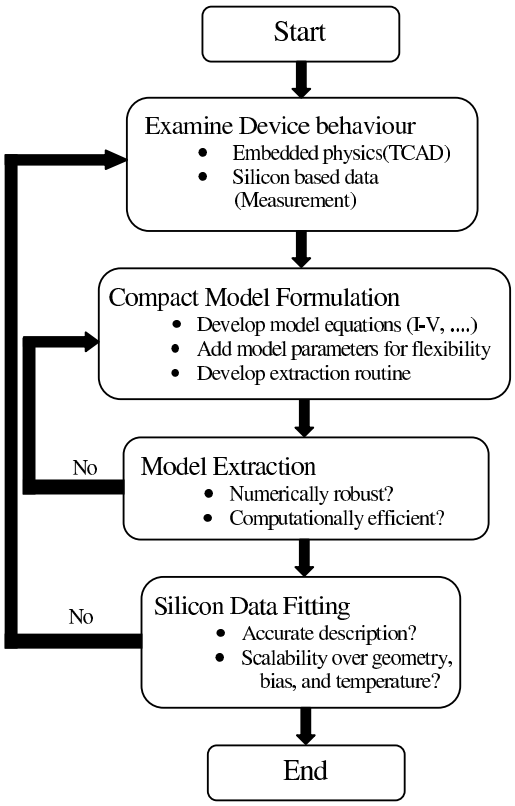


Figure 1.9: Development cycle for compact modeling

1.3.1 Overview of compact modeling of Bulk MOSFETs

As mentioned in section 1.1, MOSFET has been the main component of integrated circuits ever since its invention. Therefore, compact modeling of MOSFETs has also been continuously growing for complex circuit design. Compact model of MOSFETs usually based on a precise core model (long channel classical model) then all specific physical phenomena that include quantum effects, short channel effects, channel length modulation,etc..., are implemented into this core model as parameter corrections in order to achieve fast and accurate circuit simulation results.

Figure 1.10 shows the schematic diagram of a compact model for a MOSFET. The evolution of MOSFET compact model starts from simple, piecewise, to complicated models, continuous models to achieve more accurate circuit simulations. For example the earliest versions of BSIM model, (piecewise models), which perform separate equations

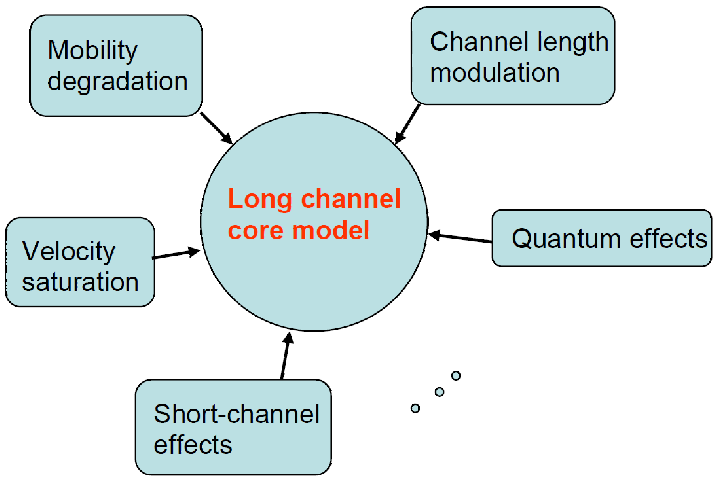


Figure 1.10: Schematic diagram of a compact model for the bulk MOSFETs

based on the charge sheet approximation for different operation regions. This leads to the discontinuous first order derivates of current and charge and hence rigorous convergence. Non-physical mathematical smoothing functions are adopted in recent BSIM3/BSIM4 models in order to manually connect the different operation regions, as well as to overcome the convergence problem [54]. Although this approach largely solves the convergence problem, the non-physical smoothing equations fail to physically describe the transition region where MOSFET transistors in analog circuits are commonly biased.

To avoid the disadvantages of BSIM models, the surface potential models developed by the *Pennsylvania State University and Philips* (PSP) [55] and those developed by the *Hiroshima University Semiconductor Technology Academic Research Center* (HiSIM) [56] have been presented as the next generation of compact model for bulk MOSFETs. Without introducing the threshold voltage, one single surface potential equation valid for all the operation regions is solved for the solution in these models.

1.3.2 Overview of compact modeling of Multigate MOSFETs

The MG devices that control the channel from multiple sides and very thin body devices are new to circuit and system designers. These devices need to be modeled to understand and predict the functionality of the circuits. Compact device models are used

in circuit design. New compact models that accurately model these novel devices, and are computationally efficient, are in development. There are new physical effects that now need to be incorporated into these device models.

The use of multiple gate devices in circuit design is critically dependent on the availability of accurate models for these devices, valid for DC, AC, transient and noise analysis. Using appropriate models, circuit simulation allows to design circuits with devices of adequate dimensions. Circuit simulation requires accurate models of the current and the terminal charges (from which capacitances are obtained) of the devices. These models should be based on expressions with a sufficiently high order of continuity. Lack of continuity between the different operating regimes leads to convergence problems in circuit simulation. In conventional MOSFETs, there have been a trend to move from piecewise models (with continuity problems) to unified models with an infinite order of continuity. Smoothening functions are often used to assure the continuity between different operating regimes. For the same reasons, multiple-gate MOSFETs will need unified highly continuous models.

For proper modeling of nanoscale MOSFET for VLSI circuit simulation, accurate and physics-based compact models are required. The modeling principles for these devices are somewhat different from conventional bulk MOSFETs, since volume conduction should be considered.

1.3.2.1 Double-Gate MOSFETs

As discussed in the last section, the compact model development for bulk MOSFETs has shown that an ideal long channel core model should be continuous, symmetric, physics-based, accurate and computationally efficient are still a modeling challenge. These requirements set the objective of the compact modeling of DG MOSFETs. Previous work mostly focused on the modeling of some particular physical phenomenon have been made to implement compact models giving insight to understand the physics and operation of DG MOSFETs. For instance, a core model for DG MOSFETs was developed by Taur based on the solution of 1-D Poisson and current continuity equations where the charge-sheet

approximation is not taken into account [28, 57].

A number of attempts have been made to approximate these expressions including intermediate parameters in order to express the body potential, inversion charge, and drain current [58, 59]. In these works, the electric characteristics of DG MOSFETs is described as functions of charges, where obtained charge equations are still implicit, thus there is no mathematical advantage to remove the intermediate parameters. In addition, each approximation initiate non-negligible error either in the transition region or on-current regions.

Numerical study of the body doping effects on double-gate MOSFET characteristics is suggested in [60]. After that the threshold voltage shift and the subthreshold current slope degradation are discussed intensively following by an analytical solution to the 1-D Poisson's equation [61]. Because it is impossible to solve three coupling implicit equations analytically, a series of appropriate assumptions were involved to solve the equation in a non-coupling way.

The short-channel effects were taken into account by solving 2-D Poisson's equation in evanescent mode which is largely adopted by the bulk MOSFETs [62, 63], or assuming parabolic potential shape [64, 65]. Whereas, the obtained solution according to the parabolic potential assumption is less accurate at the silicon-silicon dioxide interface. Explicit expressions for threshold voltage roll-off [66–68] and subthreshold [69] current slope were also developed [63] by solving the current continuity equation basing on the minimum potential barrier along the channel.

Furthermore, when quantum effects dominate, there still lacks a comprehensive compact model for DG MOSFETs. Several approaches have been applied to study quantum effects in DG MOSFETs, such as the nonequilibrium Greens function [70], density gradient model [71, 72], and Monte Carlo simulation [73–75]. However, these mathematical complex models make them impractical for compact modeling.

In another work, only the potential and charge distribution have been carried out by the analysis of quantum subband energy levels [76] and the quantum threshold shift [77], but no drain current equation has been developed for a compact model.

Recently, an implementation of an analytic potential-based terminal charge and capacitance model was carried out for AC and transient simulations [78]. Employing different forms of drain current expression results in similar expressions for the terminal charges and capacitances [79].

In this context, we apply in chapter 3 a soft computing approaches particulary Genetic Algorithm, Fuzzy Logic to implement quantum effects into an analytic charge model as quantum corrections for DG MOSFETs in order to develop continuous quantum drain current model close to NEGF numerical simulation.

1.3.2.2 Gate All Around MOSFETs

Most of the existing GAA MOSFET models are based on one-dimensional (1-D) analysis, and are suitable only for long channel devices [80]. As consequence, they are unable to reproduce the roll-off as the channel length is reduced. A two-dimensional analysis is necessary to derive threshold voltage and subthreshold swing models that properly account for the channel length dependence. A few 2-D models of the threshold voltage for doped and undoped GAA MOSFETs have been presented [81, 82]; however, all of them neglect the effect of the mobile charge density, which can be important in the near-threshold regime (in particular for undoped devices).

Furthermore, simple continuous analytic current-voltage (I-V) model for cylindrical undoped (lightly doped) GAA MOSFETs where the charge-sheet approximation allowing adequately capture of inversion charge distribution in the silicon [83].

Recently, Hamedy et.al., have proposed an analytical, physically-based, models for the threshold voltage, the subthreshold swing and DIBL of undoped cylindrical Gate All Around (GAA) MOSFETs which have been derived based on an analytical solution of the two-dimensional (2-D) Poisson equation (in cylindrical coordinates) including the mobile charge term, by using new techniques that allow to consider the effect of channel length, thickness and drain-source voltage [84]. His model is validated by comparison with the results obtained from 3-D numerical simulations with DESSIS-ISE for different channel lengths/thickness and from low to high drain-source voltage values.

As an extended work, Hamdy et.al have developed an analytical and continuous DC models for cylindrical undoped GAA MOSFETs, in which the channel current is written as an explicit function of the applied voltages [80]. The model is based on a new unified charge control model developed for the device. The explicit model shows good agreement with the numerical exact solution obtained from the new charge control model, which was validated by comparison with 3D numerical simulations.

Another compact models for GAA MOSFETs [85] have been recently developed using several approximation in order to derive analytical solutions of Poisson's equation for doped and undoped devices. In this work, self-consistency with Schrödinger's equation combined with the current continuity equation are addressed to describe the carrier transport models. Thus, it overcome some difficulties in compact modeling :the electrostatics, the quantum effects, the transport mechanisms, and the high-frequency behavior.

1.4 Outline of the thesis and contributions

The main goal of this work is to apply new soft computing approaches in order to improve the computational performance in term of computing time and accuracy, propose new design structures of nanoscale multigate MOSFETs to study their electrical performances for digital and analog applications. Moreover, both analytical and compact models are developed to be exported to the IC design community worldwide. This dissertation is devoted to the design, modeling and improvement of the electrical parameters of several MG MOSFETs design structures.

In this Chapter, a review MOSFET scaling, DG and GAA MOSFET technology and device modeling have been presented. We have also clarified the motivation of research on MG MOSFETs.

General concepts and description of evolutionary computation and artificial techniques are presented in Chapter 2. This chapter introduces the fundamentals of genetic algorithm (GA) and fuzzy logic (FL) control, gives an overview of existing multi-objective optimization and compares possible advantages of one over the other.

Chapter 3 develops short channel compact models of drain current in symmetric DG MOSFETs including the threshold voltage shift and the gate capacitance degradation due to quantum effect, channel length modulation and electron mobility degradation due to short channel effect. Starting from 1-D analytical solution of the Poisson equation, we derive the long channel drain current model of undoped DG MOSFET assuming gradual channel approximation (GCA), which is mainly depending on effective electron mobility, electron distribution and quasi-Fermi level. GA and FL are employed as training and optimization tools to generate the optimal and correct distribution of these parameters, where accurate analytical models for nanoscale DG MOSFET close to exact numerical model (NEGF) are successfully obtained.

According to the developed model of symmetric DG MOSFETs in Chapter 3, reliable and optimized design of DG MOSFET for nanoelectronics digital and analog applications is presented in Chapter 4. In this Chapter, Multi-Objective-Genetic Algorithm (MOGA) approach is proposed to find out the optimal dimensional (channel length, silicon thickness and oxide thickness) and electrical parameters (threshold voltage rool-off, OFF-current, drain-induced barrier lowering, subthreshold swing, output conductance and transconductance) of DG MOSFET which would provide to the circuit designers several possible solutions to choose the one that suites best his analog and/or digital application.

Chapter 5 investigates the subthreshold behavior of new proposed MG MOSFETs designs. In the first part of the chapter, semi-analytical models of the surface potential and the subthreshold swing factor in DG MOSFETs are developed including free carriers and interfacial traps effects. These analytical results can help us to physically understand the impact of the channel length, hot carrier induced interface charge density and free carriers on the scaling capability of the thin DG MOSFETs. In the second part of this chapter, the subthreshold parameters of the nanoscale Gradual Channel Gate Stuck (GCGS) DG MOSFETs (threshold voltage rool-off, drain-induced barrier, subthreshold swing and OFF-current) are employed as objective functions which are the pre-requisite of MOGA application. This approach is used to search for optimal subthreshold parameters where superior electrical performances in subthreshold regime are provided by the

proposed device which offers low OFF-current, high ON-current with ideal subthreshold swing required for digital application. In the third part, an analytical investigation is proposed to study the subthreshold behavior of Junctionless Gate All Around (JLGAA) MOSFET for nanoscale CMOS analog applications (low power application). Based on 2-D analytical analysis, a new subthreshold swing model for short-channel JLGAA MOSFETs is developed in order to compare their performances with the conventional GAA MOSFET to highlight the obtained improvement. The proposed analytical models are used to formulate the objective functions for searching the optimal electrical and dimensional device parameters. The obtained parameters offer significant improvement in terms of circuit electrical performance: gain and cut-off frequency satisfying the subthreshold working condition which make the JLGAA MOSFET as a better choice for nanoscale ultra-low power CMOS-based applications.

Conclusions of the dissertation and discussion of future directions beyond the scope of this work are drawn in the last chapter.

Chapter 2

Soft Computing based methods

Contents

2.1 Introduction to the soft computing

For better understanding the real meaning of the new term of soft computing, it is interesting to identify the first who has created this term. It was Lotfi A. Zadeh, father of fuzzy logic and one of the leaders in the soft computing community, who has coined the label "soft computing (SC)" to name an interdisciplinary field that covers different approaches to Artificial Intelligent (AI). He formulated this new scientific concept in [86] "In traditional -hard- computing, the prime desiderata are precision, certainty and rigor.

By contrast, the point of departure in soft computing is the thesis that precision and certainty carry a cost and that computation, reasoning, and decision making should exploit -wherever possible-the tolerance for imprecision and uncertainty" written by Zadeh about 20 years ago [86].

Zadeh has also named "soft computing" by the following definition [87]: "Soft computing is an emerging approach to computing which parallels the remarkable ability of the human mind to reason and learn in an environment of uncertainty and imprecision."

In general, SC is consisted of neurocomputing, fuzzy logic, evolutionary computing, and probabilistic reasoning. These later were mainly designed to model and perform solutions to real world problems, which are not yet modeled or too difficult to model, mathematically. SC methodologies have gained increasing attention over the past years due to their suitability for problem solving and also provide flexible information processing that are capable to handle real-life confusing situations [88].

The main principle of the SC is to elaborate the methods of computation that lead to a desired solution with low cost and more robustness by seeking for an approximate solution to inaccurate or precisely formulated problem. SC differs from conventional (hard) computing in term of tolerance of imprecision, uncertainty, partial truth and approximation. Therefore, the role model for SC is the human mind. SC is basically an optimization technique which is applied to find solution of problems that are very hard to answer.

2.2 Soft computing coupled with optimization based modeling

Optimization based modeling is basically the technique to exploit in order to find the optimal parameters model that minimize or maximize a specified cost function as shown in Figure 2.1. This technique is widely used in several fields such as physics, chemistry, economics, and engineering where the goal is to maximize efficiency, models accuracy, device reliability and other application reasons.

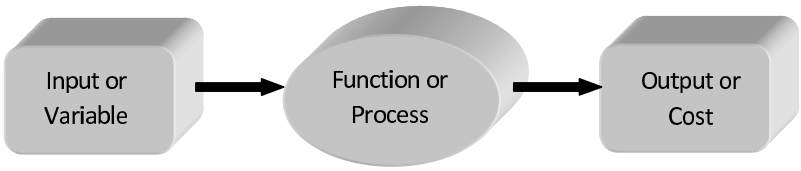


Figure 2.1: Optimization mechanism

The successful solution of such problem, especially the nonlinear problem is based on the well choice of an optimization modeling strategy by coupling the SC methodology. There are many important parameters to be taken into account for optimization such as the type of model input variables (continuous, discrete or mixed), the type of objective function (smooth or nonsmooth, differentiable, etc.), constrained or unconconstrained problem, shape of feasible design space, the number of design input variables, the number of constraints, cost of each simulation, linear or nonlinear functions, local and global optima, etc.

Therefore, the optimization procedure is a very complex problem that has to be treated by SC approaches such as FL, GA, PSO, etc... In addition, the idea of bringing SC methodologies into the area of optimization based modeling lead to prove efficient in practice and powerful in solving real world problem. The remaining parts of this chapter describe, with more details, the function of those soft computing methodologies (Sections 2.3 and 2.4 refer to single and multiobjective genetic algorithm respectively while Section

2.5 refers to Fuzzy logic computation) that will be used in the scope of our research on optimization based modeling via SC.

2.3 Genetic algorithm

Genetic algorithms provide to soft computing an efficient mechanism for solving difficult problems through a systematic stochastic search based on the principles of natural selection. There have been several schools of thought that have contributed to and enriched the field, but share the same underlying principles with GAs [89], i.e., evolutionary strategies [90] and evolutionary programming [91]. Genetic algorithm has been applied to a variety of problems, many of which conventional methods have failed to solve, when Genetic algorithm can effectively solve these and other hard problems.

2.3.1 Principal concept

Genetic algorithms [89, 92, 93] emphasize genetic encoding of potential solutions into chromosomes and apply genetic operators to these chromosomes. A canonical genetic algorithm (also called simple or standard GA) [92] is the one which uses binary representation, one-point crossover and bit-flipping mutation. A canonical genetic algorithm can be implemented as shown in the following algorithm:

Algorithm 1 Canonical genetic algorithm

Generate the initial population P(0) at random and set i = 0;

REPEAT

1: Evaluate the fitness of each individual in P(i);

2: Select parents from P(i) based on their fitness;

3: Apply single-point crossover to selected parents;

4: Apply bit-flipping mutation to crossed-over new individuals;

5: Replace parents by the offspring to produce generation P(i + 1);

UNTIL the halting criterion is satisfied

As genetic algorithms (GA) are modeled after the processes of evolution and genetic recombination, the building blocks of the algorithms are named after genetic elements. Genes are the binary encoding of each problem variable, and all of the genes as a string are referred to as a chromosome or individuals. A set of chromosomes is called a population which contain of the necessary information about the individuals. The GA randomly creates an initial population of individuals to be served to create new generations. Each chromosome in a population has a fitness associated with it, which is calculated through a fitness function. The chromosomes in each population are ranked from best to worst based on their fitness. The higher ranked chromosomes are mated to produce a new population that exhibits characteristics of the better individuals from the previous generation. Mutation is allowed to occur at a small probability. This process repeats until either a desired fitness has been achieved or a set number of generations has occurred.
The flowchart of a basic genetic algorithm just described is shown in Figure 2.2.

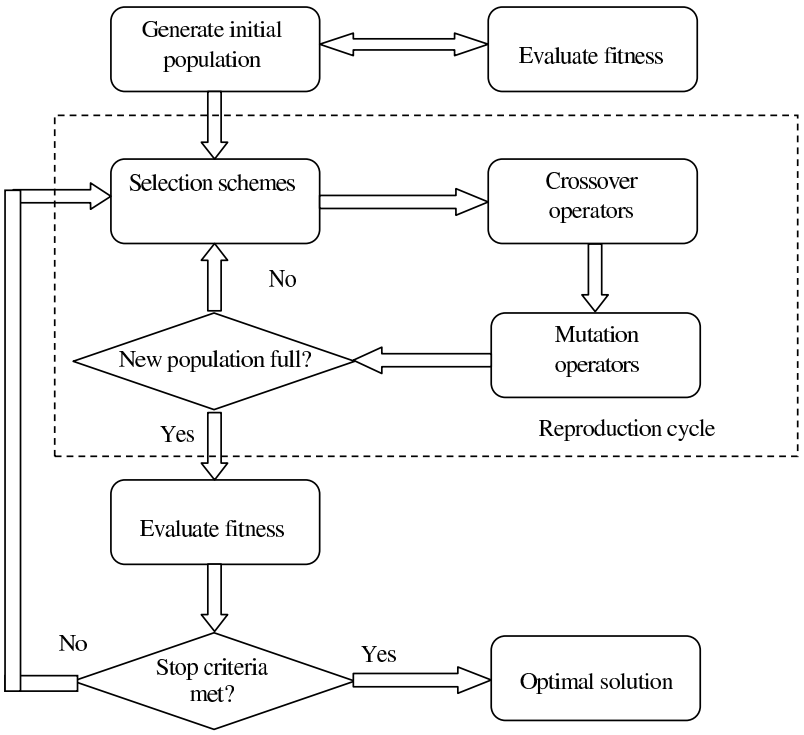


Figure 2.2: Flowchart for simple genetic algorithm

2.3.2 Representation

Since the variable values are represented in binary, there must be a way of converting continuous values into binary, and visa versa. In this context, each variable in the optimization problem must be coded as a gene, and all variables concatenated together form a chromosome. The sample chromosome shown in Figure 2.3 is composed of N parameters with each parameter containing 4 binary digits.

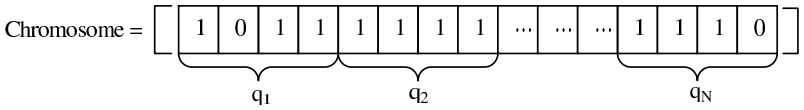


Figure 2.3: Example chromosome with N parameters composed of 4 binary digits each

Each gene q_N has a mapping from the chromosome space to the parameter space. It is important to fully understand the range and precision necessary for each variable so that the entire solution space can be explored and also to ensure that each gene, and thus each chromosome, generated by the GA is a realizable solution to the optimization problem. In addition, the chromosome must first be decoded in order to be evaluated by the fitness function because the GA works with the binary encodings as previously mentioned but the fitness function often requires continuous variables.

2.3.3 Evaluating fitness

The fitness function is the most important part of a genetic algorithm, as it is part of the algorithm that forms the connection to the physical problem being optimized. The fitness function must assign a number to each individual that is a measure of the goodness of the present individual in relation to the optimization goals. The success of the algorithm is dependent on how well the fitness function evaluates each solution in relation to the overall objectives of the optimization problem. The fitness function is generally the most time-intensive part of a genetic algorithm, so it is also important when considering the time efficiency of the optimization algorithm.

2.3.4 Selection schemes

A selection scheme determines the probability of an individual being selected for producing offspring by crossover and mutation. In order to search for increasingly better individuals, fitter individuals should have higher probabilities of being selected while unfit individuals should be selected only with small probabilities. Different selection schemes have different methods of calculating selection probability. There are many methods used to determine which individuals should be used as parents, the four most popular being rank-based selection, roulette wheel selection (also known as the fitness proportional selection), tournament selection and elitist selection.

- **Rank-based selection** selects the individuals which are ranked from highest to lowest based on their fitness [94]. A minimal fitness is chosen as the cut-off and any individuals with a lower fitness than this threshold is removed from the population. The remaining individuals are randomly paired to produce offspring and create the next generation. The advantage of rank-based selection is the simplicity of its implementation. However, this simplicity is offset by the tendency to eliminate unique characteristics of the population thus decreasing the diversity of the sample population at a very early stage.

- **Roulette wheel selection** calculates the selection probability directly from individual's fitness values and assigns it to each individual in the population based on relative fitness values [94]. Figure 2.4 shows how individuals are assigned a space on the wheel that is directly related to their relative fitness. The wheel is "spun" and the result of the spin selects the individual to be used in the mating process. Individuals with high fitness values will be selected as parents more frequently than the less-fit individuals causing characteristics associated with higher fitness values to be represented more in subsequent generations. However, it can be seen that there is still a small probability that an individual with a low fitness value will be selected for the mating process, thus preserving their genetic information and maintaining a higher level of diversity.

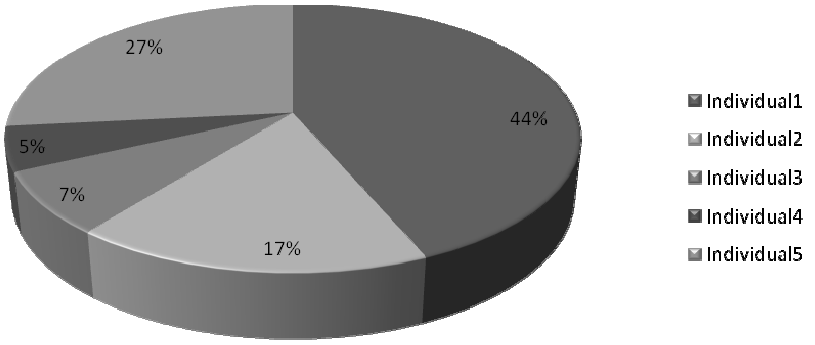


Figure 2.4: Roulette wheel selection with each slice proportional to the individual's relative fitness

Roulette wheel selection may cause problems in some cases. For example, if an initial population contains one or two very fit but not the best individuals and the rest of the population are not good, then these fit individuals will quickly dominate the whole population (due to their very large selection probabilities) and prevent the population from exploring other potentially better individuals. On the other hand, if individuals in a population have very similar fitness values, it will be very difficult for the population to move towards a better one since selection probabilities for fit and unfit individuals are very similar.

- **Tournament selection** chooses a sub-population of N individuals at random from the population and compete based on their fitness values. The individual with the highest fitness value wins the tournament and is selected as a parent in the mating pool. All the sub-population members are returned to the general population and the process repeats till the mating pool is full. Tournament selection acts much as roulette wheel selection, with the more fit individuals having a higher probability of selection while still maintaining the diversity of the population. The advantage of tournament selection is the absence of fitness ranking, which makes it a faster process than roulette wheel selection.

- **Elitist selection** is also known as elitism and elitist strategy. It always copies the best individual to the next generation without any modification. More than one individual may be copied, i.e., the best, second best, etc., may be copied to the

next generation without any modification. Elitism is usually used in addition to an accepted selection scheme.

2.3.5 Crossover operators

The crossover operator is emphasized as the most important search operator of a GA. Crossover in a GA with crossover probability selects two parent individuals and recombines them to form two new individuals, i.e., two new designs. Thus, all offspring are generated from two selected parents through the process of crossover.

There are many variations of crossover, but the most popular methods include uniform, single point, and multiple-point crossover. Single point crossover [95] is the simplest. A random location in the parent's chromosome is selected and the portion preceding that location is copied from parent 1 to child 1 and from parent 2 to child 2. The portion of the chromosome following this point is copied from parent 1 to child 2 and from parent 2 to child 1, as shown in Figure 2.5. Multiple-point crossover [95] is an extension of single point crossover, where more than one point is selected in the parent chromosome as shown in Figure 2.6.

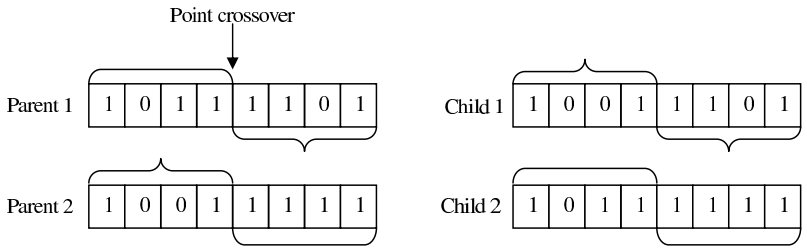


Figure 2.5: Example of single point crossover

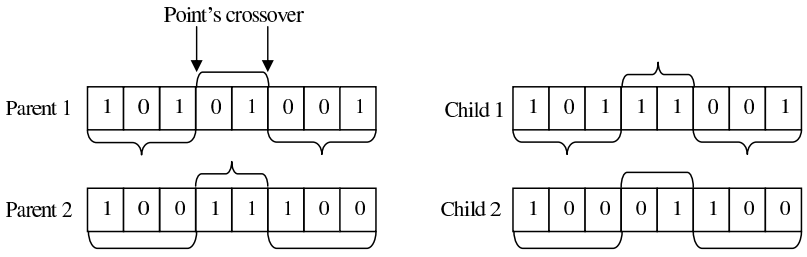


Figure 2.6: Example of multi-point crossover

Uniform crossover [95] is accomplished through the use of a randomly generated mask that contains the same number of binary bits as the parent chromosomes. The numbers in the mask indicate whether the bit from parent 1 or parents 2 should be translated to each child. Figure 2.7 shows an example of uniform crossover, where a 0 in the mask indicates for child 1 that the bit should taken from parent 1 and a 1 indicates that the bit should be taken from parent 2. The opposite is true for child 2, where a 0 indicates that the bit should come from parent 2 and a 1 indicates the bit should be from parent 1. In Figure 2.7, all bits taken from parent 1 are noted with a dot, and those lacking dots are from parent 2.

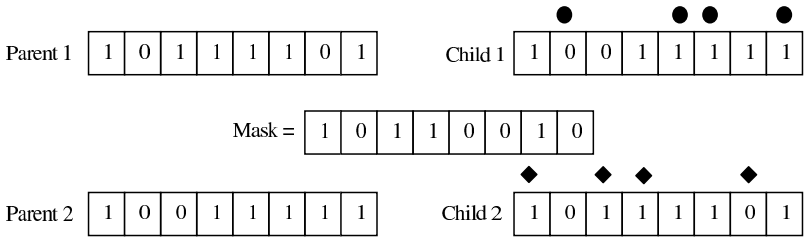


Figure 2.7: Example of uniform crossover

The problem with these crossover methods is that no new information is introduced: each continuous value that was randomly initiated in the initial population is propagated to the next generation, only in different combinations. Although this strategy worked fine for binary representations, and in the case of continuum values we are merely interchanging two data points. These approaches totally rely on mutation to introduce new genetic material.

2.3.6 Mutation operators

Mutations are random changes in chromosomes at the bit level and occur by changing a "1" to a "0" or a "0" to a "1" as shown in Figure 2.8. The mutation operator depends on mutation rate : If the random number which is generated randomly by GA in the interval [0, 1] is greater than the predetermined mutation rate, then mutation is applied and vice versa. Mutation rates used in literature are usually very small (e.g. 0.001) [96].

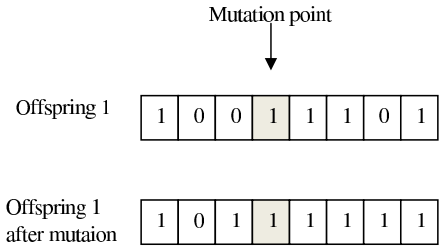


Figure 2.8: Example of mutation operator

2.3.7 Replacement operators

After the creation of new offspring using genetic operator (selection, crossover and mutation), the successor generation is produced. As mentioned previously, the parent individuals are selected according to their fitness, thus the created offspring increase the fitness of the population generation by generation. During replacement operation, genetic algorithm decides whether offspring will survive or will become exist following the most common replacement techniques:

- **Complete Replacement** deletes all the individuals of the successor population and replaces them with the same number of new individuals that have just been created.

- **Steady-state** chooses "n" old individuals from the current population and replaces them with "n" new individuals. The choice of the new individuals number "n" and the deleted individuals from the current population are important aspects of genetic algorithm.

- **Replacement with elitism** is similar to the complete replacement but in this technique one or two individuals with the highest fitness are chosen to be included in the next generation. As a result, good solutions are preventing from become extinct.

2.3.8 Convergence criteria

This generational process is repeated until a termination condition has been reached. In short, the various stopping condition are listed as follows:

- **Maximum generations**: The genetic algorithm stops when the specified number of generations have evolved.
- **Elapsed time**: The genetic process will end when a specified time has elapsed. Notice that if the maximum number of generation has been reached before the specified time has elapsed, the process will end.
- **No change in fitness**: The genetic process will end if there is no change to the population's best fitness for a specified number of generations. Notice that If the maximum number of generation has been reached before the specified number of generation with no changes has been reached, the process will end.
- **Stall generations**: The algorithm stops if there is no improvement in the objective function for a sequence of consecutive generations of length Stall generations.
- **Stall time limit**: The algorithm stops if there is no improvement in the objective function during an interval of time in seconds equal to Stall time limit.

These processes ultimately result in the next-generation population of chromosomes that is different from the initial generation. Generally the average fitness will have increased by this procedure for the population, since only the best chromosomes from the preceding generation are selected for breeding.

2.4 Multiobjective genetic algorithm

Multi-objective optimization problems have received interest form researches since early 1960s. In a multi-objective optimization problem, multiple objective functions need

to be optimized simultaneously. In the case of multiple objectives, there does not necessarily exist a solution that is best with respect to all objectives because of differentiation between objectives. A solution may be best in one objective but worst in another.

Therefore, there usually exist a set of solutions for the multiple-objective case, which cannot simply be compared with each other. For such solutions, called Pareto optimal solutions or non-dominated solutions, no improvement is possible in any objective function without sacrificing at least one of the other objective functions. Thus by using the concept of Pareto-optimality we can find a set of solutions that are all optimal compromises between the conflicting objectives. Pareto-optimality is a concept used economics, game theory, etc. A Pareto-optimal solution is one that is not dominated by any other solution i.e. it is one in which no objective can be improved without a deterioration in one or more of the other objectives.

In the past few years, there has been a wide development in applying genetic algorithms to solve the multi-objective optimization problem, known as evolutionary multi-objective optimization or genetic multi-objective optimization. The basic features of genetic algorithms are the multiple directional and global searches, in which a population of potential solutions is maintained from generation to generation.

The population-to-population approach is beneficial in the exploration of Pareto-optimal solutions. The main issue in solving multi-objective optimization problems by use of genetic algorithms is how to determine the fitness value of individuals according to multiple objectives.

2.4.1 Aggregation approach-based optimization

This is perhaps the most natural and common approach for fitness assignment [97,98]. For a given individual, the values of the multiple objective functions are combined into a single scalar objective function using a linear or nonlinear combination. The main strength of this approach is its computational efficiency and simple implementation. Its main weakness is the difficulty to determine the value of the weights that reflect the

relative importance of each function.

Several applications of evolutionary algorithms using aggregation approaches have been reported. A number of authors have provided examples of the use of the common method known as weighted-sum approach [99–101]. Gen et al. [102, 103] have extended this approach to handle uncertainty using fuzzy logic.

Medaglia and Fang [104] have proposed the use of adaptive weights instead of predetermined fixed weights. Hajela and Lin [105] have used an evolutionary approach (HLGA) in which the weights are discritized and encoded in the chromosome.

2.4.1.1 Cost Function using Weighted-Sum approach

Functional fitness functions are a quantification of an individual's fitness measuring some aspect of performance. Functional fitness functions are often formulated by trial and error or a human designer's expertise (or both). Using functional fitness functions introduces human bias into fitness function design because the human designer must decide how important a particular behavior is to the overall fitness of the individual.

Traditional functional fitness functions, which produce a single value for each individual in the population, are most useful for tasks that have a single, measurable objective. However, functional fitness functions can be used to optimize over multiple objectives. To accomplish this, a fitness function for each objective is formulated, and then a single function for all the objectives is produced by summing each objective's function. Typically, these functions are weighted to give precedence to one or more objectives, and this weighting may introduce a great deal of human bias into fitness function design. The evaluation of multi-objective problem returns a set of fitness functions f that need to be improved simultaneously and is given as,

$$\min_{(X)} f = [f_1, f_2, f_3, ..., f_n] \tag{2.1}$$

where X is the parameter space. However, the solutions that can simultaneously optimize every fitness function are difficult to find for such a multi-objective problem. Therefore,

a commonly used trade-off method combines different objectives into a linear overall objective function presented as a weighted sum:

$$\min_{(X)} = Cost\,(f) = \sum_{i=1}^{n} w_i \cdot f_i \tag{2.2}$$

where w_i is the weight vector that is designed to emphasize the importance of each fitness function f_i. X is the parameter space, which can consist of different types of design parameters for such problem. Thus, the GA multi-objective problem becomes GA single objective and the optimization can proceed by directly evaluating the value of the objective function. As an example, when a constant weight is assigned to each fitness function, which is required to construct the composite objective function, the direction of the GA search is fixed in the multi-dimensional space as shown in Figure 2.9, f_1 , f_2 are fitness functions to be minimized. The close circle in Figure 2.9 represents the final, single solution obtained by the GA. The overall objective function to be minimized simultaneously is given as,

$$F = w_1 \cdot f_1 + w_2 \cdot f_2 \tag{2.3}$$

where w_1 and w_2 are equal ($w_1 = w_2 = 0.5$). However, even with the same importance on each fitness function, each contribution to the weighted sum could be different, since the scale of each fitness function is not the same. Hence, to overcome this drawback, normalised values are preferred to be used to reduce the impacts caused by the scale of the fitness function. The above formula is thus modified as,

$$F_{norm} = w_1 \cdot f_{1,norm} + w_2 \cdot f_{2,norm} \tag{2.4}$$

where $f_{1,norm}$ and $f_{2,norm}$ denotes the normalized values of fitness functions of f_1 and f_2 respectively.

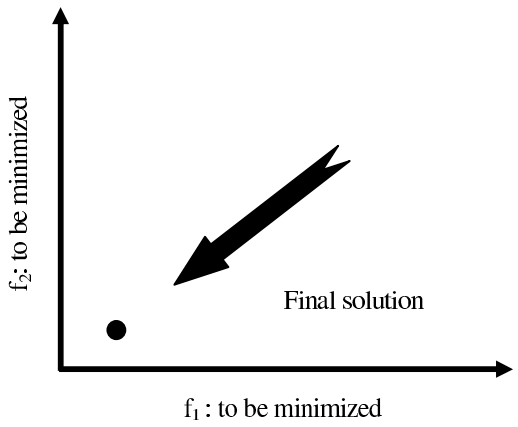


Figure 2.9: Direction of search in GA with a combined fitness function

2.4.2 Pareto front optimization

Another area where multi-objective GAs are particularly effective is Pareto-Front optimization. Many real world optimization problems contain multiple competing objectives and there is a premium on methods that can handle multiple objectives and discover optimal tradeoffs (Pareto-optimal front) between these objectives.

Despite the fact that the evaluation by a weighted sum cost function facilitates the optimization process to a great extent, the most significant limitation of this process is that the fitness functions used in the overall objective function formula are sometimes not in the same scale. Therefore, obtaining a single solution will not necessarily best satisfy the designer's priorities in satisfying the multiple objectives. To address this problem, multiple objectives sould be converted into single-objective problems by using a priori weights denoting the relative importance of the different objectives. These later, rely on multiple runs of single-objective optimization with different weights to obtain different Pareto-optimal solutions. However, the choice of weights is a non-trivial task and furthermore uniform coverage of the Pareto-optimal front is usually improbable, sometimes impossible and the methods are usually inefficient and less robust [106].

On the other hand, population-based approaches such as genetic algorithms are particularly suited to handle multiple objectives as they can process a number of solutions in par-

allel and find all or majority of the solutions in the Pareto-optimal front. Based on Goldberg's suggestion [92] of implementing a selection procedure that uses a non-domination principle, many multiobjective evolutionary algorithms have been proposed [107, 108]

In order to include multi-objective GAs optimization into the evolutionary algorithm, a new evaluation and selection scheme has to be implemented. In the case of multiple objectives, separate fitness values are assigned to the individuals for their performance in different tasks, resulting in a vector of fitness values, instead of only one aggregated fitness value. As a consequence of this, it is no longer possible to decide whether an individual is better or worse than another, by simply comparing their single fitness value.

Therefore, before selection, a ranking of the individuals is achieved by applying the non-dominated sorting algorithm. A fast running of the non-dominated sorting procedure, is shown in Figure 2.10. As an additional ranking criterion for the individuals in the population, crowding distance computation is applied in order to maintain the diversity of the population. Accordingly, two key components enable GAs to handle multiple objectives: (1) selection based on a non-domination principle, and (2) selection based on crowing distance computation.

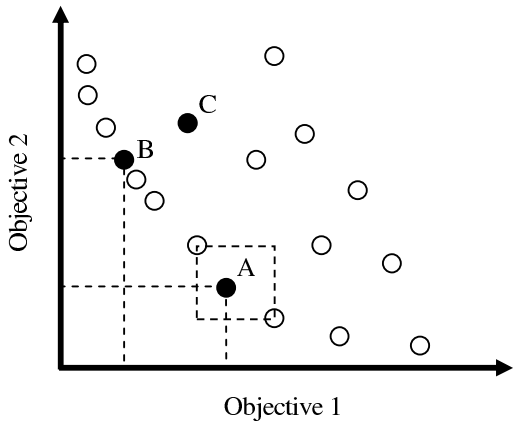


Figure 2.10: : Illustration of non-domination and crowding for a two-objective minimization problem

2.4.2.1 Non-dominated sorting

The non-dominated sorting procedure assigns domination ranks to individuals in the population based on their multiple objective values. A candidate solution X dominates Y, if X is no worse than Y in all objectives and if X is better than Y in at least one objective. For example, in Figure 2.10, solution B dominates solution C, whereas solutions A and B are non-dominant.

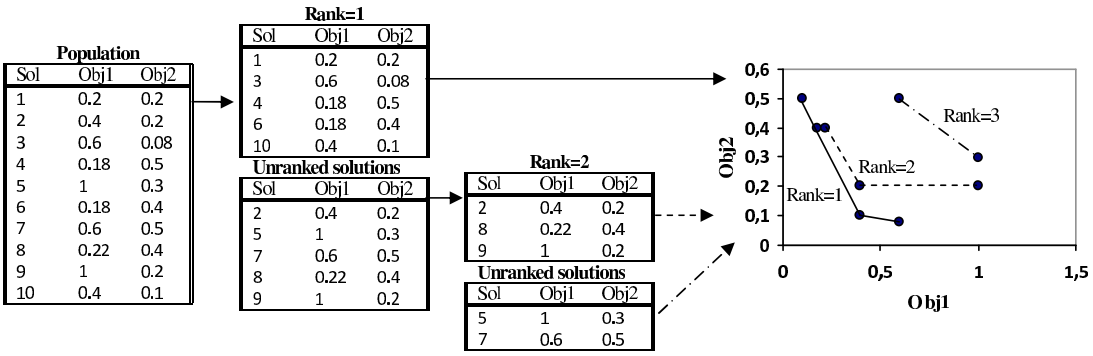


Figure 2.11: Illustration of non-dominated sorting procedure for a two-objective minimization problem from a set of randomly generated population of 10 individuals

In non-dominated sorting, we start with the set of solutions that are not dominated by any solution in the population and assign them rank 1. Next, solutions that are not dominated by any of the remaining solutions are assigned rank 2. That is, all solutions with rank 2 are dominated by at least one solution with rank 1, but are not dominated by others in the population. Thus the sorting and ranking process continues by assigning increasing ranks to those solutions that are not dominated by any of the remaining unranked solutions. After non-dominated sorting, we are left with subsets of the population with different ranks. Solutions with a given rank are not dominated by solutions that have the same rank or higher and are dominated by at least one solution with a lower rank. Therefore, with respect to Pareto optimality, solutions with lower ranks should be given priority. The non-dominated sorting procedure is illustrated for a two objective minimization problem in Figure 2.11.

2.4.2.2 Crowding distance computation

Apart from finding solutions in the Pareto front, it is also essential to achieve good coverage or spread of solutions in the front. The diversity of solutions in the objective space is usually maintained using crowding distance computation for doing so. Each solution in the population is assigned a crowding distance, which estimates how dense the non-dominated front is in the neighborhood of the solution.

Therefore, the higher the crowding distance of the solution, the more diverse the solution is in the non-dominated front. For example, in Figure 2.10, solution A is less crowded, and hence more diverse, than solution B.

The selection operator in multiobjective GAs uses the non-domination principle and also typically acts as a diversity preserving operator. As an example, a non-dominant procedures which is based on niching strategy [92], uses an individual comparison operator to compare the quality of two solutions and to select the better individual. Both the rank and the crowding distance of the two solutions are used in the comparison operator, i.e the rank of the two individuals are considered and the solution with a lower rank is selected. If the two individuals have the same rank, then the solution with the highest crowding distance is selected.

2.5 Fuzzy logic

Fuzzy logic was invented by Lotfi A. Zadeh, a professor at the University of California, Berkley, who developed fuzzy set theory in 1965 [109]. He being an expert in control engineering realized that control theory was unable to solve many complex real system problems.

As a short term, fuzzy logic can be viewed as a logical system that aims at a formalization of approximate reasoning. As a long term, fuzzy logic is used as a synonym for fuzzy set theory which has several branches such as fuzzy arithmetic, fuzzy mathematical programming, fuzzy topology, fuzzy graph theory, fuzzy data analysis, and fuzzy logic, among others [86].

The contribution of fuzzy logic to the area of soft computing is to introduce flexibility in classification, querying and problem solving, and to capture imprecision when there is lack of information [110]. In this context, fuzzy logic brings an effective way of compressing and representing knowledge through the use of linguistic variables, linguistic values, and fuzzy if-then-rules.

2.5.1 Principal concept

The basic concept underlying fuzzy logic is that of a linguistic variable, that is, a variable whose values are words rather than numbers (such as small and large). Fuzzy logic uses fuzzy sets to relate classes of objects with unclearly defined boundaries in which membership is a matter of degree.

As an example, in the theory of conventional sets, an element belongs or does not belong to a set, so the degree of membership of an element in a set can be only zero or unity. However, in the theory of fuzzy sets, an element can belong more or less to a set, thus, the degree of membership of an element in a fuzzy set can take any value in the range of [0,1]. What differentiates the two theories arises from limitations of defined sets. In classical theory the contours of the sets are "net", although for the fuzzy sets contours are gradual, or fuzzy as shown in Figure 2.12:

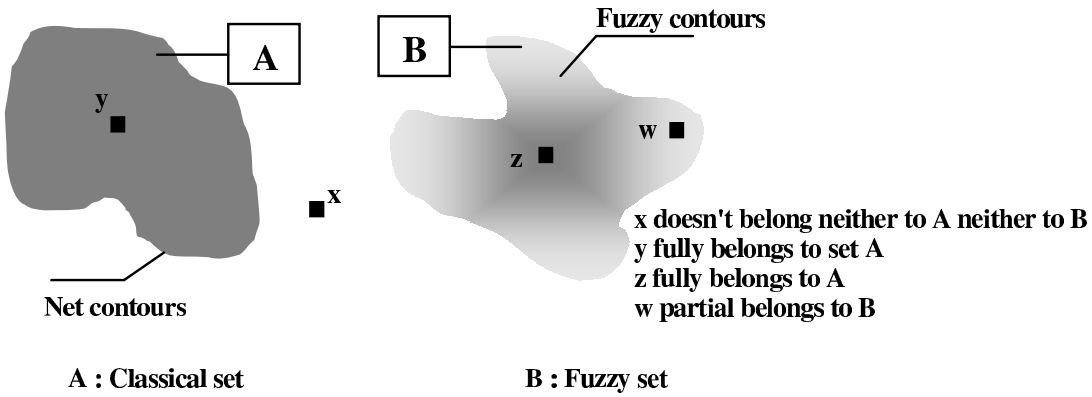


Figure 2.12: Comparison between classical and fuzzy sets

2.5.2 Fuzzy set and Membership functions

As mentioned previously, a fuzzy set is an extension of a crisp set where an element can only belong to a set (full membership) or not belong at all (no membership). Fuzzy sets allow partial membership which means that an element may partially belong to more than one set. A fuzzy set A is characterized by a membership function μ_A that assigns to each object in a given class a grade of membership to the set. The grade of membership ranges from 0 (no membership) to 1 (full membership) written as,

$$\mu_A : U \rightarrow [0, 1] \tag{2.5}$$

which means that the fuzzy set A belongs to the universal set U (called the universe of discourse) defined in a specific problem. A membership function defines how each point in the input space is mapped to a degree of membership.

For example, consider the set of membership functions for a set of tall people shown in Figure 2.13. If the set is given the crisp boundary of a classical set, it can be considered that all people taller than $1.7meter$ are considered tall, while those less than $1.7meter$ are short. But, such a distinction is not fully realistic. If one would however consider a smooth curve from "short" to "tall", then the transition would make more sense. A person may be both tall and short to some degree. The output axis would be a number between 0 and 1, known as the degree of membership in a fuzzy set of height.

The value $\mu_A(x)$ in Eq. (2.5) measures the membership or the membership degree to which an element x belongs to the set A. Then, each fuzzy set can be represented by its membership function. The membership functions may be symmetrical, consistently distributed or have a non-uniform distribution. In general, the shape of membership functions depending on the application and the quantity to be modelled may have different shapes: triangular, Gaussian or trapezoidal function, etc. [109, 111, 112]

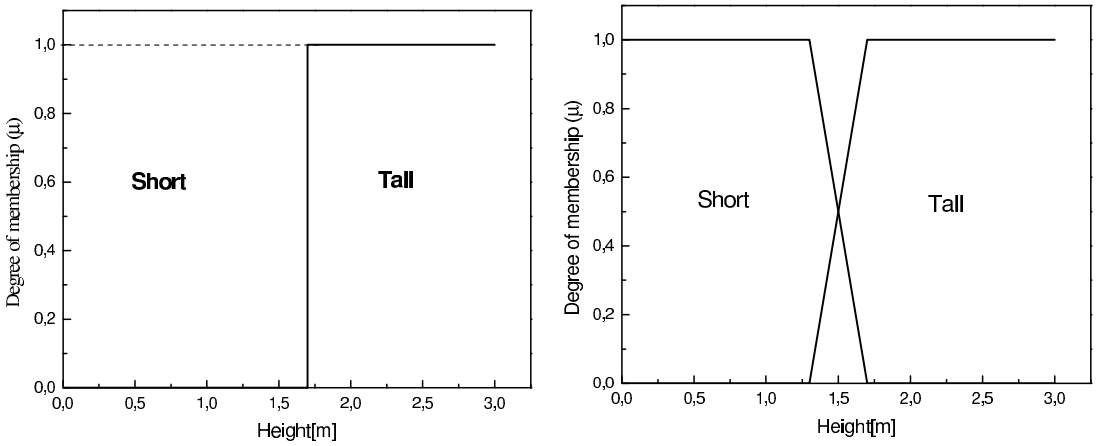


Figure 2.13: Illustration of membership functions for a set of tall people (a) crisp set (b) fuzzy set

$$f(x;a,b,c)=\begin{cases}0, & x\le a\\ \dfrac{x-a}{b-a}, & a\le x\le b\\ \dfrac{c-x}{c-b}, & b\le x\le c\\ 0, & c\le x\end{cases}$$

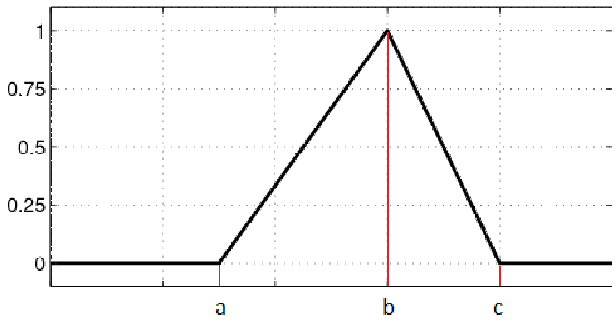


Figure 2.14: Triangular membership function

$$f(x;\sigma,c)=e^{\frac{-(x-c)^2}{2\sigma^2}}$$

c: centre de la gaussienne
σ: sa largeur

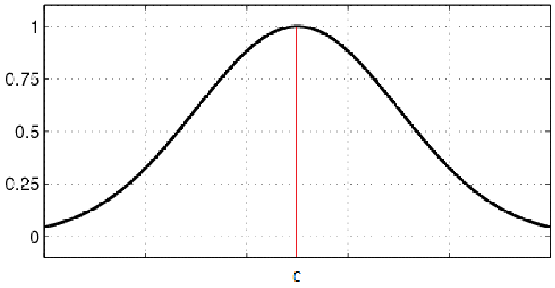


Figure 2.15: Gaussian membership function

$$f(x;a,b,c,d) = \begin{cases} 0, & x \le a \\ \dfrac{x-a}{b-a}, & a \le x \le b \\ 1, & b \le x \le c \\ \dfrac{d-x}{d-c}, & c \le x \le d \\ 0, & d \le x \end{cases}$$

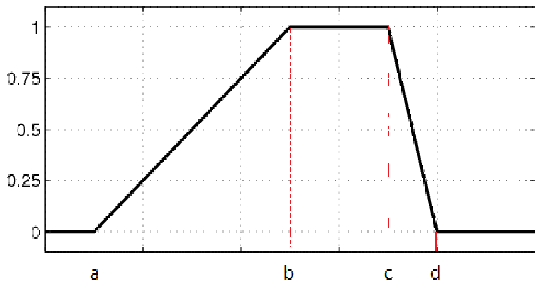


Figure 2.16: Trapezoidal membership function

2.5.3 Fuzzy logic rules

The use of fuzzy sets allows the characterization of the system behaviour through fuzzy rules between linguistic variables. A fuzzy rule is a conditional statement R_i based on expert knowledge expressed in the form:

$$R_i: \quad IF \quad x \quad is \quad small \quad THEN \quad y \quad is \quad large \tag{2.6}$$

where x and y are fuzzy variables and small and large are labels of the fuzzy sets. If there are n rules, the rule set is represented by the union of these rules i.e.,

$$R = R_1 \quad else \quad R_2 \quad else \quad ... \quad R_n \tag{2.7}$$

A fuzzy controller is based on a collection R of control rules. The execution of these rules is governed by the compositional rule of inference [113]. The relationship between the premise and the consequence of the rule is determined by a fuzzy inference, then the degree of truth is defined by a membership function which depends on the degree of truth μ_A and μ_B of the two elementary propositions.

The most common inferences for the determination of the membership functions resulting from the fuzzy scheme are given by:

The inference of Mamdani:

$$\mu_{\mathrm{R}}(\mathrm{x},\mathrm{y}) = \min(\mu_{\mathrm{A}}(\mathrm{x}),\mu_{\mathrm{B}}(\mathrm{y})) \tag{2.8}$$

The inference of Larsen:

$$\mu_{\mathrm{R}}(\mathrm{x},\mathrm{y}) = \mu_{\mathrm{A}}(\mathrm{x}) \cdot \mu_{\mathrm{B}}(\mathrm{y}) \tag{2.9}$$

2.5.4 Fuzzy system controller

Unlike conventional techniques, fuzzy logic does not use accurate formulas or specific mathematical relationships [114]. However, it controls the inferences with several fuzzy rules based on fuzzy operators such as AND, OR, THEN ...

The general structure of a fuzzy logic controller is presented in Figure 2.17 and comprises of three principal components:

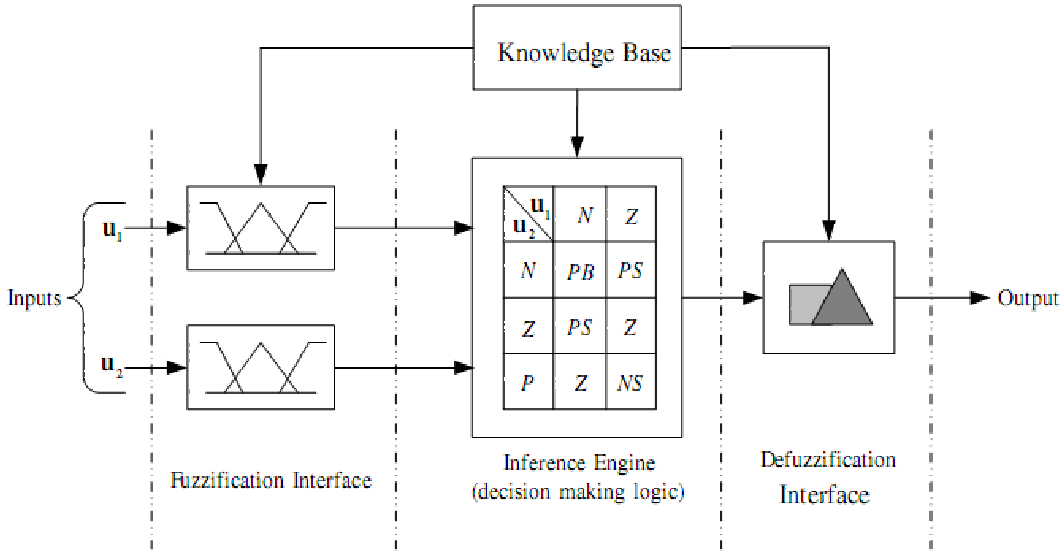


Figure 2.17: Basic configuration of a fuzzy logic controller

2.5.4.1 Fuzzification interface

Fuzzification allows to define membership functions for the linguistic variables. It converts input data into suitable linguistic values using a membership function. This

operation is a projection of the physical variable to the fuzzy sets by characterizing the variable. In addition, it allows an accurate measurement of the degree of membership of the input variable for each fuzzy set [115].

On the other hand, the membership functions defined over the so called universe of discourse (the expected range of variation) of the input variables are applied to their actual values, to determine the degree of truth for each rule.

2.5.4.2 Fuzzy interface inference

The interface inference consists of three blocks:

- **The knowledge base** consists of a database with the necessary linguistic definitions and the control rule set.
- **The rule base** consists of a set of relations linking the input variables to the output variables of the system to be adjusted. The truth-value for the premise of each rule is computed and applied to the consequence part of each rule. This results in one fuzzy set to be assigned to each output variable for each rule.
- **The inference engine** performs the digital processing of inference rules, described by fuzzy operators for linguistic or fuzzy output. It simulates a human decision making process in order to infer the fuzzy control action from the knowledge of the control rules and the linguistic variable definitions. Thus, all of the fuzzy sets assigned to each output variable are combined together to form a single fuzzy set for each output variable. This operation is made by different methods, that are cited as: the inference method max-min, max-product and sum-product. Each of these methods uses a special digital processing operator of fuzzy logic [115].

2.5.4.3 Defuzzification interface

It Converts an inferred fuzzy output set into a a crisp (non-fuzzy) number. During this step, the deduction of the digital output data is obtained from the fuzzy inference in

order to calculate the value of a digital output variable using a set of rules according to the degrees of membership in all fuzzy sets of the input variables and the fuzzy sets of the output variable.

Defuzzification strategy is made by different methods, that are cited as the method of center of gravity, maximum value method and average maximums method [116, 117].

2.6 Application of soft computing in modeling of nanoscale CMOS devices

Due to the fact that simulation of nanoscale CMOS circuits has been the primary factor driving improvements in integrated circuit performance and cost which contributes to the rapid growth of the semiconductor industry, there is a need to develop a new theory and modeling techniques that capture the physics of quantum transport and ballistic transport accurately and efficiently to guide the design for nanoscale CMOS circuits [57,70,118,119].

But from the circuit modeling point of view even 2D solution of numerical models (non-equilibrium Green's function (NEGF) formalism with mode space representation, NEGF with full 2D space representation, Monte Carlo, fully self-consistent coupled Schrödinger and Poisson equations,) is an overkill approach in terms of both complexity and computational cost.

For analytical modeling, in general, it is difficult or almost impossible to obtain closed form analytical models for nanodevices (analytical drain current modeling, physical modeling,) [70, 119–122]. Thus, models are obtained by a simplification of the full physical model. However, the accuracy of such a model can be questionable because of the simplifications made during the model development phase.

Model accuracy and simplicity are important for the design of complex systems. SC methods would be preferable to be applied and could provide practical solutions. In this context, this thesis presents the applicability of SC strategies especially GA and FL for investigation and simulation of the nanoscale (multigate) CMOS-based devices.

The obtained results will be discussed in order to show the efficiency of SC methods for studying future nanoscale devices. SC offers several unique features that make it a particularly good choice for these types of CMOS devices because it:

- Improves the modeling techniques of nanoscale devices which have complex and nonlinear behavior and provides practical insight into physical phenomena in ultra-small electronic devices without the uncertain accuracy or meticulous tuning effort that face more rigorous nanoscale models.

- Improves the computational performances in term of high complex structures and low computation time in comparison with the classical analytical or numerical methods

- Offers better performance in flexibility and suitability for the compact models to be incorporated into circuits electronics simulators. Thus, allow to designer to jump to a step towards a new generation of simulation tools allowing device engineers to explore new classes of electronic devices.

Chapter 3

Compact modeling of drain current model including quantum effects in nanoscale DG MOSFET

Contents

3.1 Introduction

As the MOSFET gate length enters nanoscale field, short channel effects such as threshold voltage roll-off and drain-induced-barrier-lowering become increasingly significant, which limit the scaling capability of MOSFET design [53, 123]. Downscaling MOSFETs to their limits is a key challenge faced by the nanoelectronic industry. Therefore, new designs and structures become necessary to overcome these challenges. The multi-gate design, particularly the Double Gate (DG) MOSFETs(Figure 3.2),have the big importance emerging in nanoscale CMOS circuit design. This is mainly due to the superior control of short channel effects (SCEs) because of the reduced influence of the drain voltage on the channel charge. An accurate information extraction about the current-voltage (I-V) characteristics requires the solution of Schrödinger and Poisson equations based on the non-equilibrium Green's function (NEGF) formalism, assuming quantum effects are to be fully accounted [124]. But from the nanoscale CMOS circuit design point of view even 2-D solution of numerical NEGF is an overkill approach in term of both terms: complexity and computational cost [124]. In this regard, therefore, a high computational speed is necessary if the model is to be implemented in circuit simulators (PSPICE, CADENCE,SYNOPSIS,).

For analytical modeling of semiconductor devices, the Gradual Channel (GCA) model is widely used for analytical semiconductor device modeling. This model, based on first two moments of Boltzman transport equation (BTE), is simple with powerful methods for device simulations. On the other hand, it is well known that GCA model has not accuracy enough for simulation of deep-submicrometer devices in which, rapid changes and confinement of eclectic field, and non-local effects such as velocity overshoot and quantum effects are pronounced [118, 125, 126]. Recently, several papers have been published to model the nanoscale DG MOSFET [127–133]. However, in these publications, simple and accurate closed expressions for quantum capacitance, channel length modulation and drain current were not provided, thus limiting the models which will be used by the designers.

In the present chapter, we present an efficient and systematic techniques for nanoscale DG MOSFETs modeling, where simple and accurate device models can be automatically achieved from a computational process to maximally reduce human trial and error efforts.

Since the inversion charge is one of the key parameters defining electron mobility, charge concentration and drain current models for nanoscale DG MOSFETs, their evaluations are of prime importance for reliability application and circuit performance improvement for nanoscale electronic devices.

The developed models should be able, including quantum effect (QE) and short channel effect (SCE), to correctly represent the Current-Voltage characteristics of the nanoscale device, and effectively capture the electrical behavior of the device due to process variations. In addition, the model should be formulated such that it can be conveniently incorporated into existing circuit simulators for high-level circuit simulation and yield design. Unlike the numerical models used to study the nanoscale structure, such as 2-D numerical Non-Equilibrium Green's Function (NEGF) formalism, which is complicated and requires a high computation time and storage memory, the proposed approaches, Genetic Algorithm (GA) and Fuzzy logic(FL), have lower complexity and lower simulation time, which are the prerequisite of the nanoelectronic circuit simulators.

3.2 Quantum inversion charge model

The salient feature of a DG MOSFET is the thin silicon layer which is beneficial to device scaling. Quantum effects arise due to the confinement of electron motion in the thin silicon film in contrast to the confinement by the surface potential (or field) in bulk devices. To obtain the quantum electrical characteristics of a DG MOS structure, one needs to solve the Poisson equation given by,

$$\Delta\phi(x,y) = \frac{qn_i}{\varepsilon_{si}} e^{(\phi(x,y)-\phi_F)/V_t} \tag{3.1}$$

where q is the electron charge, n_i is the silicon intrinsic concentration,ε_{si} is the silicon permittivity, V_t is the thermal voltage, $\phi(x, y)$ represents the 2-D electrostatic potential distribution in the channel region, and ϕ_F is the non-equilibrium quasi- Fermi level referenced to the Fermi level in the source, satisfying the following boundary conditions,

$$\phi_F(0, y) = 0 \tag{3.2a}$$

$$\phi_F(L, y) = V_{ds} \tag{3.2b}$$

V_{ds} being the drain voltage, ϕ_F can be approximated by a second order polynomial function,using [67] as,

$$\phi_F(x) = \frac{V_{ds}}{L^2}x^2 \tag{3.3}$$

Taur in [134], has introduced a long channel model for the inversion charge of undoped DG MOSFET devices based on a 1-D analytical solution of Poisson equation incorporating only the mobile charge term as,

$$Q_i = C_{ox}\left[-2C_{ox}\frac{V_t^2}{Q_0} + \sqrt{\left(2C_{ox}\frac{V_t^2}{Q_0}\right)^2 + 4V_t^2 \ln\left(1 + e^{\frac{V_{gs}-V_{fb}-\phi_F+V_{th}}{2V_t}}\right)}\right] \tag{3.4}$$

where $C_{ox} = {}^{\varepsilon_{ox}}/_{t_{ox}}$ represents the oxide capacitance per unit area, V_{fb} is the flat band voltage, V_{th} is the threshold voltage, and Q_0 is the charge coefficient which are given [134] by $V_{th} = V_t ln\left(\frac{16V_t \times \varepsilon_{si}}{q \times n_i \times t_{si}^2}\right)$, $Q_0 = (8V_t\varepsilon_{si}/t_{si})$. For silicon films thinner than 5 nm, quantum confinement should be considered; it leads to a reduction of the channel charge density and an increase of the threshold voltage. From Eq. (3.4), we can see that an accurate model of the inversion charge depends mainly on the oxide capacitance and threshold voltage. Therefore, in order to develop an accurate charge model, new oxide capacitance and threshold voltage models, which include the quantum effects, should be introduced

in Eq. (3.4).

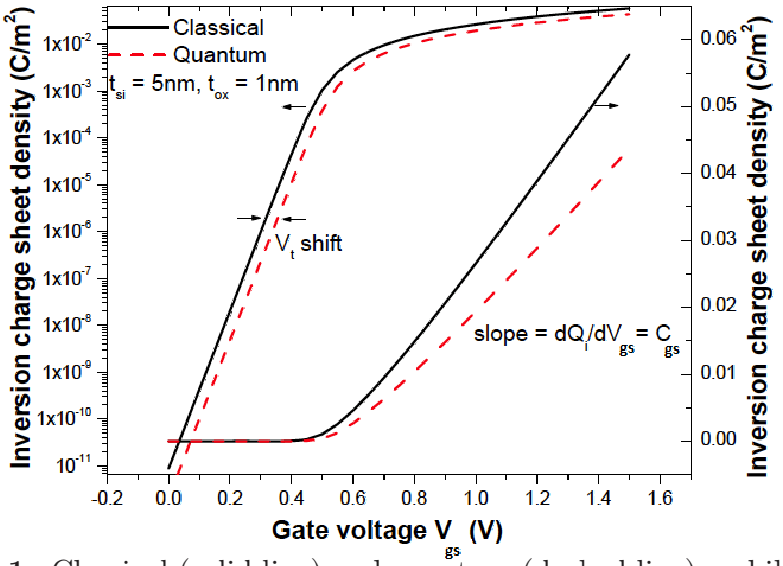


Figure 3.1: Classical (solid line) and quantum (dashed line) mobile charge sheet density Q_i of symmetric DG MOSFETs in both linear (right) and logarithmic (left) scales versus gate voltage.

Figure 3.1 illustrates the definition of the threshold voltage V_{th} shift due to quantum effects and the gate capacitance C_{gs} as well. The V_{th} shift represents the parallel shift of Q_i-V_{gs} curves at subthreshold region with respect to the classical curve at the same inversion charge sheet density Q_i. On the other hand, C_{gs} degradation is the difference between the both slopes of Q_i-V_{gs} classical and quantum curves at linear region. In order to estimate the inversion charge behavior including quantum effect, it is required to develop a new analytical model with quantum corrections based on the classical model. In other word, two distinctive quantum effects, threshold voltage shift as a function of the silicon film thickness and the quantum degradation of inversion layer capacitance, should be implemented as effective quantum threshold voltage and equivalent quantum oxide capacitance respectively.

3.3 Quantum correction using Genetic Algorithm

3.3.1 DG MOSFET: Design description

The basic structure of the DG MOSFET investigated in this Chapter is shown in Figure 3.2. As MOSFET feature size moves into nanoscale regime, canonical carrier transport theories are no longer capable of describing carrier transport accurately. The canonical theories are basically derived from the Boltzmann transport equation (BTE), with more or fewer approximations being made [128]. These models focus on scattering-dominant transport, which typically occurs in long channel devices. However, transistors operate in ballistic or quasi-ballistic transport regime. Simulations using conventional models may either under predict or over predict the electrical device behavior [128–130]. Figure 3.2 shows the cross-sectional structure of the DG MOSFET investigated in this chapter.

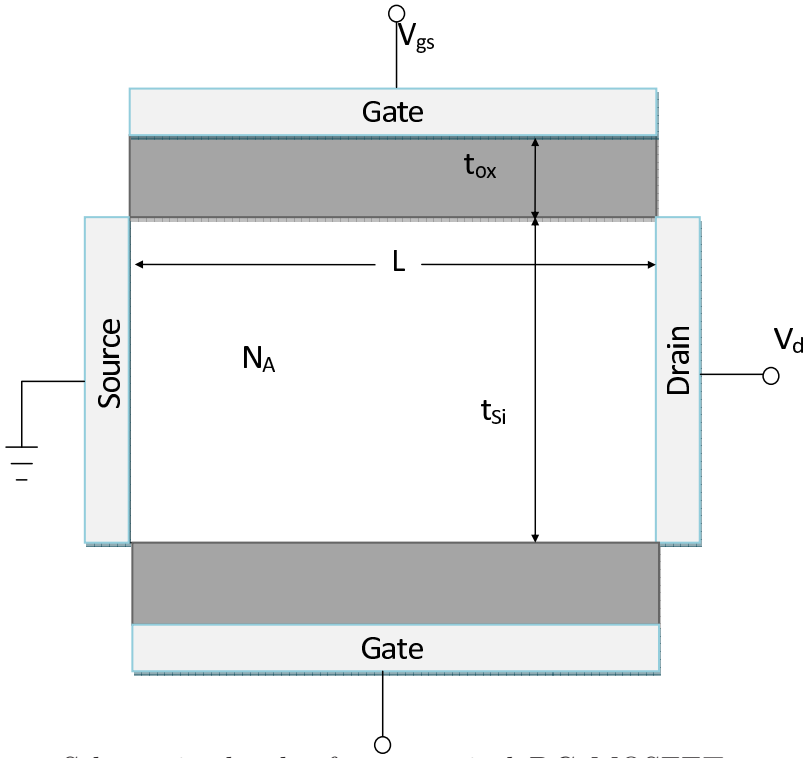


Figure 3.2: Schematic sketch of symmetrical DG MOSFET structure investigated in this study with (channel doping $N_A = 10^{15} cm^{-3}$, t_{si} represents silicon thickness and t_{ox} is the oxide thickness).

The substrate is p-type Silicon with a thin channel thickness, and doped concentration is $10^{15}cm^{-3}$. The source and drain are of n-type with doped concentration of $10^{20}cm^{-3}$. The design of an optimal DG MOSFET will require new insights into the underlying physics, especially electrons transport in the channel region. Quantum-mechanical confinement of electrons significantly affects the electrical characteristics of highly scaled MOSFETs.

Therefore, an analytical DG MOSFETs modeling with arbitrary Si-film thickness (less than 5nm) is needed for physical insight as well as for a reliable device model. To simulate nanoscale DG MOSFETs, the Non-Equilibrium Green's Function Formalism (NEGF) provides one of the best frameworks available [125, 131].

However, Artificial Intelligence techniques (AI) have been recognized as an important approach for the semiconductor device computer-aided design area in addressing the growing challenges of designing next generation of nanoelectronic devices, circuits, and systems [124, 129]. The AI-based methods represent important steps towards automating the device modeling process. However, because the evolutionary techniques have to learn the device behavior from numerical or experimental databases without using existing device physical models like: drift-diffusion (D-D), hydrodynamic and gradual-channel approximation (HGCA), which make the reliability of the AI-based model low and questionable.

In the next point, we present alternative approaches based on evolutionary and intelligent techniques to achieve reliable, accurate and simple compact models by the concept of quantum correction for nanoelectronics circuit simulations.

3.3.2 Drain current model

One of the approaches for mapping between the accurate and approximate models is to correct approximate model parameters so that simulation results based on approximate model, mimic the accurate simulation results. Based on the efficiency proven by NEGF formalism for the modeling of nanoscale DG MOSFETs and the difficulty imposed at the

moment by the constraints of the nanotechnology (sub-50nm) to form an experimental database [124, 129], we have used the NEGF formalism as accurate model.

The gradual channel approximation (GCA), which assumes that the quasi Fermi potential stays constant along the direction perpendicular to the channel, is used in our study as an approximated model. Accurate models for long channel double-gate MOSFETs [130], [57, 85, 135] have been recently developed using the conventional approaches, showing good agreement with 2-D numerical simulations.

The inclusion of short-channel effects SCEs in undoped multiple gate MOS models, using physical equations and without decreasing the order of continuity of the devices, is still a modeling challenge. For devices with channel lengths shorter than 50 nm, the drift-diffusion mechanism may not be the dominant transport mechanism. Ballistic or quasiballistic transport may occur. Adequate models for nanoscale devices must consider the balllistic or quasi-ballistic regime [136, 137]. The drain current of a symmetrical DG MOSFET assuming gradual channel approximation is given by

$$I_{DS} = q\mu_{eff}(x,y)n(x,y)\frac{d\phi_F(x)}{dx} = q\mu_{eff}(x,y)n_i e^{[\phi(x,y)-\phi_F]}\frac{d\phi_F(x)}{dx} \tag{3.5}$$

where μ_{eff} is the effective electron mobility, $n(x,y)$ represents the free charge concentration in the channel region.

3.3.3 Modeling methodology

In GA, variables of a problem are represented as genes in a chromosome, and the chromosomes in the population are evaluated according to their fitness values. Given a random initial population GA operates in cycles called generations. The problem to be solved is defined in terms of an evaluation function (fitness function), which is used to evaluate the chromosomes. A chromosome evaluated as having a high fitness value is likely to be a good solution of the problem. Implementation of GA requires determination of six fundamental issues: chromosome representation, selection function, the genetic operators, initialization, and evaluation function [92, 138].

As it is shown, the parameters $\mu_{eff}(x,y)$,$n(x,y)$ and $\phi_F(x)$ in Eq. (3.5) are proper for this purpose. In our approach, Genetic Algorithm (GA) generates the optimal and corrected distribution of these parameters, which are inserted in the approximate model (GCA) to produce simulation results close to the accurate model (NEGF). Figure 3.3 shows the proposed GA-based approach block diagram.

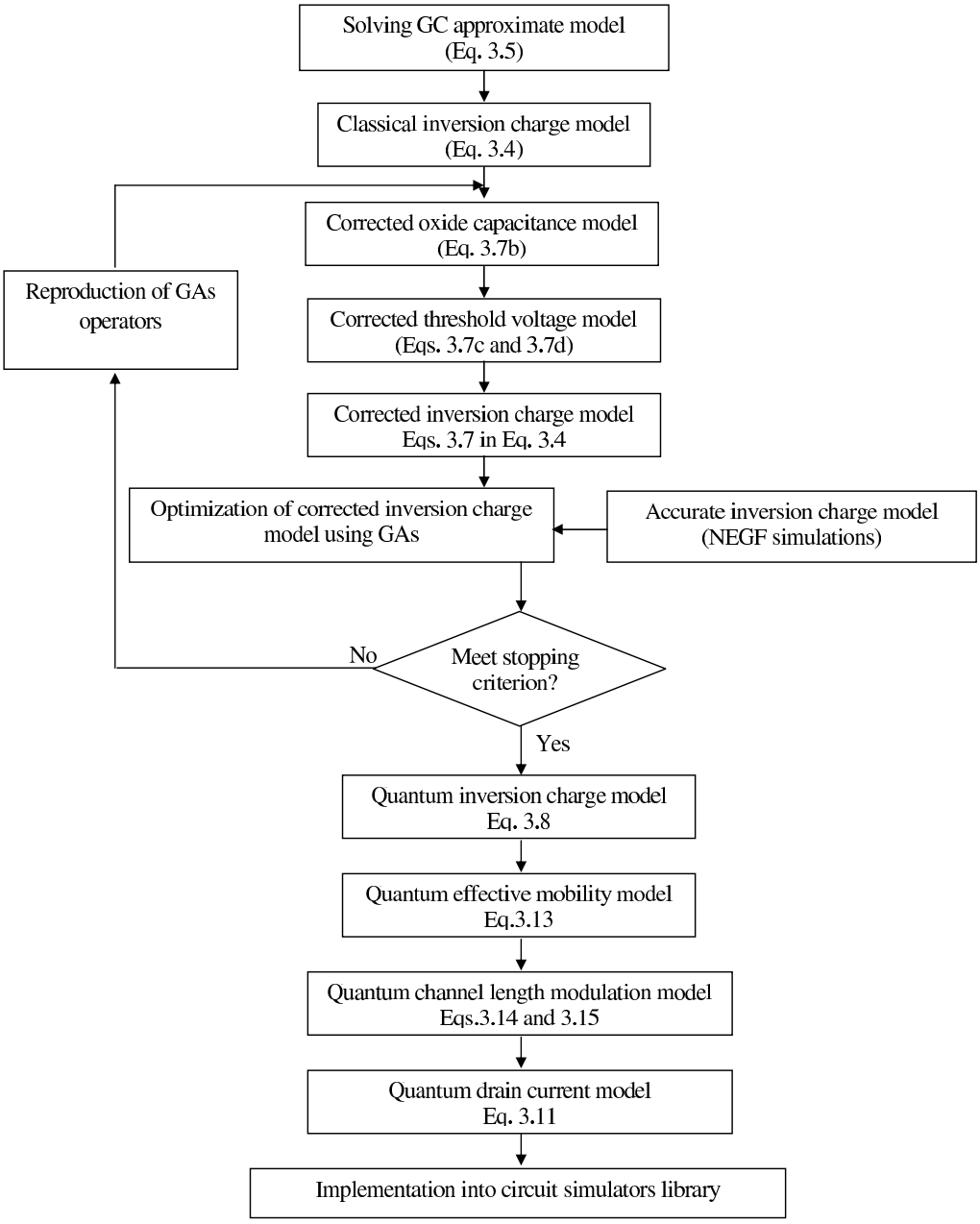


Figure 3.3: Flowchart of our charge-based computation approach

According to Eq. (3.1) and Eq. (3.5), in a semiconductor device, basic variables are electron distribution (n), potential distribution (ϕ), quasi Fermi potential (ϕ_F) and the effective electron mobility (μ_{eff}). Therefore, these electrical parameters distributions have been used for training and optimisation of GA to generate optimized and accurate analytical model to study the nanoscale DG MOSFETs. In the present study, a mean squared error of each parameter, *Par*, the generation is taken as the fitness function,

$$f = \frac{1}{M} \sum_{V_{ds}} \sum_{V_{gs}} \sum_{t_{si}} \sum_{t_{ox}} \sum_{L} \left[\frac{Par_{NUM} - Par_{GA-ANA}}{Par_{NUM}} \right]^2 \tag{3.6}$$

where f is the fitness value, Par_{GA-ANA} is the predicted parameter based on GA and analytical computations; Par_{NUM} represents the target function (numerical results based on 2-D numerical, NEGF, simulation); and M represents the number of samples (database size).

It is aimed to minimize this fitness function, for each parameter, in order to develop accurate simple compact drain current model for nanoscale DG MOSFETs. In this context, new oxide capacitance C_{oxq} and threshold voltage V_{thq} expressions that include quantum effects should be implemented in Eq. (3.4).

The quantum oxide capacitance C_{oxq} can be defined as the series combination of the C_{ox} and the inversion capacitance par unit area. It is given by the following expressions:

$$C_{oxq} = \frac{C_{ox}}{1 + C_{ox}\frac{Y_I}{\varepsilon_s}} \tag{3.7a}$$

$$C_{oxq} = \frac{C_{ox}}{1 + \xi_1 C_{ox} t_{si}} \tag{3.7b}$$

$$V_{thq} = V_{th} + \delta V_{thq} \tag{3.7c}$$

$$\delta V_{thq} = \frac{\xi_2}{t_{si}^2} \tag{3.7d}$$

where Y_I represents the centroid. This latter is mainly depends on the applied gate voltage and the channel thickness. In [118], the inversion layer at the centroid was modeled by assuming that the centroid was at the quarter of the channel thickness. If we get $Y_I/\varepsilon_s = \xi_1 t_{si}$, Eq. (3.7a) can be rewritten as Eq. (3.7b)

The variation of the quantum threshold voltage, V_{Tq} , as function of channel thickness can be given in Eq. (3.7c), with δV_{thq} represents the threshold voltage shift due to the quantum effects, and it is given by Eq. (3.7d). ξ_1 and ξ_2 are fitting parameters which will be calculated using GAs as it is shown in figure 3.3.

Now, substituting the quantum oxide capacitance, C_{oxq} , Eq. (3.7b) and the quantum threshold voltage, V_{Tq} ,Eq. (3.7c) into Eq. (3.4), a new inversion charge model can be given as,

$$Q_{iq} = C_{oxq}\left[-2C_{oxq}\frac{V_{th}^2}{Q_0} + \sqrt{\left(2C_{oxq}\frac{V_{th}^2}{Q_0}\right)^2 + 4V_{th}^2 ln\left(1 + e^{\frac{V_{gs}-V_{fb}-\phi_F+V_T+\delta V_{Tq}}{2V_{th}}}\right)}\right] \quad (3.8)$$

The fitting parameters (ξ_1 and ξ_2) in Eq. (3.8) can be extracted using Eq. (3.6).

3.3.4 Results and discussion

For the purpose of GA-based optimization of Eq. (3.8), routines and programs for GA computation were developed using MATLAB 7.2 and all simulations are carried out on a Pentium IV, 3GHz, 1GB RAM computer. For the implementation of the GA, tournament selection is employed which selects each parent by choosing individuals at random, and then choosing the best individual out of that set to be a parent.

Scattered crossover creates a random binary vector. It then selects the genes where the vector is unity from the first parent, and the genes where the vector is zero from the second parent, and combines the genes to form the child. In our case, the crossover rate and the mutation rate are equal to 0.8 and 0.2 respectively.

An optimization process was performed for 20 population size and maximum number of generations equal to 100, for which stabilization of the fitness function was obtained.

The obtained results of the proposed approach are presented for the studied device in two-dimensional space. The transistor length is 20 nm with 20 mesh points and its thickness is 5nm with 5 mesh points. Therefore, simulation data are 2D matrixes of 20×5. The quantum simulations, self-consistent computations, have been carried out using 2D Silvaco and nanoMOS2.5 numerical simulator tools [139, 140].

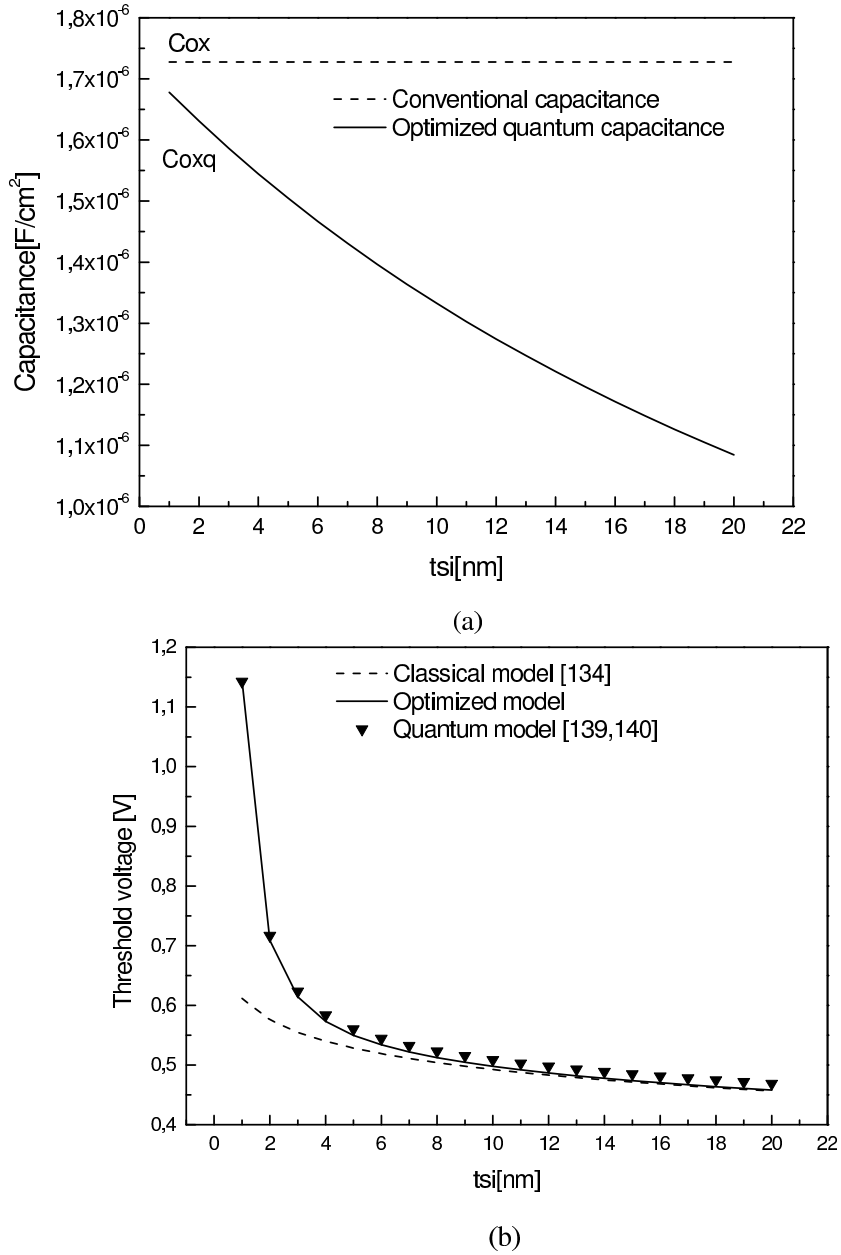


Figure 3.4: (a) Classical and optimized quantum oxide capacitance versus film thickness (b) Classical and quantum threshold voltage versus film thickness

Figures 3.4(a) and 3.4(b) show the variation of the optimized quantum oxide capacitance and the optimized quantum threshold voltage, as function of channel thickness. As it is shown in Figure 3.4(a), the conventional capacitance C_{ox} doesn't change with thikness. However, the behavior of the optimized quantum capacitance tends to decrease with respect to the silicon thickness according to Eq. (3.7b). In Figure 3.4(b), a good agreement between our optimized threshold voltage model and numerical model was obtained.

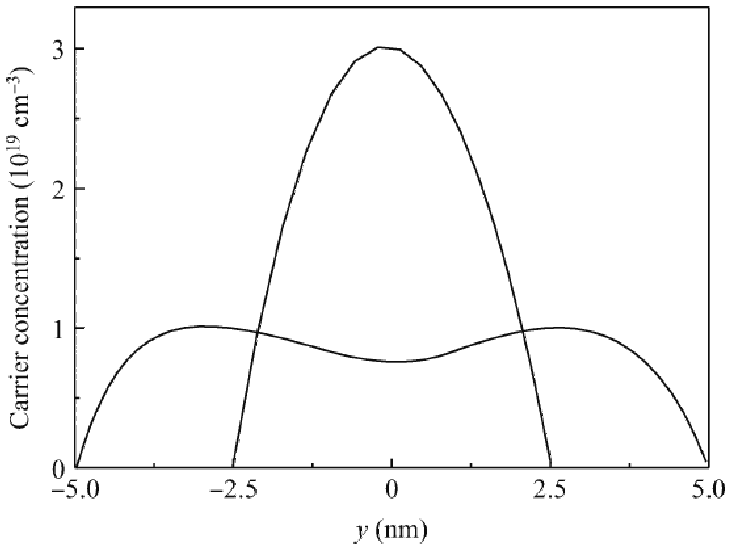


Figure 3.5: Influence of the film thickness on the electron concentration distribution

Figure 3.5 presents the influence of the film thickness on the electron concentration distribution, in which the quantum distribution of charge is obtained by coupling Schrödinger equation to Poisson's equation. For the device with a very thick body, the carriers flow near the interfaces $Si - SiO_2$. However, the carrier profile is modified for thinner devices less than $5nm$, where the most of the carriers flow in the middle of the film, not at the interfaces [118].

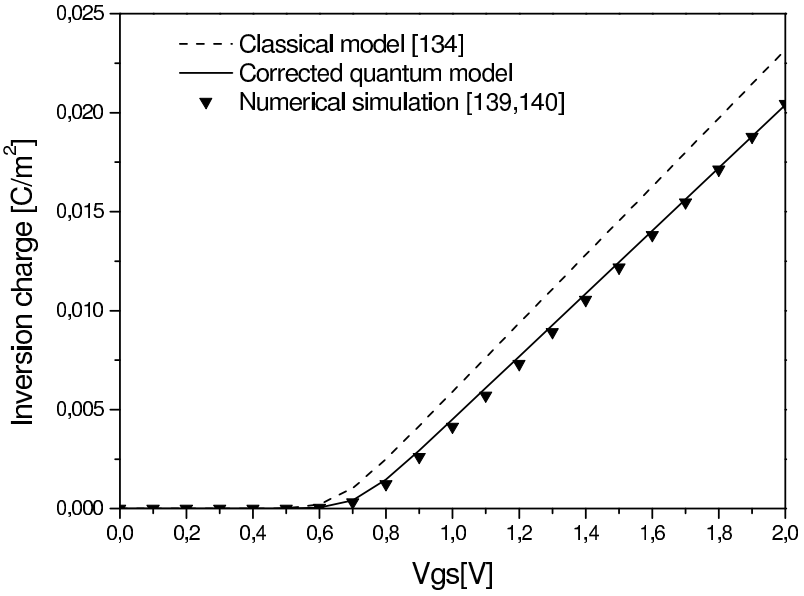


Figure 3.6: Classical and corrected quantum inversion charge versus gate-source voltage

Figure 3.6 shows the inversion charge density versus the gate-source voltage for nanoscale undoped DG MOSFET. The increase and the shift of the inversion charge density due to the QM effect are well predicted by our model, given in Eq. (3.8). For below threshold voltage and in the subthreshold regime, quantum and classical inversion charge densities are close to each other. However, for a high gate-source voltage, the electrons are strongly confined in the direction perpendicular to the $Si - SiO_2$ interface due to the increasing influence of the vertical electric field component.

As shown in Figure 3.6, an excellent fit was found between our inversion charge model and the numerical Poisson-Schrödinger self-consistent (NEGF) simulation.

3.4 Implementation of the quantum effects in the compact drain current model

The drain current for DG MOSFET, including quantum effects, can be calculated from:

$$I_{dsq} = \mu_{eff} \frac{W}{L} \int_{V_s}^{V_d} Q_{iq}(\phi_F) d\phi_F \tag{3.9}$$

where W is the channel width. Using Eq. (3.8) and Eq. (3.9) and after some mathematical manipulations, the variation of the channel voltage as function of the inversion charge can be written as,

$$d\phi_F = -\frac{dQ_{iq}}{2dC_{oxq}} - V_t \left(\frac{dQ_{iq}}{Q_{iq}} + \frac{dQ_{iq}}{Q_{iq} + 2Q_0} \right) \tag{3.10}$$

Writing $d\phi_F$ as a function of Q and dQ in Eq. (3.9), and integrating between Q_{iqs} and Q_{iqd} , we obtain:

$$I_{dsq} = \mu_{eff} \frac{W}{L} \left[\frac{Q_{iqs}^2 - Q_{iqd}^2}{C_{oxq}} + 4V_t(Q_{iqs} - Q_{iqd}) + V_t Q_0 \ln \left(\frac{Q_0 + 2Q_{iqd}}{Q_0 + 2Q_{iqs}} \right) \right] \tag{3.11}$$

The charge densities at the source and the drain ends of the transistor Q_{iqs} and Q_{iqd} are respectively:

$$Q_{iqs} = Q_{iq}(x = 0) = Q_{iq}(\phi_F = 0) \tag{3.12a}$$

$$Q_{iqd} = Q_{iq}(x = L) = Q_{iq}(\phi_F = V_{ds}) \tag{3.12b}$$

For the transistor with a very thick body, the low-field mobility μ_0, does not change with thickness. However, the behavior of the effective electron mobility in very thin channel films, t_{si} less than 10nm, tends to decrease [141]. In this case, the in-depth average values of the electron mobility and the effective electric field weighted by the electron distribution are given [142] by

$$\mu_{eff} \approx \frac{\mu_0}{1 + \left(\frac{E_{eff}}{E_0} \right)^{\delta}} = \frac{1}{1 + \eta \frac{Q_{iq}}{2\varepsilon_{si} E_0}} \quad \text{with} \quad E_{eff} = \frac{Q_{iq}}{2\varepsilon_{si}} \tag{3.13}$$

where E_0 represents an applied eclectic field, which is considered in our study as fit-

ting parameter. This latter is calculated using the GAs (Figure. 3.3), ε_{si} is the silicon permittivity and η is an empirical fitting parameter $\eta = 0.001$.

For an applied drain-source voltages, more than the saturation voltage (V_{sat}), the velocity is practically at its saturation value in a region near to the drain end. Inside this region, channel length modulation, region of length ΔL, inversion charge is relatively constant, and the conventional transport equations (like: BTE, GCA, D-D) break down. If we apply the 2D Poisson equation in the channel region to study the channel length modulation [143], then ΔL can be obtained as,

$$\Delta L = \lambda \ln \left[\frac{\phi_d + \sqrt{\phi_d^2 - \phi_{dsat}^2 + \left(\lambda \frac{\theta v_{sat}}{\mu_{eff}}\right)^2}}{\phi_{dsat} + \lambda \frac{\theta v_{sat}}{\mu_{eff}}} \right] \tag{3.14}$$

where ϕ_d is drain channel voltage, ϕ_{dsat} represents the saturation drain channel voltage, λ is the natural length that depends only on the device structure, v_{sat} represents the electron saturation velocity near the drain end and θ is a fitting parameter where $\theta = 2$. (the parameters of Eq. (3.14) are well defined in Ref. [143]). So, for $V_{ds} \leq V_{sat}$ the channel length modulation trends to zero, we can write the effective channel length as,

$$L_{eff} = L - \Delta L \tag{3.15}$$

In the drain current compact model Eq. (3.11), we replace channel length L by the effective channel length value Eq. (3.15) in order to include the channel length modulation effect.

Figure 3.7 presents comparisons between target data (NEGF) and drain current data calculated by our model, Eq. (3.11), for both nanoscale DG MOSFET designs. We can see that the proposed model provides a good agreement for a very wide interval of geometrical and physical parameters for the both investigated nanoscale DG MOSFETs in comparison with numerical simulations. Hence, the proposed compact model can be used to predict other combinations of input variables (V_{gs}, V_{ds}, L, etc.) in full range (see chapter 4).

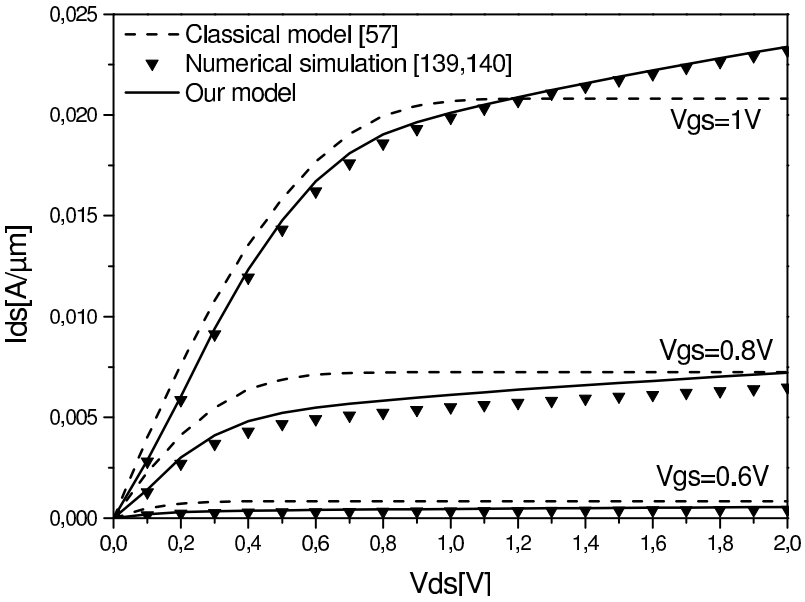


Figure 3.7: Numerical (symbols) and calculated (solid lines) drain current vs. drain voltage

This last observation shows the applicability of GA technique to study the nanoscale DG MOSFETs using a long channel compact current model. The forgoing results show that our model makes it feasible to include quantum effects accurately and generally in nanoelectronic device simulation.

3.5 Electron mobility model using Fuzzy logic computation

The FL-based modeling can provide an effective representation of complex non-linear systems in terms of fuzzy sets and fuzzy inference [144]. Several published works [144–146] offer extensive explanations to the fundamentals of FL and its wide range of applications. The input-output behavior of a fuzzy system is programmable using linguistic information in the form of IF (preconditions) THEN (postconditions) rules, describing an approximate or qualitative knowledge of an observed process. FL is a superset of conventional Boolean logic that has been extended to include the concept of partial truth-truth-values between

'completely true' and 'completely false'. More details about this method is illustrated in Chapter 2. Due to its simple mechanism and high performance for behavior modeling, FL can be applied to study the electrons mobility behavior for nanoscale transistors, which is the main objective of this work.

3.5.1 Modeling methodology

Based on the efficiency proven by NEGF for the modeling of nanoscale DG MOSFETs, we have used the NEGF formalism to form the database which will be used to learn our FL-based model as it is shown in Figure 3.8.

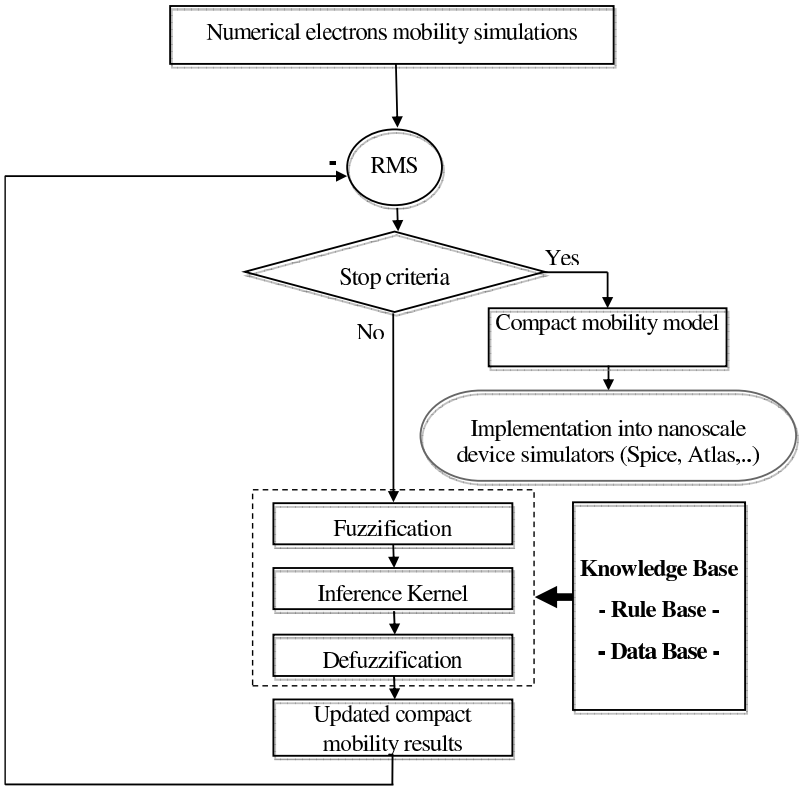


Figure 3.8: Flowchart of our FL-based electrons mobility computation approach

The first step of our approach consists of the compact analytical electrons mobility model for conventional long channel DG MOSFETs. For the long channel transistor with thick silicon body, the low-field mobility,μ_0, does not change with thickness and therefore,

the study of the electron transport becomes in this case simple. However, the behavior of the effective electron mobility for nanoscale transistors tends to decrease [141]. In this case, the in-depth average values of the electron mobility and the effective electric field weighted by the electron distribution (see Eq. (3.13)) mainly depend on the inversion charge distribution in the channel. In this context, based on the inversion charge model proposed by Taur et al [134], a new extended model, Q_{iq}, (see Eq. (3.8)) called the corrected inversion charge model of undoped DG MOSFET, in which the quantum effects have been introduced as fitting parameters which will be determined using our FL-based approach as it is shown in Figure 3.8.

From Eq. (3.13), an accurate modeling of the inversion charge concentration leads to an accurate electrons mobility computation. So, in our FL-based computation we focus to study the inversion charge behavior.

To define the fuzzy associative memory, we need some knowledge about how each of these parameters affects the mobility behavior:

- V_{Tq} shifts the whole $Q_{iq} - V_{gs}$ curve.
- ξ_1 describes the curvature of $Q_{iq} - V_{gs}$ and provides a scale factor.
- ξ_2 provides a scale factor.

Based on the effect of each parameter on the $Q_{iq} - V_{gs}$ characteristics, we can define the following rules in order to develop our knowledge Base (Figure 3.8):

Algorithm 2 FL Rules

If (the calculated curve $Q_{iq} - V_{gs}$ is to the right of the numerical data) then

decrease V_{thq}

else

increase V_{thq}

If (the calculated curve $Q_{iq} - V_{gs}$ is more curved than the numerical data) then

decrease ξ_1

else

increase ξ_1

If (the calculated curve $Q_{iq} - V_{gs}$ is over the numerical data) then

decrease ξ_2

else

increase ξ_2

In order to implement the above rules, we have used the triangular fuzzy sets, while defuzzification is carried out through the method of centre of area. The input and output parameters are normalized by using the numerical database as reference. The linguistic variables chosen for this FL-based model are the principal and secondary errors (Er_P and Er_S) for each parameter of the compact electron mobility model. These errors can be calculated, for each parameter, from:

$$Er\_P(\xi_1) = \frac{Q_{iq-N}(\mathrm{V_{gs}} \approx \mathrm{V_{thq}})}{Max(Q_{iq-N})} - \frac{Q_{iq-F}(\mathrm{V_{gs}} \approx \mathrm{V_{thq}})}{Max(Q_{iq-N})} \tag{3.16a}$$

$$Er\_P(\xi_2) = \frac{Q_{iq-N}(\mathrm{V_{GS}} \approx \mathrm{V_{sat}})}{Max(Q_{iq-N})} - \frac{Q_{iq-F}(\mathrm{V_{GS}} \approx \mathrm{V_{sat}})}{Max(Q_{iq-N})} \tag{3.16b}$$

$$Er\_S(\xi_1, \xi_2) = \frac{Q_{iq-N}(\mathrm{V_{GS}} \approx \mathrm{V_M})}{Max(Q_{iq-N})} - \frac{Q_{iq-F}(\mathrm{V_{GS}} \approx \mathrm{V_M})}{Max(Q_{iq-N})} \tag{3.16c}$$

where Q_{iq-N} and Q_{iq-P} represent the 2D numerical inversion charge simulation and FL-based inversion charge model, respectively. V_M is the medium voltage given by $V_M = \frac{V_{thq}+V_{DD}}{2}$ with represents the supply voltage.

The both errors are the input linguistic variables and the inversion charge is the final

output linguistic variable. In this work, the principal error of each parameter represents the drain current deviation affected, only, by the main parameter, and the secondary one is the drain current deviation affected by a combination of several parameters (mutual effect).

In this approach, we design a fuzzy inference system based on the past known behavior of a target system. The fuzzy system is then expected to be able to reproduce the behavior of the target system (Figure 3.8). Each of the input and output fuzzy variables is assigned seven linguistic fuzzy subsets varying from negative large (NL) to positive large (PL). Each subset is associated with a triangular membership function to form a set of seven membership functions for each fuzzy variable. The linguistic terms chosen for this controller are seven. They are negative large (NL), negative medium (NM), negative small (NS), zero (Z), positive small (PS), positive medium (PM) and positive large (PL). After assigning the input, output ranges to define fuzzy sets, mapping each of the possible five input fuzzy values of principal error(Er_P), three input fuzzy values of secondary error (Er_S) to the seven output fuzzy values is carried out through a rule base. Table 3.1 shows the fuzzy associate memory table of the fuzzy V_{Tq}, ξ_1 and ξ_2 controllers.

Table 3.1: Fuzzy associate memory table (FAM) for the fuzzy , V_{thq}, ξ_1 and ξ_2 controllers.

		Principal error Er_P					
			NL	NM	Z	PM	PL
Secondary	error Er_S	N	NL	NM	NS	PS	PM
		Z	NM	NM	Z	PM	PM
		P	NM	NS	PS	PM	PL

3.5.2 Results and discussion

From Figure 3.8, the computation will iterate from an initial point until a stopping condition is found. For each iteration, new values for the parameters will be estimated by

the fuzzy calculator. The global RMS (Root Mean Square) error between the numerical and the calculated results, considering all points on the database, will be updated. In our case, we have used a stopping condition of global RMS error less than a 5%.

Figure 3.9 shows good agreement between numerical and predicted results of the electron mobility for the investigated nanoscale DG MOSFETs. It is to note that our simulations were carried out for a wide range of nanoscale DG MOSFET parameters (geometrical and electrical parameters) in order to ensure the applicability of the proposed FL-based model to study the electron mobility for the nanoscale DG MOSFETs.

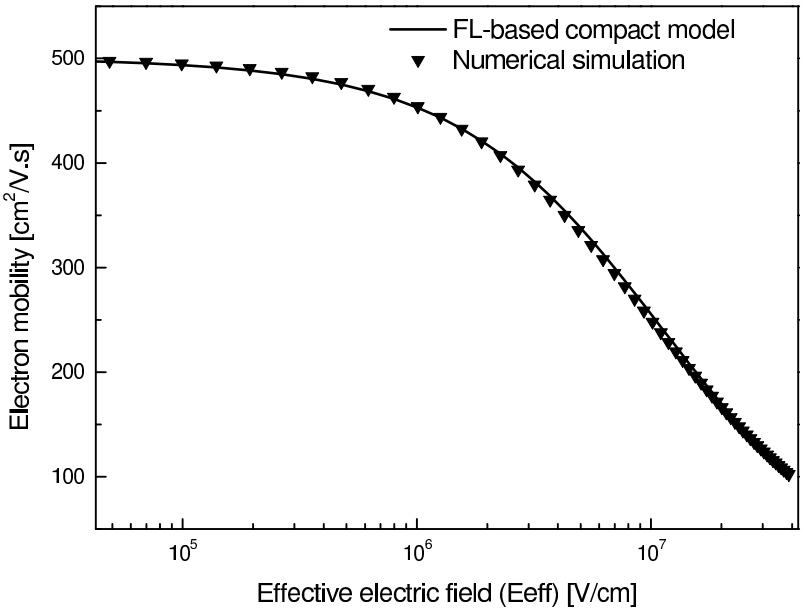


Figure 3.9: Electrons mobility characteristic calculated from the FL-based compact model (solid lines), compared with numerical simulations (symbols) for $t_{si} = 5$nm and $t_{ox} = 1.5$nm

Figure 3.10 shows the evolution of the Fuzzy logic parameters versus the simulation cycle times using the computer (P.IV-3GHz). It is clearly shown that the convergence point of the Fuzzy computation process can be achieved for 4×10^4 cycle times (several seconds), for which the stability of the generated FL parameters was found. This result makes the fuzzy logic-based approach as a powerful tool to study the nanoscale devices.

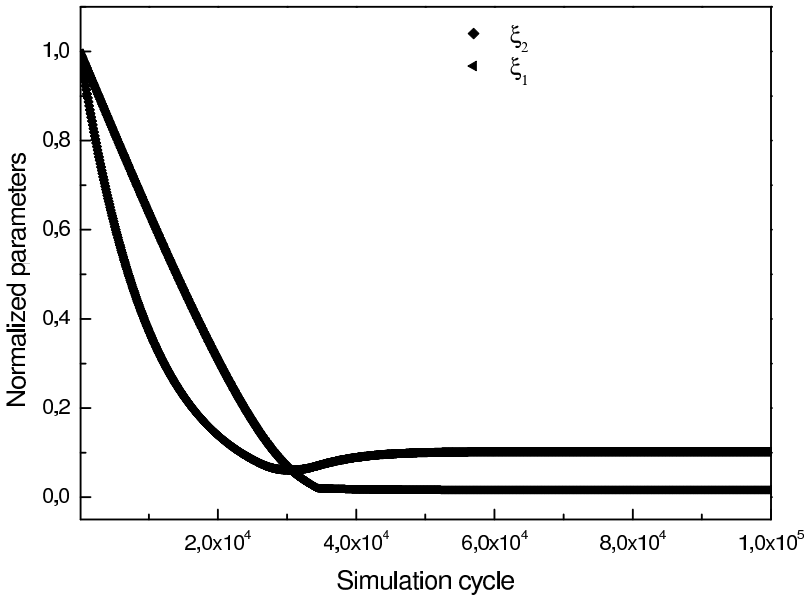


Figure 3.10: Evolution of the Fuzzy logic parameters versus the simulation cycle times

3.5.3 Comparison between modeling approaches

Table 3.2 gives a comparison of the effectiveness and the CPU (central processing unit) time requirements, for the simulation of the nanoscale DG MOSFETs with various approaches where in our proposed approaches (FL and GA-based method), computation time should be compared to the orders of magnitude increase in computation time for more rigorous nanoscale DG MOSFET models, such as those based on the manual parameters computation and those obtained numerically [140].

In order to show a comparison between our proposed models and other approaches in the field of nano-CMOS circuits simulation, table 3.2 shows that the neural method (AI-based method) is a behavioral approach of modeling where the neural model is given as a black-box and defined by three different blocks: input vector-weight matrix and activation function-output vector, in addition, the analytical compact models proposed by V. Hariharan et al [128] and Q. Chen [126] et al are more complex, includes several fitting parameters, does not take into account the very thin channel effects [128] and uses fewer approximations [126, 128].

Contrary, in our proposed approaches, the developed models are accurate, simple and analytical closed expressions that include the channel length modulation, the very thin channel effects and two global optimized fitting parameters (ξ_1 and ξ_2). The obtained results can be explained by the fact that the GA and FL-based techniques are characterized as computational models based on parallel distributed processing of data. Therefore, the GA and FL computation provides practical insight into carrier transport modeling in nanoscale devices without the uncertain accuracy or meticulous tuning effort that face more rigorous DG MOSFET nanoscale models. The GA and FL-based modeling is a step towards a new generation of simulation tools that will allow device and material engineers to explore new classes of electronic devices.

Table 3.2: Comparison between the various approaches of modeling for nano-DG MOSFETs

Approach	**Model**	**CPU time (s)**	**Effectiveness of the approach**
Numerical simulations NEGF [140]	Numerical	Hours	Accurate/ slow
Manual parameters adjustment	Empirical	Hours/days	Less accurate/ very slow
Analytical compact model [126, 128]	Analytical	several minutes	Less accurate/ fast
AI- based model [124]	Behavioral	several seconds	Accurate/ fast
Our FL-based model [147]	Analytical	several seconds	Accurate/ fast
Our GA-based model [148]	Analytical	several seconds	Accurate/ fast

3.6 Sammary

In this chapter, new analytical models that include quantum and channel length modulation effects for undoped nanoscale DG MOSFETs are presented. The 2-D self-consistent computation and Gradual Channel approaches are used as accurate and approximate models, respectively. In the proposed approaches, the Genetic Algorithm and Fuzzy Logic techniques are used for mapping parameters and generate the optimal parameters distribution in a relatively short time, with no need for user intervention during the search. These parameters are inserted into the approximated model (GCA) which is capable to

produce simulation results close to the accurate 2-D numerical simulation.

The presented analytical models for threshold voltage, threshold voltage shift, quantum oxide capacitance, inversion charge density, electron mobility and drain current overcome problems using classical models. The proposed models have several advantages such as accuracy, simplicity and applicability for wide device dimension range. It is to note that the proposed models can be extended to include the hot carrier and degradation effects. However, new models and analytical expressions should be developed in this case.

The comparisons between numerical simulations and our compact model results have indicated that the proposed closed analytical form is particularly suitable to be incorporated in electronic device simulators to study the nanoscale CMOS circuits.

The text of Chapter 3, in part, is a reprint of the material as it appears in "A compact charge-based model to study the nanoscale undoped double gate MOSFETs for nanoelectronic circuit design using genetic algorithms" by T. Bendib, F. Djeffal, and D. Arar, Journal of Semiconductors, IOP Publishing, 2013. The dissertation author was the primary investigator and author of this paper.

The text of Chapter 3, in part, is a reprint of the material as it appears in "Fuzzy-logic-based approach to study the electrons mobility in nanoscale double gate MOSFETs" by T. Bendib, F. Djeffal, D. Arar, Z. Dibi, and A. Ferdi, IOP Conference Series: Materials Science and Engineering, IOP Publishing, 2012. The dissertation author was the primary investigator and author of this paper.

Chapter 4

Design and optimization of DGMOSFETs for nanoscale circuit applications

Contents

4.1 Introduction

The Double Gate (DG) MOSFET is considered as one of the most promising devices for downscaling below 50nm [53,123,149]. Due to the Double Gate design, the gates gain increased electrostatic control of the channel and short-channel effects can be drastically suppressed. Apart from the benefit of allowing a shorter channel, the DG MOSFETs can achieve a higher packing density due to their enhanced current drive compared to conventional MOSFETs.

The downscaling of device dimensions has been the primary factor leading to improvements in Integrated Circuits (CIs) performance and cost, which contributes to the rapid growth of the semiconductor industry. However, even in DG MOSFET devices, small signal parameters and Short Channel Effects (SCEs), such as the threshold voltage roll-off, the DIBL and the subthreshold swing degradation, cannot be neglected for channel lengths below 100nm [53,126,149].

Several works have reported that the novel structures for DG MOSFETs with high performance and scalability can be used for nanoscale analog and digital circuits [150,151]. To improve the device immunity against SCEs and the small signal parameters, new design approaches are required to enhance the reliability and electrical performances of the devices for nanoscale digital and analog applications.

Although numerous papers have modeled and studied the subthreshold and saturation behaviours of the nanoscale DG MOSFET [53, 126–128, 130, 140, 149, 150], until now, there are no studies to investigate the global electrical performances optimization, subthreshold and small signal parameters, of the nanoscale DG MOSFETs by using a global evolutionary-based optimization technique. One preferable approach is the multi-objective-based optimization, which could provide practical solutions for the nanoscale CMOS circuits design. The first step of our approach consists of accurate compact modeling of subthreshold and small signal parameters for nanoscale DG MOSFETs. The different compact models can be used in our study as objective functions, which are given as function of input design variables. The design of optimal nanoscale DG MOSFETs

requires new insights into the underlying physics, especially quantum mechanical (QM) treatment of the carriers confined in very thin Si films (see chapter 3).

Quantum-mechanical confinement of inversion-layer carriers significantly affects the drain current behavior of highly scaled MOSFETs [85, 118, 127, 152–154]. Therefore, an accurate analytical modeling of DG MOSFETs with arbitrary Si-film thickness is needed for physical insight as well as for a reliable optimization approach. Nanoscale DG MOSFETs introduce challenges to compact modeling associated with the enhanced coupling between the electrodes (source, drain, and gates), quantum confinement, ballistic or quasi-ballistic transport, gate tunnelling current, etc. [85]. However, in this compact model the subthreshold parameters and the quantum confinement for very thin silicon channels (less than 5nm) have not been taken into account. It has been shown in [118, 127, 153] that using the centroid instead of $Si - SiO_2$ interface for the carrier distribution is a good choice to model the device electrostatics. The same authors [118, 127, 153] also modeled the inversion centroid charge to overcome the strong variations of the surface potential. However, in these works, a closed-form model for the drain current was not provided, thus limiting the model use by our MOGA-based design approach.

In [127], an analytical model of the inversion charge including many fitting parameters by considering channel thickness effect only and ignoring the device dimensions and biases effects was suggested. In the proposed work, new accurate model for drain current is introduced by correcting the pervious classical charge model in [152] and the empirical threshold voltage shift model introduced by [154] to account the QM effects. These models were developed and successfully optimized according to 2-D self-consistent (NEGF) simulation in chapter 3. Thus, the performed accurate analytical models, for subthreshold and saturation regimes, will be used as objective functions to optimise the electrical performances of the nanoscale DG MOSFETs.

In this chapter, we present the applicability of multi-objective genetic algorithms optimization (MOGAs) approach to optimize the subthreshold and saturation behaviors of DG MOSFET for nanoscale CMOS digital and analog applications. The key idea of this approach is to find the best dimensions and electrical parameters of the transistor

to facilitate and improve the circuits design strategy. Design optimization, adopted in this work, is the process of finding the maximum/minimum of the subthreshold and small signal parameters called the objective functions and must also satisfy a certain set of specified requirements within constraints [155,156]. In the present chapter, we present an alternative approach based on MOGAs, where the designer can specify several objective functions simultaneously and all optimal results are presented as a hyper-plane called "Pareto front". The main advantages of this approach are its simplicity of implementation and provide to designer several possible solutions to choose the one that suites best his (analog and/or digital) application.

4.2 Electrical parameters of nanoscale DG MOSFET

4.2.1 Design description of nanoscale DG MOSFET

A schematic cross section of a symmetric n-channel DG MOSFET and the definition of the geometrical and electrical characteristics are shown in Figure 4.1.

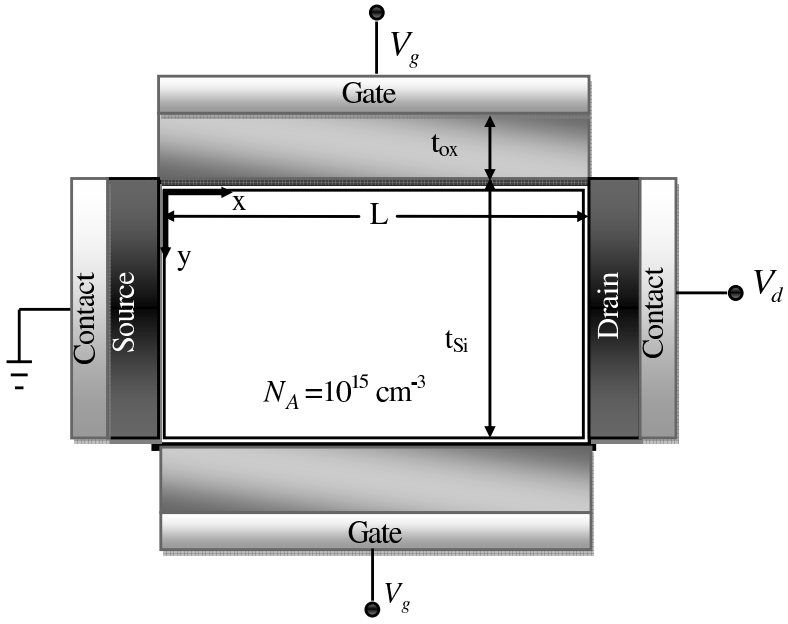


Figure 4.1: Magnetization Schematic sketch of symmetrical DG MOSFET structure investigated in this study with (channel doping $N_A = 10^{15} cm^{-3}$, t_{si} represents silicon thickness, L is channel length and t_{ox} is the oxide thickness)

As shown in the figure, t_{si} is the silicon film thickness, L is the channel length, t_{ox} is the oxide thickness and $N_{D/S}$ represents the doping level of the drain/source region respectively.

4.2.2 Model formulation of nanoscale DG MOSFET

4.2.2.1 Subthreshold current

In the subthreshold region, the current is mainly diffusion dominated and proportional to the electron concentration at the virtual cathode $n_{\min}(y)$ [157], and hence, the current density can be expressed as,

$$J_n(y) = qD_n \frac{n_{\min}(y)}{L} \left(1 - e^{V_{ds}/V_t}\right) \tag{4.1}$$

where D_n represents the diffusion constant and V_t is the thermal voltage, V_{ds} is the drain bias and q is the electron charge. $n_{\min}(y)$ is the minimum carrier concentration in the virtual cathode and can be expressed as,

$$n_{\min}(y) = \frac{n_i^2}{N_A} e^{\frac{\psi_{\min}(y)}{V_t}} \tag{4.2}$$

where n_i is the intrinsic carrier concentration, N_A is the channel doping concentration, and $\psi_{\min}(y)$ is the minimum channel potential. The subthreshold current can be obtained by integrating Eq. (4.1) over the entire channel film thickness. It leads, after some mathematical manipulations, to

$$I_{sub} = 2\frac{V_t}{Es} K(e^{\frac{\psi_{\min}}{V_t}} - e^{\frac{\psi^s_{\min}}{V_t}}) \tag{4.3}$$

where Es represents the constant electric field, $Es = 2(\psi_{\min} - \psi^s_{\min})/t_{si}$, $\psi^s_{\min}$ is the minimum potential at (Si/SiO_2) interface given by $\psi^s_{\min} = \psi_{\min}(x_{\min}, 0)$, $\psi_{\min}$ represents the minimum potential, $\psi_{\min} = \psi(x_{\min}, t_{si}/2)$, and K is a constant defined as $K = (q\mu_n W V_t n_i^2/LN_A)(1 - e^{-V_{ds}/V_t})$ with W is the width of the DG MOSFET and μ_n is electron mobility in the channel region.

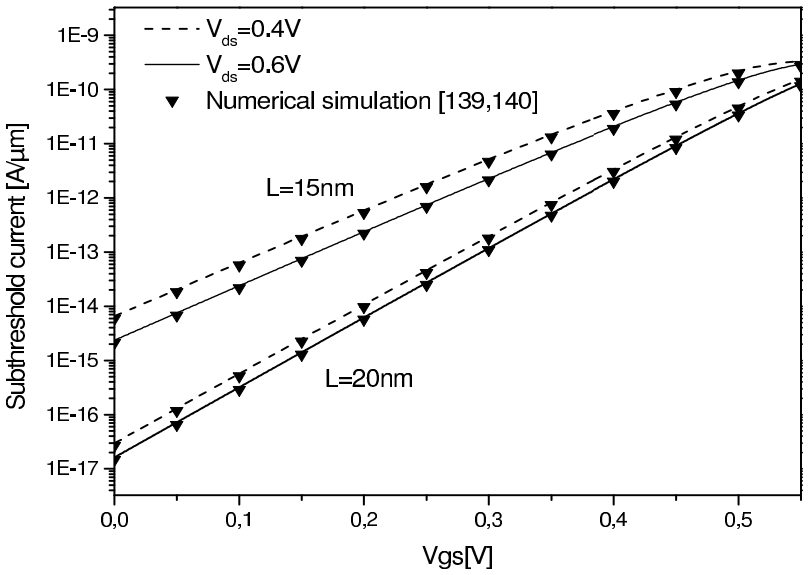


Figure 4.2: Subthreshold current as function of gate-source voltage

Figure 4.2 shows the variation of the subthreshold current versus gate source voltage for $V_{ds} = 0.4V$ and $V_{ds} = 0.6V$ over channel length variation $L = 15nm$ and $L = 20nm$. As shown in this figure, it can be deduced that the OFF-current is important for shorter channel length whereas it is reduced by increasing the drain source voltage. In this context, OFF-current is decreased with increasing channel length due to the less impact of the SCEs or due to the improved subthreshold slope as well as improved the ratio I_{on}/I_{off} .The comparison between numerical simulation [139, 140] and analytical simulation calculated by Eq. (4.3) finds out good agreement between the two models.

4.2.2.2 Subthreshold swing factor

Based on the assumption that the subthreshold swing (S) depends mainly on the carriers concentration $n_{\min}(y)$ at the minimum channel potential located at the depth y of the channel [69, 157], a compact model of subthreshold swing can be given, after some mathematical manipulations as,

$$S = S_0 \left[1 + \Delta S\right]^{-1} \tag{4.4}$$

where $S_0 = 60\text{mV/dec}$ represents the ideal value of the subthreshold swing, and ΔS is the subthreshold swing degradation coefficient given as,

$$\Delta S = \frac{\left(-\sinh\left(\frac{L}{\lambda}\right)\right)\beta + \sinh\left(\frac{x_{\min}-L}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} \tag{4.5}$$

with $\beta = \frac{\sinh\left(\frac{x_{\min}}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}$ where $\lambda = \sqrt{\frac{\varepsilon_{si}\cdot t_{ox}\cdot t_{si}}{2\cdot\varepsilon_{ox}}}$ represents the natural length of the studied device, ε_{si} and ε_{ox} represent the silicon and oxide permittivity, respectively, and x_{min} represents the minimum surface potential location which depends on electrical and geometrical parameters of the DG MOSFET [157].

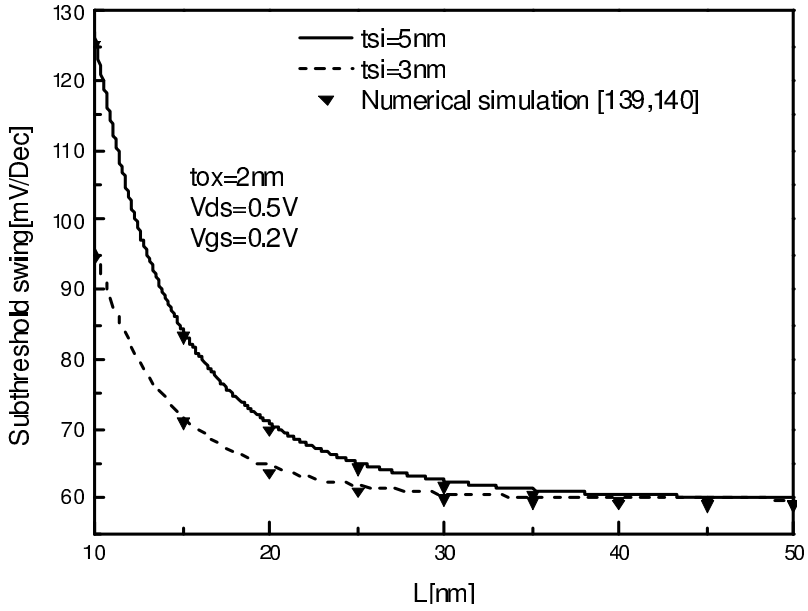


Figure 4.3: Subthreshold swing versus channel length

Figure 4.3, plots the subthreshold swing as a function of channel length calculated from our compact model according to Eqs. (4.4) and (4.5), for DG MOFET structure. It can be deduced that the subthreshold swing increases rapidly as the channel length down and reaches the ideal value when (a) $L > 30nm$ for $t_{Si} = 3nm$ (b) $L > 40nm$ for $t_{Si} = 5nm$. As shown in this figure, the subthreshold swing is reduced with decreasing the thickness width t_{si} down to $3nm$, due to the decreased naturel length λ and consequently

the decreased subthreshold swing degradation ΔS. Furthermore, subthreshold swing S decreases as channel length L increases due mainly to the suppressed SCEs.

The comparison of the subthreshold swing evolution with numerical simulation [139, 140] for various cases, shows that the DG MOSFETs provides better subthreshold swing and can be expected to have an ideal subthreshold swing factor 60mV/dec which is a good indicator validating our assumptions about the immunity against (SCEs) particularly when compared to 2-D self-consistent (NEGF) formalism.

4.2.2.3 Threshold voltage roll-off and DIBL

For nanoscale DG MOSFETs, short-channel effects such as threshold voltage roll-off and DIBL have an important impact on the device performances. Based on the surface potential model proposed in [157], the threshold voltage can be derived using the condition of the minimum channel potential $\psi_{s\,\min}|_{V_{gs}=V_{th}} = 2.\phi_B$, with $\psi_{s\,\min} = \psi_s(x_{\min})$, V_{th} is the threshold voltage value, and ϕ_B represents the bulk potential of silicon body given as $\phi_B = (K_B T/q).\ln(N_A/n_i)$ where K_B represents the Boltzmann constant. The location of the minimum surface potential can be obtained analytically by solving $\frac{d\psi_s(x)}{dx} = 0$ [157]. The solution of the equation $\psi_{s\,\min}|_{V_{gs}=V_{th}} = 2.\phi_B$ at low drain-source voltage for very short channel lengths can be given as,

$$V_{th} = \frac{-2\left(V_{bi} + \frac{q\cdot N_A\cdot\lambda^2}{\varepsilon_{si}}\right)\left(\sinh\left(\frac{L}{2\lambda}\right)/\sinh\left(\frac{L}{\lambda}\right)\right)}{1-2\left(\sinh\left(\frac{L}{2\cdot\lambda}\right)/\sinh\left(\frac{L}{\lambda}\right)\right)} + \frac{\left(2\phi_B + \frac{q\cdot N_A\cdot\lambda^2}{\varepsilon_{si}}\right)}{1-2\left(\sinh\left(\frac{L}{2\cdot\lambda}\right)/\sinh\left(\frac{L}{\lambda}\right)\right)} \tag{4.6}$$

The threshold voltage roll-off is a consequence of the charge sharing effect and typically considered one of the main indications of the short channel effect. The threshold voltage roll-off is given [157] by

$$\Delta V_{th} = V_{th} - V_{th,L} \tag{4.7}$$

where $V_{th,L}$ represents the threshold voltage for long channel devices and given by [157]

$$V_{th,L} = 2\phi_B + q \cdot N_A \cdot \lambda^2/\varepsilon_{si} \tag{4.8}$$

The DIBL effect occurs when the barrier height for channel carriers at the edge of the source is reduced due to the influence of drain electric field, upon application of a high drain voltage. As the voltage drop between the source and drain increases, the depletion region under the drain can lower the potential barrier of the source-to-channel junction. If the barrier between the source and channel is decreased, electrons are more freely injected into the channel region [157]. Therefore, the threshold voltage is lowered and the gate has less control of the channel. From the threshold voltage obtained at $V_{ds} = 0.1V$ and $V_{ds} = 0.3V$, the DIBL effect can be extracted from the analytical model given by Eq. (4.6). The DIBL can be expressed as,

$$DIBL = \frac{V_{th}|_{V_{ds}=0.3V} - V_{th}|_{V_{ds}=0.1V}}{(V_{ds} = 0.3V) - (V_{ds} = 0.1V)} \times 1000\,[mV/V] \tag{4.9}$$

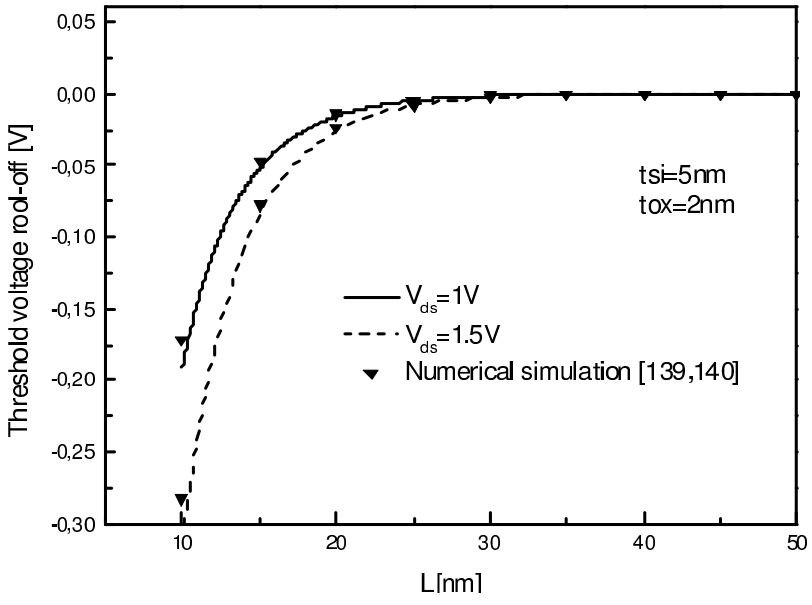


Figure 4.4: threshold roll-off versus channel length

Figure 4.4 depicts the predicted threshold voltage roll-off model versus the channel

length L at $V_{ds} = 1V$ and $V_{ds} = 1.5V$, compared with numerical simulations where the predicted model is based on Eqs. (4.6), (4.7) and (4.8). It can be noted that the threshold voltage rool-off increases rapidly as the channel length increase and reaching the ideal value when $L = 35nm$ with $V_{ds} = 1.5$ and $L = 25nm$ with $V_{ds} = 1$. Furthermore, as the drain source voltage gets higher, the threshold voltage rool-off as well as DIBL become more significant for very short channel length ($L < 20$) which can be explained by the fact that the free electrons injected in the channel by applying high drain electric field contribute essentially in the nanoscale domain.

4.2.2.4 Transconductance and output conductance

The drain current I_{ds}, of a symmetrical DG MOSFET including quantum and modulation length effects, is given in [143, 148] as we have already mentioned in Chapter 5,

$$I_{dsq} = \mu_{eff}\frac{W}{L_{eff}}\left[\frac{Q_{iqs}^2 - Q_{iqd}^2}{C_{oxq}} + 4V_t(Q_{iqs} - Q_{iqd}) + V_t Q_0 \ln\left(\frac{Q_0 + 2Q_{iqd}}{Q_0 + 2Q_{iqs}}\right)\right] \tag{4.10}$$

where μ_{eff} represents the effective electron mobility including saturation velocity effect, L_{eff} is the effective channel length including channel length modulation effect, Q_{oxq} is the quantum oxide capacitance, Q_{iqs} and Q_{iqd} are the quantum inversion charge at source and drain end, respectively, and Q_0 is the charge coefficient given [134] by $Q_0 = (8V_t\varepsilon_{si}/t_{si})$. Our explicit drain current model is extremely accurate because the concept of quantum correction is used (see chapter 3). They are accurate not only in terms of drain current but also in terms of the derivatives such as transconductance and output-conductance. Thus, according to the drain current expression Eq. (4.10), the transconductance and output-conductance parameters can be calculated for different device dimensions and applied gate and drain voltages. The transconductance and the output conductance are given as,

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}} \tag{4.11}$$

$$g_{ds} = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}} \tag{4.12}$$

The calculated analytic expressions of the transconductance Eq. (4.11) and output conductance Eq. (4.12) are continuous and valid in all operation regions as well as the drain current expression Eq. (4.10).

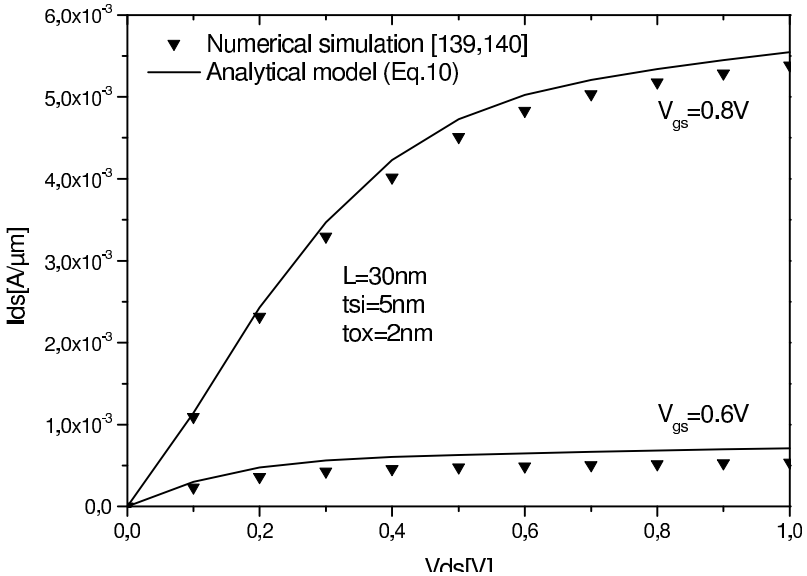


Figure 4.5: $I_{DS} - V_{DS}$ characteristics for different gate voltages

Figure 4.5 presents comparisons between numerical simulations data [139, 140] and drain current data calculated from Eq. (4.10) for the nanoscale DG MOSFET. We can see that the proposed models provide a good agreement for a very wide interval of geometrical and physical parameters for nanoscale DG MOSFETs in comparison with numerical simulations. The physical soundness of the analytic model for short channel DG MOSFETs and the validity of the modeling procedure including SCEs and QE have been validated in Chapter 3 by the well-agreeing drain current plots for all operation regimes over a wide range of channel lengths and channel thickness. Hence, the proposed compact models can be used as objective functions in our MOGAs-based approach.

4.3 MOGA-based optimization

Recently, evolutionary computation techniques (EC) have been recognized as an important approach for the semiconductor devices computer-aided design area in addressing the growing challenges of designing next generation of nanoelectronics devices, circuits, and systems [150, 158]. Evolutionary-based optimization technique has been defined as finding a vector of decision variables satisfying constraints to give acceptable values to all objective functions [150], [155, 156, 158]. The MOGAs differ from most optimization techniques because of their global searching carried out by one population of solutions rather than from one single solution. An ideal multi-objective optimization procedure constitutes of two steps. The first is to find some optimal solutions corresponding to multiple objectives considered in research space. The next step is to choose the most suitable solution by using higher level information. Due to the simple mechanism and high performance provided by MOGAs for multi-objective global optimization, MOGAs can be applied to study and improve the nanoscale DG FET-based circuits design strategy.

The main step of our approach consists of compact models of subthreshold and small signal parameters for DG MOSFETs defined previously. These compact models will be used in the next section as objective functions, which are given as function of input design variables.

4.3.1 Computation methodology

For the purpose of MOGAs-based optimization of electrical performances of the DG MOSFET, routines and programs for MOGAs computation were developed using MATLAB 7.2 and all simulations are carried out on a Pentium IV, 3GHz, 1GB RAM computer. For the implementation of the MOGAs, tournament selection is employed which selects each parent by choosing individuals at random, and then choosing the best individual out of that set to be a parent. Scattered crossover creates a random binary vector. It then selects the genes where the vector is unity from the first parent, and the genes where the vector is zero from the second parent, and combines the genes to form the child.

An optimization process was performed for 20 population size and maximum number of generations equal to 100, for which stabilization of the fitness function was obtained. The adopted multi-objective genetic algorithm works as follows [155], [156],

Algorithm 3 Multiobjective Genetic Algorithm

1: Start with a randomly generated population of ′n′ 1-bit chromosomes (candidate solutions to the problems):
2: Calculate the overall objective function of each chromosome ′X′ in the population.
3: Create ′n′ offspring from current population using the three MOGA operators namely selection, crossover and mutation.
4: Replace the current population with the updated one.
5: Repeat the above steps until the termination criteria is reached.

The MOGAs parameters were varied and the associated optimization error was recorded.

Based on the assumption that the subthreshold swing and the DIBL effect are linearly correlated, suggesting that the degradation of these parameters has the same origin and perfectly controlled by the natural channel length [159], [160]. Hence, the optimization of the subthreshold swing leads to the optimization of the DIBL. Therefore, the optimization of the electrical behavior of the DG MOSFET can be reduced from six MOGAs problem to five objective functions. Therefore, five objectives are considered in this Chapter, i.e. subthreshold swing degradation coefficient ΔS, OFF-state current $I_{sub}(V_{gs} = 0V)$, threshold voltage roll-off $\Delta V_{th}(X)$, transconductance $g_m(X)$ and output conductance $g_{ds}(X)$. So, the obtained design can provide the best electrical performances by satisfying of the following objective functions:

- Minimization of the OFF-current state:$I_{OFF}(X)$
- Minimization of the subthreshold swing degradation coefficient:ΔS
- Minimization of the threshold voltage roll-off:$\Delta V_{th}(X)$
- Maximization of the transconductance function:$g_m(X)$
- Minimization of the output conductance function:$g_{ds}(X)$

where X represents the input normalized variables vector which is given as $X = (t_{si}, t_{ox}, L, V_{gs}, V_{ds})$. It is to note that the input vector can be extended to include other design parameters like: overlap and underlap lengths, channel doping profile, source and drain region lengths. The overall objective function is obtained by given weightage based on 'Weighted sum approach method' as follows,

$$F(X) = w_1(1/g_m(X)) + w_2 I_{OFF}(X) + w_3 \Delta S(X) + w_4 \Delta V_{th}(X) + w_5 g_{ds}(X) \qquad (4.13)$$

where w_i (i=1-5) are weight functions satisfy $\sum_i w_i = 1$ [156].

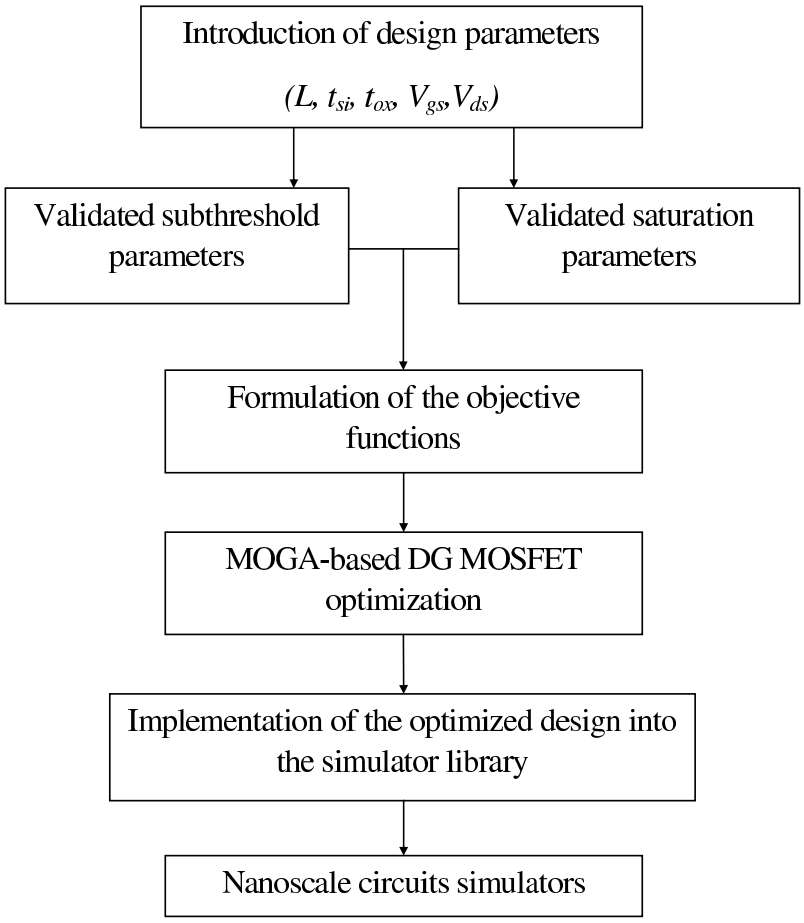


Figure 4.6: Flowchart of the proposed approach for nanoscale circuits optimization

If high derived current, low power dissipation and high commutation speed transistor are the required parameters by the devices designer. Therefore, the transconductance,

OFF-state current, subthreshold swing, output conductance and threshold voltage roll-off are equally important. Hence, w_i (i=1-5) can be assigned equal values as 0.20. Lower value of OFF-state current is needed to design a transistor with low power dissipation and high transconductance and commutation speed values are needed to improve the transistor performances in circuits design. It is to note that the optimization of the transconductance and OFF-state current leads to increase of the ON-state current, and therefore an increasing of the ratio can be obtained by the proposed approach. Given the clearly defined problem to be solved and a bit string representation for the candidate solutions, the MOGA based-optimization follows the flowchart presented in Fig. 4.6.

4.3.2 Results and discussion

The database used for validation and optimization of the device configuration is built on the basis of numerical model of the current-voltage characteristics of a nanoscale ultra-thin body DG MOSFET developed using the non-equilibrium Green's function formalism (NEGF) [140] (see chapter 3). The developed MOGA-based approach can be used as the interface between device compact modeling and circuit simulators like SPICE, Cadence, and Anacad's Eldo in order to optimize the electrical circuit performances. A simplified overview is shown in Fig. 4.6. For the optimized configuration, the normalized overall objective function, was 8.70×10^{-3} and almost 100% of the submitted cases were learnt correctly.

Figure 4.7 shows the variation of normalized overall objective function as function of generation number where the minimum objective function can be reached for 2000 iterations. The steady decrease in the subthreshold and small signal parameters of the best solution in each generation until it reaches a best possible value can be attributed to the selection procedure used namely tournament selection.

Final optimized DG MOSFET parameters are summarized in Table 4.1

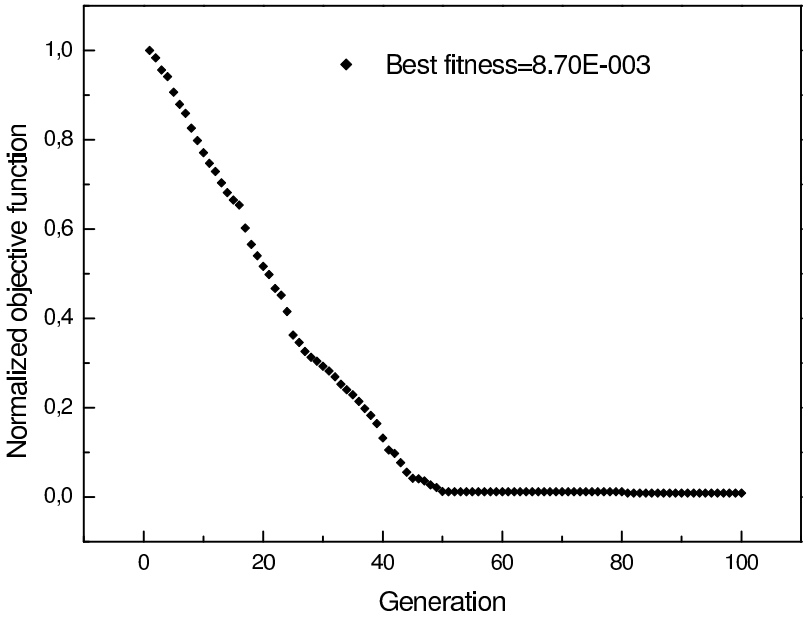


Figure 4.7: Variations of normalized overall objective function with generations

Table 4.1: Optimized nanoscale DG MOSFET design parameters

Symbol	Quantity	Design(1) [142]	Design(2) [160]	Optimized design
V_{ds}	Drain source voltage	1 V	0.8 V	1 V
V_{gs}	Gate voltage	1V	0.9 V	0.9 V
t_{si}	Silicon thickness	4 nm	3 nm	2.5 nm
t_{ox}	thickness of the SiO_2	1 nm	1 nm	1 nm
L	Channel length	10 nm	10 nm	11 nm
Objective functions				
	Subthreshold parameters:			
ΔV_{th}	Threshold voltage roll-off	2.80×10^{-2} V	1.14×10^{-2} V	6.21×10^{-3} V
ΔS	Subthreshold swing	2.90×10^{-1}	2.02×10^{-1}	1.20×10^{-1}
I_{OFF}	OFF-state current	4.22×10^{-13} $A/\mu m$	6.17×10^{-15} $A/\mu m$	3.40×10^{-16} $A/\mu m$
I_{ON}	On state-current	4.34×10^{-8} $A/\mu m$	2.72×10^{-8} $A/\mu m$	8.19×10^{-8} $A/\mu m$
I_{ON}/I_{OFF}	Ratio ION/IOFF	1.02×10^{5}	1.32×10^{7}	2.40×10^{8}
	Small signal parameters :			
g_m	Transconductance	3.28×10^{1} $mS/\mu m$	2.89 $mS/\mu m$	3.56×10^{1} $mS/\mu m$
g_{ds}	Output conductance	1.86 $mS/\mu m$	9.85×10^{-1} $mS/\mu m$	5.64×10^{-1} $mS/\mu m$

4.3.3 Impact on nanoscale circuits design

In order to show the impact of the MOGAs-based approach on the design and optimization of the nanoscale CMOS circuits we propose the study of a single transistor amplifier including our transistor optimization approach. The amplifier consisted of a DG MOSFET and a current generator as shown in Figure 4.8.

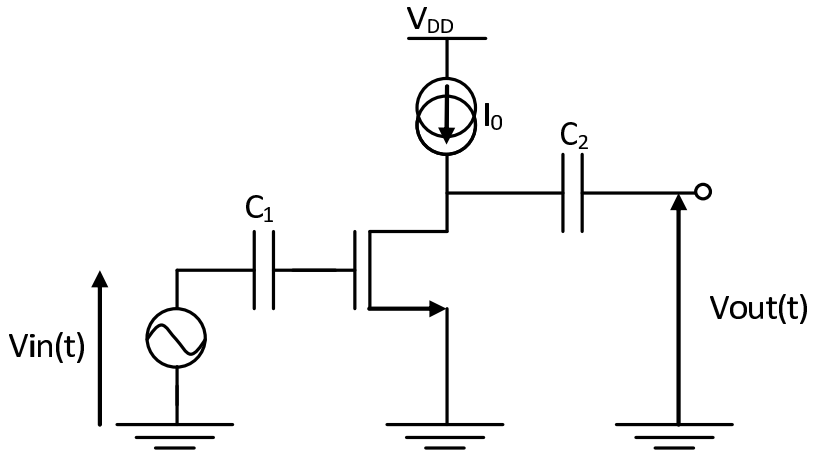


Figure 4.8: Nanoscale DG MOSFET voltage amplifier

The current generator is set at $I_0 = 1mA$ and the gate voltage is set to give the optimized biasing conditions of the transistor. The gain and cut-off frequency values of the nanoscale DG MOSFET amplifier with and without device optimization are shown in Table 4.2. The gain and cut-off frequency, for optimized design, is about 63.16 and 164 GHz, respectively. However, the gain and cut-off frequency degraded to about 29.39 and 133 GHz, respectively, for device without optimization. The gain and cut-off frequency are given by $G_v = |g_m/g_{ds}|$ and $f_T = g_m/(2\pi C_{oxq})$, respectively.

From Table 4.2, it is observed that an enhancement of circuit electrical performances, the gain and the cut-off frequency, can be obtained by using the proposed approach as design tool to study and optimize the nanoscale circuit electrical behavior.

Table 4.2: Optimized nanoscale single transistor amplifier design parameters

Symbol	Quantity	Optimized design	Design without optimization [160]
V_{ds}	Drain source voltage	1 V	0.8 V
V_{gs}	Gate voltage	0.9 V	0.9V
t_{si}	Silicon thickness	2.5 nm	3 nm
t_{ox}	thickness of the SiO2	1 nm	1 nm
L	Channel length	11 nm	10 nm
G_v	Gain voltage	63.16 V/V	29.39V/V
f_T	Cut-off frequency	164 GHz	133 GHz

4.4 Summary

In this chapter, a new MOGAs-based design approach to study and optimize the electrical performances of DG MOSFET for nanoscale digital and analog CMOS applications has been proposed. The application of MOGAs in this Chapter is aimed at the maximization of electrical performances of the nanoscale DG MOSFETs and the developed approach has successfully searched the maximum possible ultimate electrical performances and the input design parameters that can yield those specific performances.

Application of the MOGAs-based design approach to nanoscale single transistor amplifier has also been discussed. It can be concluded that proposed MOGAs-based approach is efficient and gives promising results. It is to note that the proposed approach can be extended to include other design parameters like underlap, overlap and series resistances. However, new complex and compact models which include these parameters should be developed. This MOGAs-based design approach not only benefits the modeling and optimization of nanoscale DG MOSFETs but also can be extended for other real world applications.

The similar methodology can be used to study other design structures of nanoscale multigate MOSFETs for such application like ultra-low power application (see chapter 5).

The text of Chapter 4, in part, is a reprint of the material as it appears in "Electrical performance optimization of nanoscale double-gate MOSFETs using multiobjective genetic algorithms" by T. Bendib and F. Djeffal, IEEE Transactions on Electron Devices, 2011. The dissertation author was the primary investigator and author of this paper.

Chapter 5

Modeling and optimization of subthreshold behavior for nanoscale multigate MOSFETs

Contents

5.1 Introduction

Multi gate field-effect transistors (MuGFETs) have been reported as promising candidates for future nanoelectronic technology [53, 160, 161]. Research in MuGFETs for deep submicron CMOS-based applications is currently being carried out by many semiconductor manufacturers, as these devices hold the promise for pushing the limits of silicon integration beyond the limits of classical planar technologies [12, 53, 160, 161]. In addition, MuG FETs have emerged as excellent devices to provide the electrostatic integrity needed to scale down transistors to minimal channel lengths that allows a continuous progress in analog and digital applications. All of these devices show high electrical performance in the subthreshold domain, where an optimal subthreshold swing and a low leakage current can be recorded for nanoscale applications.

However, as the channel length shrinks, the control of the gate voltage on the threshold voltage decreases because of the increased charge sharing from source and drain. So, the threshold voltage reduction with decreasing channel lengths, the subthreshold swing, the OFF-current, the drain induced barrier lowering (DIBL) and the transconductance, the most important small signal parameter which describes the transistor behavior for analog applications, are important parameters that need to be addressed while providing immunity against Short-Channel-Effects (SCEs) and better small signal parameter [53, 150, 159, 162, 163].

To improve the device immunity against SCEs and the transconductance parameter, new modeling and optimization based approaches for MuGFETs are required to analyze and examine subthreshold behavior of the devices for digital and/or analog application. The accuracy of these new models, that are based on physics, allow the process engineer and circuit designer to make projections beyond the available silicon data for scaled dimensions and also enables fast circuit/device co-optimization. In counterpart, the simplifications in the physics enable very fast analysis of device/circuit behavior when compared to the much slower numerically-based TCAD simulations. Thus, it is necessary to develop new accurate models of MuGFETs including design optimization approaches to

enhance the reliability and electrical performances of the devices for technology/circuit development in the short-term and for product design in the long-term.

One preferable approach is the evolutionary-based modeling, which could provide practical solutions for a nanoscale CMOS circuit design. We called this the "intelligent simulator" approach [124]. The key idea of this approach is to find the best geometrical and electrical parameters of the transistor to facilitate the circuits design strategy. In order to facilitate a device design and improve electrical behavior for high-performances digital and analog circuits, the proposed approach suggests multi-objective functions problem.

In this chapter, we examine the possibility of developing new models assessing the performance of our proposed MuGFETs structures (DG MOSFET, GCGS DG MOSFET and JLGAA MOSFET) under different combined constraints. Based on surface potential formalism, these models are developed for the subthreshold domain in order to accurately describe the device behavior and to facilitate the application of multi-objective genetic algorithms optimization (MOGAs) approach which will be used to optimize geometrical and electrical parameters of MuGFET for nanoscale CMOS digital and analog applications. Thus, the developed models are used as objective functions which should satisfy a certain set of specified requirements within constraints [155, 156, 164]. The optimal result is defined using weighting-sum approach which is simple to implement and provide to designer optimal solution that suites best his application (analog or digital).

The rest of this chapter is partitioned as follows: Section 5.2, provides the modeling approach for DG MOSFET including free carrier and interfacial trap effects. Section 5.3 and Section 5.4 propose new multigate structures GCGS DG MOSFET and JLGAA MOSFET respectively. In these sections, analytical subthreshold models are developed, the design parameters of these structures are optimized and the performed simulation results are discussed. Finally, Section 5.5. summarizes some concluding notes.

5.2 Double Gate MOSFETs including free carrier and interfacial traps effect

It is widely recognized that double gate (DG) MOSFETs are considered among the most probable choices to continue CMOS performance boost beyond the conventional scaling frontiers [12, 124, 149, 165, 166]. However, the use of classical physics to describe the properties of DG MOSFETs leads to an inaccurate prediction of their electrical characteristics.

The extraction of accurate information about the subthreshold behavior requires the numerical solution of the Schrödinger and Poisson equations including hot-carriers and degradation effects, based on the Non-Equilibrium Greens Function (NEGF) formalism, assuming quantum effects are to be fully accounted [124]. To avoid complexity and computational cost of numerical solving using NEGF formalism [124], an accurate semi-analytical modeling is considered as most aiming approach to ease the computation. This later is necessary if the model is needed to be implemented in circuit simulators (PSPICE, CADENCE, SYNOPSIS,...).

In nanoscale devices, the interfacial hot-carrier induced becomes a major reliability concern. These hot-carriers result from the impact ionization in the channel near the drain junction, which subsequently are injected into the gate oxide and give rise to a localized and non-uniform pileup of interface states near the channel−drain junction [53, 162, 167]. Recently, several papers have been published to model and study the MOSFET including interfacial traps [53, 162, 168]. However, in these publications, simple and accurate closed expressions for thin layer channel, surface potential and subthreshold swing parameters including interfacial traps and free carrier effects were not provided, thus limiting the models use by designers. To analyze the nanoscale DG MOSFET for the digital circuit applications precisely, it is important to develop an accurate 2-D semi-analytical subthreshold swing model in which the hot-carrier and free carrier effects are included.

In the present section, we investigate the DG MOSFET at miniaturization limits including the free carriers and hot-carrier degradation effects after considering the step-

function approximation as discussed in [53,162,167,168] for interface charge distribution. In this context, the Poisson equation for subthreshold regime in which the free carriers and interfacial traps effects are included, is solved, allowing the determination of the 2-D potential distribution along the channel. The proposed semi-analytical model explains the effect of the channel length L, hot-carrier-induced interface charge density N_f and free carriers q_i on the scaling capability of the thin DG MOSFETs. The presented model of the hot-carrier degradation effect on nanoscale thin DG MOSFETs is further confirmed with 2-D numerical simulations [139].

5.2.1 Description of the studied structure

A detailed view of the nanoscale DG MOSFET is illustrated in figure 5.1. The cross sectional view of a 4-terminal n-channel DG MOSFET is shown in figure 5.1 where the front and back gate oxides, gate materials and the gate voltages are the same. The structure is symmetric with the doping level of the drain/source region is given by $N_{D/S}$ respectively. In the figure, x denotes the direction along the channel length and y denotes the direction along the silicon film thickness. The channel is nearly undoped to take the advantage of enhanced mobility by eliminating the charged-impurity scattering.

In this structure, we assume the existence of an interfacial charge density (N_f) near the drain, thus the undoped channel region can be divided into fresh and damaged subregions. The total length of the channel is L, the length of the fresh subregion I is denoted by L_1, whereas the length of the damaged subregion II can be deduced as $L_d = L - L_1$.

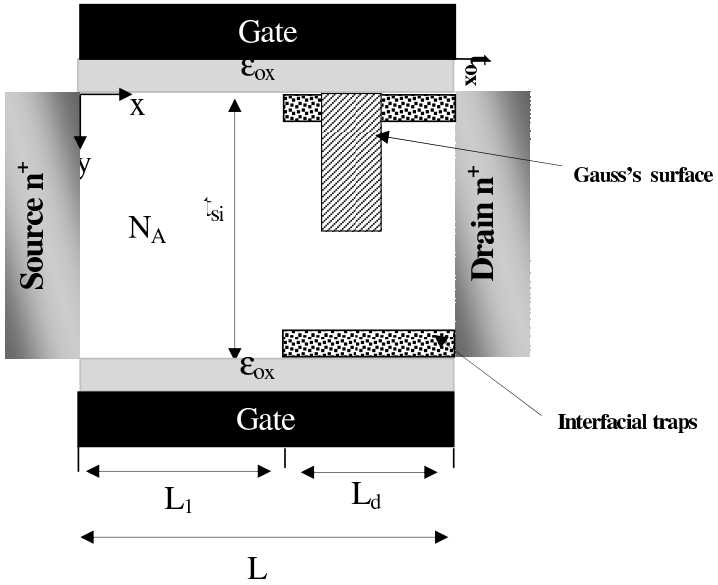


Figure 5.1: Cross-sectional view of the DG MOSFET inner structure including the interfacial traps distribution

5.2.2 Model formulation

Modeling of the electrical behavior of nanoscale transistors needs an accurate description of the complex nature of the electrons transport in the subthreshold regime inside the channel. To this aim we used a two-dimensional potential analysis for the majority carrier (electron) transport including the free carrier and traps effects in order to develop accurate semi-analytical models and guarantee the good agreement with numerical simulations across the full range of the applied voltages and device parameters. Based on several works recently published [142, 160, 169], the application of the Drift Diffusion mechanism (DDm) represents a great simplification, over the use of any of the other formalisms, and provides an accurate modeling approach to study the nanoscale device behavior in subthreshold regime. For the nanoscale devices, the solution of 2-D Poisson's equation, under weak inversion conditions, satisfying suitable boundary conditions is required to model the short channel effects (SCEs). Refer to figure 5.1, the 2-D Poisson's

equation for the channel region, without free carriers and traps effects, is given by

$$\frac{\partial^2 \psi(x,y)}{\partial x^2} + \frac{\partial^2 \psi(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si}} \tag{5.1}$$

subject to the boundary conditions,

$$\varepsilon_{ox}\frac{V_{F,eff} - \psi(x,0)}{t_{ox}} = \varepsilon_{si}\left.\frac{\partial \psi(x,y)}{\partial y}\right|_{y=0} \tag{5.2a}$$

$$\varepsilon_{ox}\frac{V_{B,eff} - \psi(x,t_{si})}{t_{ox}} = \varepsilon_{si}\left.\frac{\partial \psi(x,y)}{\partial y}\right|_{y=t_{si}} \tag{5.2b}$$

$$\psi(0,y) = V_{bi} \tag{5.2c}$$

$$\psi(L,y) = V_{bi} + V_{ds} \tag{5.2d}$$

So, we have to resolve such boundary problem separately for each region after adding a new condition defined on interfacial point between the free region and damaged (with traps effects) one as, $\psi(L_1, y) = V_p$. where ε_{ox} is the oxide permittivity, t_{si} is the thickness of silicon channel. V_{bi} is the junction voltage between the source/drain and intrinsic silicon with $V_{bi} = (kT/q)\ln\left(N_{D/S}/n_i\right)$, n_i is the intrinsic silicon density and V_{ds} is the drain to source voltage.

As it is presented in [142] for obtaining the expression of the surface potential, $\psi_s(x)$, the Gauss's law is applied to the particular closed surface in the channel region (Figure 5.1). In our case the free carrier and traps effects should be taken into account. So, electric field for the second region (damaged) can written as,

$$-E(x)\frac{t_{si}}{2} + E(x+dx)\frac{t_{si}}{2} - E(x)dx = -\frac{qN_A t_{si}}{2\varepsilon_{ox}} - \frac{q_i(x)}{2\varepsilon_{si}} + \frac{qN_f t_{si}}{2C_{ox}} \tag{5.3}$$

In the right hand side, the first term represents the depletion charge, the second term is the mobile inversion charge density and the last one corresponds to the interfacial traps effects. For thin films used in this study ($t_{si} < 10nm$), electric field $E(x)$ in Eq. (5.3) can be approximated as [142, 169]. After algebraic manipulations the following equation

is obtained to explain the surface potential, $\psi_s(x)$, for both regions as,

$$\frac{d^2\psi_s(x)}{dx^2} - \frac{1}{\lambda^2}\psi_s(x) = D \tag{5.4}$$

The inversion charge of long channel DG MOSFET devices based on a 1-D analytical solution of Poisson equation incorporating only the mobile charge term is given [160]as,

$$Q_{iL} = \frac{qn_i^2}{N_A} t_{si} e^{\frac{q\psi_s}{kT}} \tag{5.5}$$

where k is the Boltzmann constant, q represents the electron charge.

From Eq. (5.5), it is interesting to point out that the exact inversion charge model depends on the channel depth, which is expected to affect the subthreshold behavior due to the 2-D extra potential, $\Delta\phi(x, y)$, in the silicon film induced by the SCEs [160,170]. By following the studies published in [160, 170, 171], it can be seen that in nanoscale devices, the extra potential induced in the silicon film due to SCEs modifies the inversion charge density by the correction factor CF:

$$q_i = \frac{Q_{iL}}{CF} \tag{5.6}$$

where

$$CF = \frac{1}{L}\int_0^L \frac{1}{t_{si}}\int_0^{t_{si}} e^{-\Delta\phi(x,y)/kT} dxdy \tag{5.7}$$

The good approximation for the extra potential described in [169] can be used to calculate numerically CF and, therefore, the inversion charge from Eq. (5.6) as a function of drain and gate voltages. In region I (fresh region, $0 \leq x \leq L_1$) the equation to be solved is,

$$\frac{d^2\psi_{s1}(x)}{dx^2} - \frac{1}{\lambda^2}\psi_{s1}(x) = D_1 \tag{5.8}$$

with $\lambda = \sqrt{\frac{\varepsilon_{si} t_{si}}{2C_{ox}}}$, $D_1 = \frac{qN_A}{\varepsilon_{si}} - \frac{2C_{ox}}{t_{si}\varepsilon_{si}} V_g^* + \frac{q_i}{t_{si}\varepsilon_{si}}$ and C_{ox} is the oxide capacitance [170].

Under the following boundary conditions,

$$\psi_{s1}(0,y) = V_{bi} \tag{5.9a}$$

$$\psi_{s1}(L_1,y) = V_p \tag{5.9b}$$

where V_g^* represents the effective gate voltage.

The parameter λ is the natural length, which characterizes the SCEs in DG MOSFETs, assuming that the current flows along the channel. In region II (damaged region, $L_1 \leq x \leq L$) the equation to be solved is,

$$\frac{d^2\psi_{s2}(x)}{dx^2} - \frac{1}{\lambda^2}\psi_{s2}(x) = D_2 \tag{5.10}$$

with $D_2 = \frac{qN_A}{\varepsilon_{si}} - \frac{2C_{ox}}{t_{si}\varepsilon_{si}}V_g^* + \frac{q_i}{t_{si}\varepsilon_{si}} - \frac{qN_f}{C_{ox}}$

Under the following boundary conditions,

$$\psi_{s2}(L,y) = V_{bi} + V_{ds} \tag{5.11a}$$

$$\psi_{s2}(L_1,y) = V_p \tag{5.11b}$$

$$\left.\frac{\partial\psi_{s1}(x)}{\partial x}\right|_{x=L_1} = \left.\frac{\partial\psi_{s2}(x)}{\partial x}\right|_{x=L_1} \tag{5.11c}$$

$$\left.\psi_{s1}\right|_{x=L_1} = \left.\psi_{s2}\right|_{x=L_1} \tag{5.11d}$$

V_p represents the potential at the both regions interface can be deduced by resolving the linear system given in Eq. (5.11c)and Eq. (5.11d), which reflects the continuity of the electric field and potential equations at $x = L_1$.

Since ψ_s given by Eq. (5.4) depends on $q_i(x)$ (Eq. (5.6)), replacing Eq. (5.6) in Eq. (5.4) leads to an implicit equation on $q_i(x)$, which is solved numerically for obtaining $q_i(x)$.

After some mathematical manipulations we lead to semi-analytical expressions of the surface potential for both regions as,

For region I:

$$\psi_{s1} = C_{11}\exp(m_1 x) + C_{12}\exp(-m_1 x) - \frac{R_1(x)}{m_1^2} \tag{5.12}$$

For region II:

$$\psi_{s2} = C_{21}\exp(m_2 x) + C_{22}\exp(-m_2 x) - \frac{R_2(x)}{m_2^2} \tag{5.13}$$

with C_{ij}, m_i and $R_i(x)$ calculated for filling the boundary conditions given by Eqs. (5.9a), (5.9b) and Eqs. (5.11a), (5.11b), (5.11c), (5.11d).

Refer to Figure 5.2 it is clear that the minimum potential is located in the first region (fresh region). So, the development of the Subthreshold swing model is mainly depends on ψ_{s1} behavior. Based on the previous assumption about proportionality between the drain current and the free carriers density at the virtual cathode following the Boltzmann distribution function, the general subthreshold swing (S) model is given [170] by,

$$S = \frac{kT}{q}\ln(10) \times \left[\frac{\partial \psi_{s1\,\min}}{\partial V_{gs}}\right]^{-1} \tag{5.14}$$

Hence, a closed form expression for subthreshold swing for the studied DG MOSFET including hot-carriers degradation effects can be obtained using Eq. (5.12) and Eq. (5.14). A small subthreshold swing is required to provide an adequate value of the on-to-off current ratio so that a DG MOSFET can effectively work as a switch. The subthreshold swing of a long channel fully depleted DG MOSFET has an ideal value ($S = 60mV/dec$). To have an acceptable performance, the subthreshold swing has to be close to the ideal value.

5.2.3 Results and discussion

Figure 5.2 shows the variation of surface potential along the channel for the studied DG MOSFET. To explore better performance of our approach, the calculated potential using conventional model, without free carrier effects, is also included for comparison. Two interesting features can be easily observed. Firstly, the incorporation of free carriers effect introduces a shift in the surface potential profile along the channel compared to the conventional model, which shows the dependency between the decrease in this poten-

tial and free carriers effects in weak inversion regime. The shift in the potential profile screens the region near the channel centre from the variations in drain voltage and thus ensures augmentation in subthreshold swing in comparison with conventional DG MOSFETs models (without free carriers effects). Thus, the incorporation of free carriers in subthreshold parameters computations is very important in order to ensure the accuracy of the device models.

Finally, the surface potential for both structures with traps deviates considerably from that of the fresh device where the potential surface in the damaged region is increased when the interface charges N_f are present. This is due to the important effect of the hot-carrier induced localized charge density on the electrons transport characteristics (drain current) through the channel. In addition, the profile of the surface channel potential is altered considerably loosing its parabolic nature if the length of damaged region is modified.

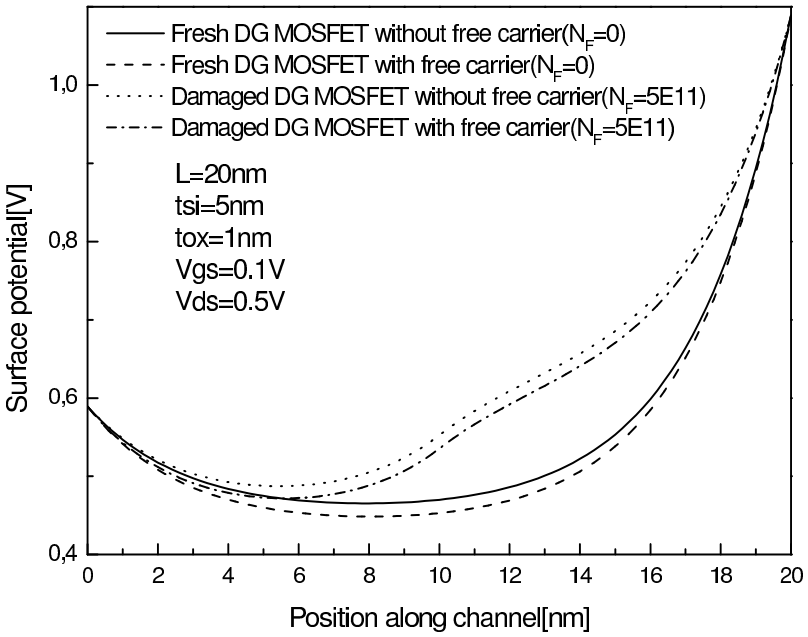
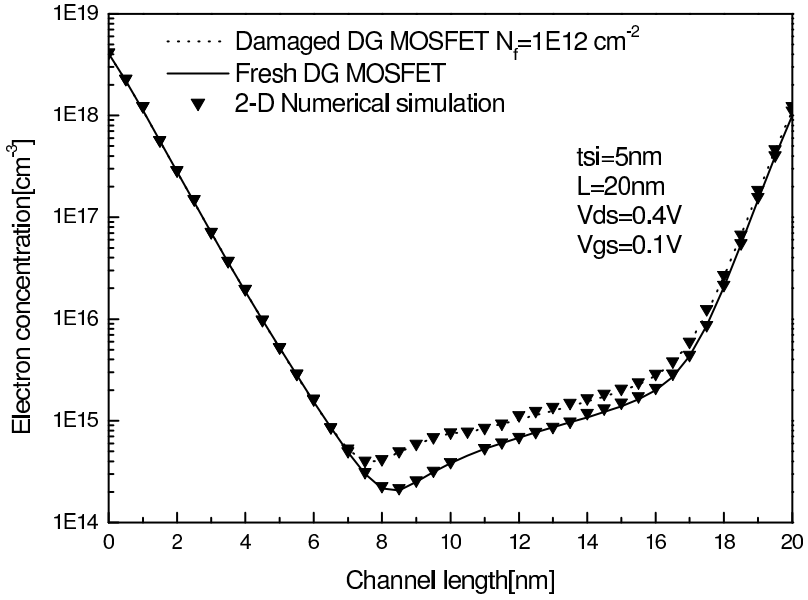
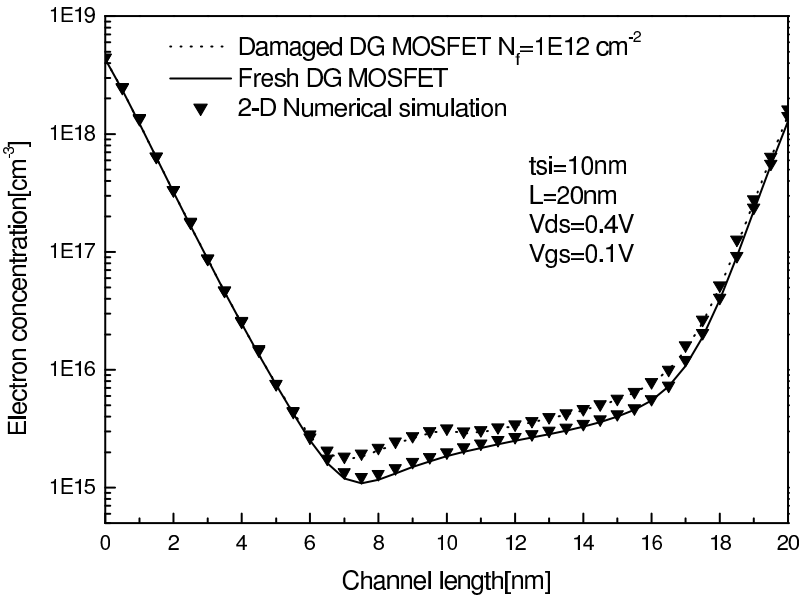


Figure 5.2: Surface potential distribution for the analyzed DG MOSFET with and without interfacial traps including free carriers effects ($L_1 = L/2$, $t_{ox} = 1nm$, $t_{si} = 5nm$, $N_A = 10^{16}\text{cm}^{-3}$ and $L = 20nm$)



(a)



(b)

Figure 5.3: Interface charges' concentrations along the channel length for different silicon film thicknesses for the analyzed DG MOSFET with and without interfacial traps including free carriers effects ($L_1 = L/2$, $t_{ox} = 1nm$, $N_A = 10^{16}\text{cm}^{-3}$ and $L = 20nm$) (a) $t_{si} = 5nm$, (b) $t_{si} = 10nm$

Figures 5.3(a) and 5.3(b) show the variation of the interface charges' concentrations along the channel for different channel thicknesses. It is clearly shown, in Figure 5.3(a)

and 5.3(b), that as the channel thickness increases, the carrier concentration increases, which means that with a little gate voltage bias, a greater amount of charge carriers accumulate near the metal-semiconductor interface, causing depletion and thereby inversion to take place quickly, resulting in lower threshold voltages and higher subthreshold swing factor. It is shown that the model calculations are in good agreement with the simulation results for a wide range of channel thicknesses.

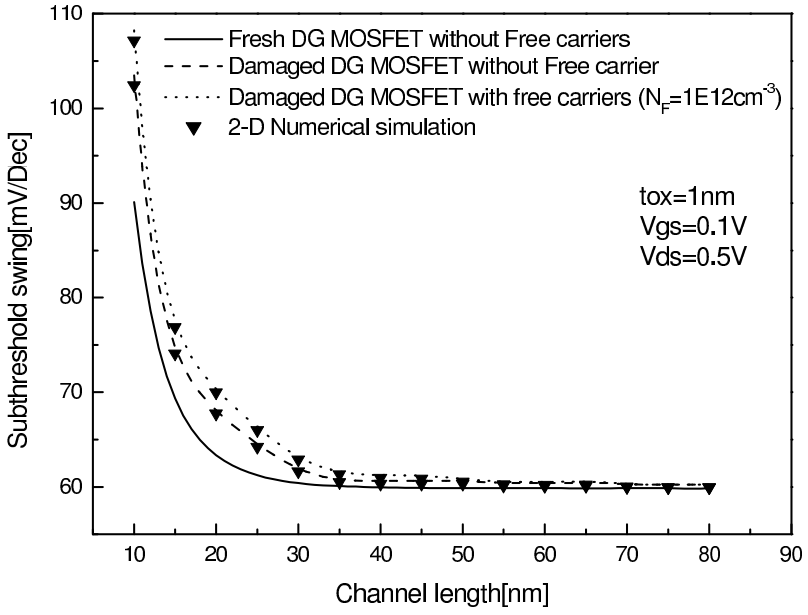


Figure 5.4: Calculated subthreshold swing for the DG MOSFET with and without traps as a function of channel length including free carriers effects ($L_1 = L/2$, $t_{ox} = 1nm$ and $t_{si} = 5nm$, $N_A = 10^{16}\text{cm}^{-3}$)

Figure 5.4 shows the model and simulated values of subthreshold swing plotted against channel length, L, for fixed values of $L_1 = L/2$, $t_{ox} = 1nm$ and $t_{si} = 5nm$. Comparison with the simulated results shows clearly that the conventional subthreshold swing model, without free carriers effects, underestimates the subthreshold swing parameter, however an improved agreement with the simulation results [139] is obtained when the free carrier effect is considered. It is also observed that the subthreshold swing parameter in the damaged device doesn't differ considerably from that of the fresh device for longer channel lengths. However, this difference becomes more apparent for very short channel length

devices (less than 40 nm). This observation can be explained by the effect of the hot-carrier induced localized interface charge density on the minimum potential value in weak inversion regime for short channel length devices.

It is clearly shown, in Figure 5.5, that the subthreshold swing is increased with the increasing of the channel thickness, where the subthreshold swing parameter becomes more pronounced with increasing the channel thickness. However, for thinner silicon films the subthreshold swing parameter degradation becoming less severe due to the better gate control of the free carrier in the channel. In addition, the inclusion of the free carriers effects to study the subthreshold transport in nanoscale transistors, with thick channel thickness, has major role in determining the subthreshold parameters behavior due to the extra surface potential generated at the channel/oxide interface, which may affect the electric field and carriers transport in weak inversion regime.

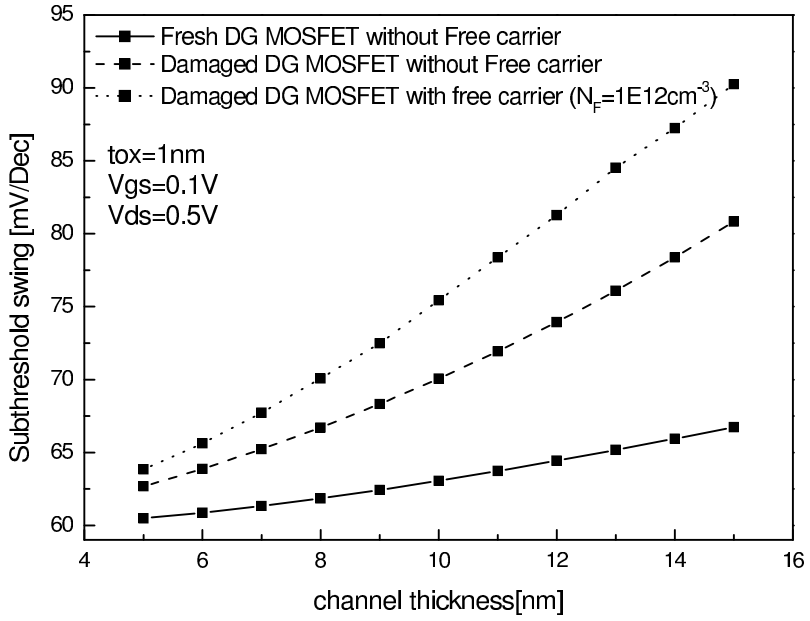


Figure 5.5: Variation of Subthreshold swing with channel thickness for DG MOSFET including interfacial traps and free carriers effects with ($L_1 = L/2$, $t_{ox} = 1nm$, $N_A = 10^{16}\text{cm}^{-3}$ and $L = 30nm$)

It is to note that the quantum mechanical effects (QMEs) of both spatial confinement and field confinement are neglected. QMEs have been researched in the literature; see for

example Ref. [124], the authors claimed that, QMEs were small for the devices with t_{si} less than 5nm. In Ref. [172], the authors concluded that, for the undoped DG MOSFETs, QMEs would not affect the subthreshold swing greatly as long as t_{si} was not much less than 5nm. Therefore the justification of the negligence of QMEs in this work is that the silicon body thickness is large (t_{si} more than 5nm) and the device is under weak inversion condition, thus energy quantization, spatial confinement and field confinement are negligible.

5.3 Gradual Channel Gate Stack DG MOSFETs

The improvement of the MOSFET structure is a challenge against the parasitic phenomena appearing when the channel length shrinks down to nanoscale level. Among the undesirable problems appearing because of miniaturization we cite the short channel effects (SCE) which is basically caused by the influence of the drain potential on the gate control over the channel. Thus, the subthreshold behaviour is obviously affected and became strongly dependent on channel length.

The Graded Channel Gate Stack Double Gate (GCGSDG) MOSFET has been considered as one of the most promising designs for the scaling of CMOS technology down to the nanometer range [157]. This is mainly due to the superior control of short channel effects (SCEs) because of the reduced influence of the drain voltage on the channel charge.

The main goal of this section is to investigate the subthreshold behaviour of our proposed Graded Channel Gate Stack Double Gate MOSFET (GCGS DG MOSFET) structure. The disadvantages offered by the conventional MOSFET especially in nanoscale regime can open the way to examine the possibility of developing new models improviving the performances of our structure under different combined constraints. The proposed approach for developing subthreshold models is based on the surface-potential formalism, which will not only enable the accurate description of the GCGS DG MOSFET behavior, but will also facilitate the incorporation of new added conditions to the whole approach when needed. In addition, the effect of different design parameters on each subthreshold

parameter, especially the swing factor and the OFF current, has been analyzed to determine which design model meets the high speed commutation requirement closely for digital application.

5.3.1 Description of the studied structure

A detailed view of nanoscale GCGSDG MOSFET is depicted in Figure 5.6. The whole channel is constituted of two regions low and high doping concentration regions N_{AL} and N_{AH} respectively. The total channel length of the device is L, the length of the low doping region is denoted by L_1, thus, the length of the high doping region can be deduced by $L - L_1$. the structure is totally symmetric with a double-layer gate stuck, oxide and high-k layer. The doping level of the drain and source sides is given by: N_D and N_S respectively.

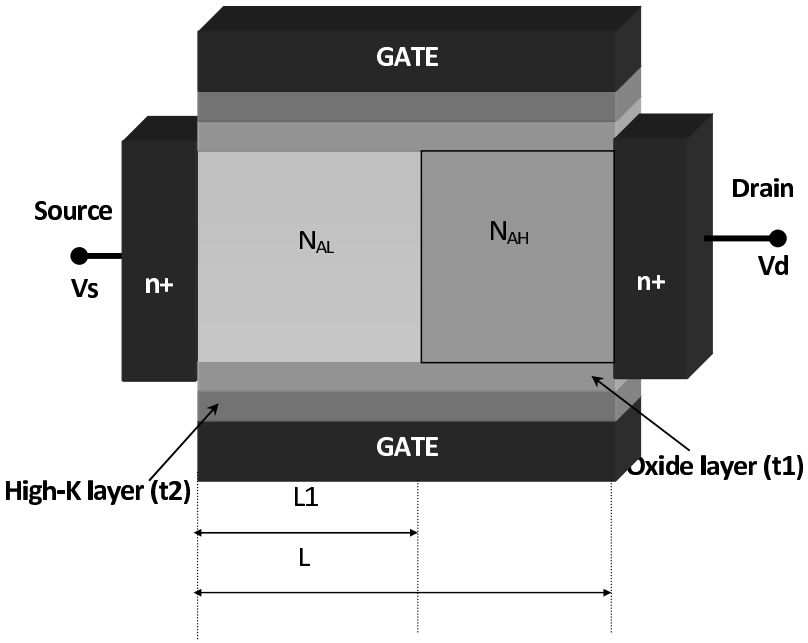


Figure 5.6: Cross-sectional view of the GCGSDG MOSFET proposed inner structure

5.3.2 Model formulation

Refer to Figure 5.6, the 2-D Poissons equation for the channel region, without free carriers and traps effects, is given by,

$$\frac{\partial^2 \psi(x,y)}{\partial x^2} + \frac{\partial^2 \psi(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si}} \tag{5.15}$$

subject to the boundary conditions,

$$\varepsilon_{ox}\frac{V_{F,eff} - \psi(x,0)}{t_{oxeff}} = \varepsilon_{si}\left.\frac{\partial \psi(x,y)}{\partial y}\right|_{y=0} \tag{5.16a}$$

$$\varepsilon_{ox}\frac{V_{B,eff} - \psi(x,t_{si})}{t_{oxeff}} = \varepsilon_{si}\left.\frac{\partial \psi(x,y)}{\partial y}\right|_{y=t_{si}} \tag{5.16b}$$

$$\psi(0,y) = V_{bi} \tag{5.16c}$$

$$\psi(L,y) = V_{bi} + V_{ds} \tag{5.16d}$$

So, we are required to resolve the boundary problem separately according to each region after adding a new condition defining the transition point from region I to region II by,

$$\psi(L_1,y) = V_p \tag{5.17}$$

where ε_{ox} is the oxide permittivity, t_{si} is the thickness of silicon channel. V_{bi} is the junction voltage between the source/drain and intrinsic silicon with $V_{bi} = (kT/q)\ln\left(N_{D/S}/n_i\right)$, n_i is the intrinsic silicon density and V_{ds} is the drain to source voltage.

The introduction of effective voltages at the front and bottom gates allow to alleviate derivations for symmetric structure as follows,

$$V_g^* = V_{F,eff} = V_{B,eff} = V_{gs} - \phi_{ms} \tag{5.18}$$

where ϕ_{ms} is the gate work function referenced to intrinsic silicon and V_{gs} represents the gate source voltage.

The effective oxide layer thickness of insulator layer t_{oxeff} is given by the superposition

of the thickness of the SiO_2 layer t_1 ($\varepsilon_{ox} = \varepsilon_1$) and the thickness of the high-k layer t_2 (ε_2) as follow,

$$t_{oxeff} = t_1 + (\varepsilon_1/\varepsilon_2) \cdot t_2 \tag{5.19}$$

Young's pioneer work showed that by taking a particular profile for the potential distribution, many simplifications are provided in term of computational complexity [173]. By adopting the same scheme expressed by a parabolic profile as,

$$\psi(x,y) = a(x) + b(x)\, y + c(x)\, y^2 \tag{5.20}$$

We can transform our initial boundary problem to an ordinary differential equation that is much easier to resolve. After application of the boundary conditions and $\frac{\partial \psi(x,y)}{\partial y}\Big|_{y=t_{Si}/2} = 0$ known as the symmetry condition, yields the formula describing the channel potential distribution,

$$\psi(x,y) = \psi(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_s(x) - V_g^*}{t_{oxeff}} y - \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\psi_s(x) - V_g^*}{t_{oxeff} t_{Si}} y^2 \tag{5.21}$$

where $\psi_s(x)$ represents the surface potential at Si/SiO_2 frontiers given by $y = 0$ and $y = t_{si}$.

Substituting (5.21) in (5.15), an ordinary differential equation dealing only with the surface potential is obtained,

$$\frac{d^2\psi_s(x)}{dx^2} - \frac{1}{\lambda^2}\psi_s(x) = D \tag{5.22}$$

The general solution of such equation is the sum of the complementary solution given by $A_1 e^{\frac{x}{\lambda}} + A_2 e^{-\frac{x}{\lambda}}$ associated with the homogeneous equation and the particular solution easily guessed to be $-\lambda^2 D$. Thus, the general solution of Eq. (5.22) has the form $\psi_s(x) = -\lambda^2 D + A_1 e^{\frac{x}{\lambda}} + A_2 e^{-\frac{x}{\lambda}}$ where A_1 and A_2 are constants determined by satisfying the boundary conditions,

In region I ($0 \leq x \leq L_1$) the equation to be solved is:

$$\frac{d^2\psi_{s1}(x)}{dx^2} - \frac{1}{\lambda^2}\psi_{s1}(x) = D_1 \tag{5.23}$$

with $\lambda^2 = \frac{\varepsilon_{si} \cdot t_{oxeff} t_{si}}{2\varepsilon_1}$ and $D_1 = \frac{qN_{AL}}{\varepsilon_{si}} - \frac{1}{\lambda^2}V_g^*$

In region II ($L_1 \leq x \leq L$) the equation to be solved is:

$$\frac{d^2\psi_{s2}(x)}{dx^2} - \frac{1}{\lambda^2}\psi_{s2}(x) = D_2 \tag{5.24}$$

with $D_2 = \frac{qN_{AH}}{\varepsilon_{si}} - \frac{1}{\lambda^2}V_g^*$

After some mathematical manipulations, according to the boundary conditions reported in (5.16c), (5.16d) and (5.17), we deduce the surface potential in both regions as,

$$\psi_{s1}(x) = -\lambda^2 D_1 + \frac{\phi_{D1}\sinh\left(\frac{x}{\lambda}\right) - \phi_{s1}\sinh\left(\frac{x-L_1}{\lambda}\right)}{\sinh\left(\frac{L_1}{\lambda}\right)} \tag{5.25}$$

with $\phi_{D1} = V_p + \lambda^2 D_1$ and $\phi_{s1} = V_{bi} + \lambda^2 D_1$

$$\psi_{s2}(x) = -\lambda^2 D_2 + \frac{\phi_{s2}\sinh\left(\frac{x-L_1}{\lambda}\right) - \phi_{D2}\sinh\left(\frac{x-L}{\lambda}\right)}{\sinh\left(\frac{L-L_1}{\lambda}\right)} \tag{5.26}$$

with $\phi_{D2} = V_p + \lambda^2 D_2$ and $\phi_{s1} = V_p + \lambda^2 D_1$

In order to calculate the subthreshold swing factor it is important to determine first the minimum surface potential according to $\psi_{s\,\min} = \min(\psi_{s1\,\min}, \psi_{s2\,\min})$.

The location of the minimum surface potential along the channel is obtained by solving the basic equation for both subregions,

$$\frac{\partial\psi_{s1,s2}(x)}{\partial x} = 0 \tag{5.27}$$

After solving this equation, we get the following results:

$$x_{\min 1} = \frac{1}{2}\left[L_1 - \lambda \ln\left(\frac{\phi_{s1} - \phi_{D1}e^{\frac{L_1}{\lambda}}}{\phi_{D1} - \phi_{s1}e^{\frac{L_1}{\lambda}}}\right)\right] \tag{5.28}$$

$$\psi_{s1\,\min} = -\lambda^2 D_1 + \frac{\phi_{D1}\sinh\left(\frac{x_{\min 1}}{\lambda}\right) - \phi_{s1}\sinh\left(\frac{x_{\min 1}-L_1}{\lambda}\right)}{\sinh\left(\frac{L_1}{\lambda}\right)} \tag{5.29}$$

$$x_{\min 2} = \frac{1}{2}\left[L_1 + L + \lambda \ln\left(\frac{\phi_{D2}e^{\frac{L}{\lambda}} - \phi_{s2}e^{\frac{L_1}{\lambda}}}{\phi_{s2}e^{\frac{L}{\lambda}} - \phi_{D2}e^{\frac{L_1}{\lambda}}}\right)\right] \tag{5.30}$$

$$\psi_{s2\,\min} = -\lambda^2 D_2 + \frac{\phi_{s2}\sinh\left(\frac{x_{\min 2}-L_1}{\lambda}\right) - \phi_{D2}\sinh\left(\frac{x_{\min 2}-L}{\lambda}\right)}{\sinh\left(\frac{L-L_1}{\lambda}\right)} \tag{5.31}$$

The key electrical parameters for digital applications that indicate the impact of short-channel effects on a MOSFET are the subthreshold swing (S) and the OFF-state current. The subthreshold swing is defined as the required change in gate voltage that results in an order-of-magnitude change in the subthreshold drain current. Assuming that the drain current I_{ds} is proportional to the total amount of the free carrier at the virtual cathode and their density follows the Boltzmann distribution function [157], [160], [174], the general subthreshold swing (S) model is given by:

$$S = \frac{kT}{q}\ln(10) \times \left[\frac{\partial \psi_{s1\,\min}}{\partial V_{gs}}\right]^{-1} \tag{5.32}$$

The subthreshold swing can be given as,

$$S = S_0\left[1 + \Delta S\right]^{-1} \tag{5.33}$$

where $S_0 = 60\text{mV/dec}$ represents the ideal value of the subthreshold swing which is defined as the subthreshold swing for long channel devices, and ΔS is the subthreshold swing degradation coefficient given as,

$$\Delta S = \frac{\left((\alpha+\beta) - \sinh\left(\frac{L_1}{\lambda}\right) - \sinh\left(\frac{L-L_1}{\lambda}\right) - \sinh\left(\frac{L}{\lambda}\right)\right)\gamma + \sinh\left(\frac{x_{\min 1}-L_1}{\lambda}\right)}{\sinh\left(\frac{L_1}{\lambda}\right)} \tag{5.34}$$

with $\alpha = \sinh\left(\frac{L_1}{\lambda}\right)\cdot\cosh\left(\frac{L_1-L}{\lambda}\right)$, $\beta = \sinh\left(\frac{L-L_1}{\lambda}\right)\cdot\cosh\left(\frac{L_1}{\lambda}\right)$ and $\gamma = \frac{\sinh\left(\frac{x_{\min 1}}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}$
where $\lambda = \sqrt{\frac{\varepsilon_{si}\cdot t_{oxeff}\cdot t_{si}}{2\cdot\varepsilon_1}}$ represents the natural length of the studied device and $x_{\min 1}$ defined previously depends on electrical and geometrical parameters of the GCGSDG

MOSFET.

In the weak inversion region, the current is principally diffusion dominated and proportional to the electron concentration at the virtual cathode. Therefore, the subthreshold current derived for our GCGS DG MOSFET can be expressed as,

$$J_n(y) = qD_n \frac{n_{\min}(y)}{L}\left(1 - e^{V_{ds}/V_t}\right) \tag{5.35}$$

where D_n represents the diffusion constant and V_t is the thermal voltage. After some mathematical manipulations, a simple closed form of the subthreshold current can be given [157] as,

$$I_{sub} = 2\frac{V_t}{Es}(K_1(e^{\frac{\psi_{\min}}{V_t}} - e^{\frac{\psi^s_{\min}}{V_t}}) + K_2(e^{\frac{\psi_{\min}}{V_t}} - e^{\frac{\psi^s_{\min}}{V_t}})) \tag{5.36}$$

where Es represents the constant electric field, $Es = 2(\psi_{\min} - \psi^s_{\min})/t_{si}$, $\psi^s_{\min}$ is the minimum potential at (Si/SiO_2) interface given by $\psi^s_{\min} = \psi_{\min}(x_{\min}, 0)$, $\psi_{\min}$ represents the minimum potential,$\psi_{\min} = \psi(x_{\min}, t_{si}/2)$ and K_i is a constant defined as,

$$K_1 = (q\mu_n W V_t n_i^2 / L_1 N_{AL})(1 - e^{-V_P/V_t}) \tag{5.37a}$$

$$K_2 = (q\mu_n W V_t n_i^2 / (L - L_1) N_{AH})(1 - e^{-(V_{ds} - V_P)/V_t}) \tag{5.37b}$$

with W is the width of the GCGSDG MOSFET.

5.3.3 Miltiobjective-based optimization

The most important propriety of MOGA is the global searching by population of solutions, instead one solution, that correspond to each point in the search space. So, this approach require several objective functions which form a complex problem to be solved in order to give rise the best compromise among the various objective functions.

An ideal multi-objective optimization procedure is constituted of two steps. The first is to find some optimal solutions corresponding to multiple objectives considered in search space. The next step is to choose the most suitable solution by using higher level information. Due to the simple mechanism and high performance provided by MOGA

for multi-objective global optimization, MOGA can be applied to study the nanoscale GCGSDG MOSFETs. In the present study, Pareto approach can be a suitable choice. Pareto approach searches non-dominant solutions called Pareto optimal solutions in the objective space. The number of Pareto optimal solutions is always not single [156, 175]. The objective in the design of optimal GCGSDG MOSFET for digital CMOS-based devices is to find the better configuration of the transistor that satisfies the high working performances in subthreshold regime.

5.3.4 Computation methodology

The first step of our approach consists of compact models of subthreshold parameters for short channel GCGSDG MOSFETs. It is to note that this structure is proposed by our team [52]. Using the SILVACO software [139] for validation of the developed analytical models, it was observed that the formulated analytical subthreshold parameters models can be used as objective functions, which are given as function of input design variables. Based on the linearity dependence, between the subthreshold swing and both parameters threshold voltage roll-off and DIBL, given in [160], the optimization of the subthreshold behavior can be reduced from four MOGAs problem to two objective functions. Therefore, two objectives are considered in this study, i.e. subthreshold swing degradation coefficient and OFF-state current. Considered the objectives, a mixture model is formulated below:

- Minimize $\Delta S(x) = \frac{\left((\alpha+\beta)-\sinh\left(\frac{L_1}{\lambda}\right)-\sinh\left(\frac{L-L_1}{\lambda}\right)-\sinh\left(\frac{L}{\lambda}\right)\right)\gamma+\sinh\left(\frac{x_{\min 1}-L_1}{\lambda}\right)}{\sinh\left(\frac{L_1}{\lambda}\right)}$
- Minimize $I_{sub}(x)|_{V_{gs}=0} = 2\frac{V_t}{Es}(K_1(e^{\frac{\psi_{\min}}{V_t}} - e^{\frac{\psi^s_{\min}}{V_t}}) + K_2(e^{\frac{\psi_{\min}}{V_t}} - e^{\frac{\psi^s_{\min}}{V_t}}))$

where x represents the input variables vector which is given as, $x = (t_{si}, t_1, t_2, \varepsilon_2, L, L_1, N_{AH}, N_{AL})$.

The overall objective function is obtained by given weightage based on Weighted-sum approach as follows:

$$F(x) = w_1 \Delta S(x) + w_2 \, I_{sub}(x)|_{V_{gs}=0} \tag{5.38}$$

where w_i (i=1-2) are weight functions satisfy $\sum_i w_i = 1$.

If high speed and low power dissipation transistor (high frequency digital applications) is the device produced by this process, then both subthreshold swing and OFF-state current are equally important. Hence, w_1 and w_2 can be assigned equal values as 0.5. Lower values of subthreshold swing, threshold voltage roll-off and DIBL are needed to design high speed transistor and lower value of OFF-state current is needed to improve the power dissipation and tunnel current of the device. It is to note that the optimization of the subthreshold swing factor leads to increase of the ON-state current, and therefore an increasing of the ratio can be obtained by our approach. Given the clearly defined problem to be solved, the adopted MOGA works following the steps given by the algorithm 3 [156].

The MOGA parameters were varied and the associated optimization error was recorded (see Table 5.1).

Table 5.1: Parameters used for MOGA-based computation

MOGA parameters	**Values**
Population size	120
Maximum number of generations	500
Selection	Tournament
Crossover	Scattered
Mutation	Adaptive feasible
Crossover fraction	0.8
Mutation rate	0.01

5.3.5 Results and discussion

For this configuration, the fitness function, overall objective function, was 6×10^{-3} and almost 100% of the submitted cases were learnt correctly. This resulted in 60 000 parameter set evaluations, and took about 62s to complete using Windows XP with Pentium IV (1.5 GHz).

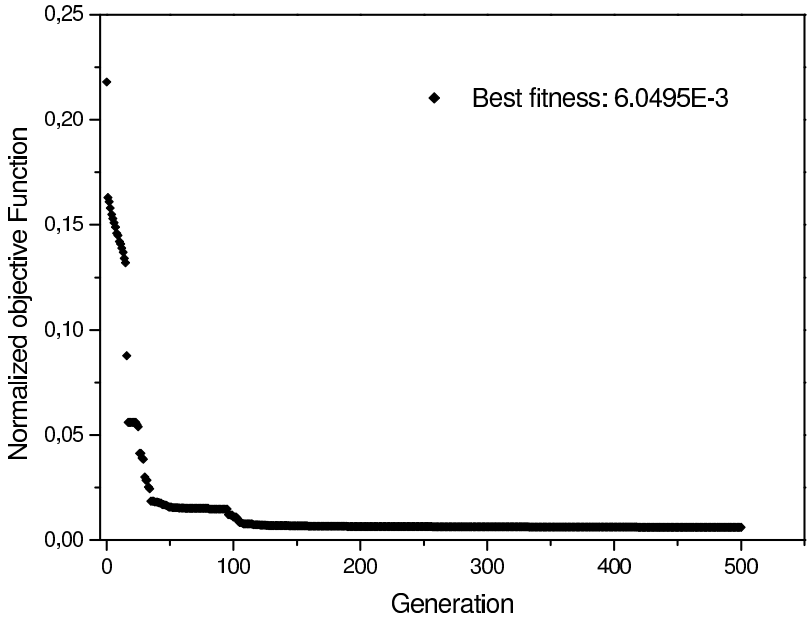


Figure 5.7: Variation of normalized overall objective function with generations

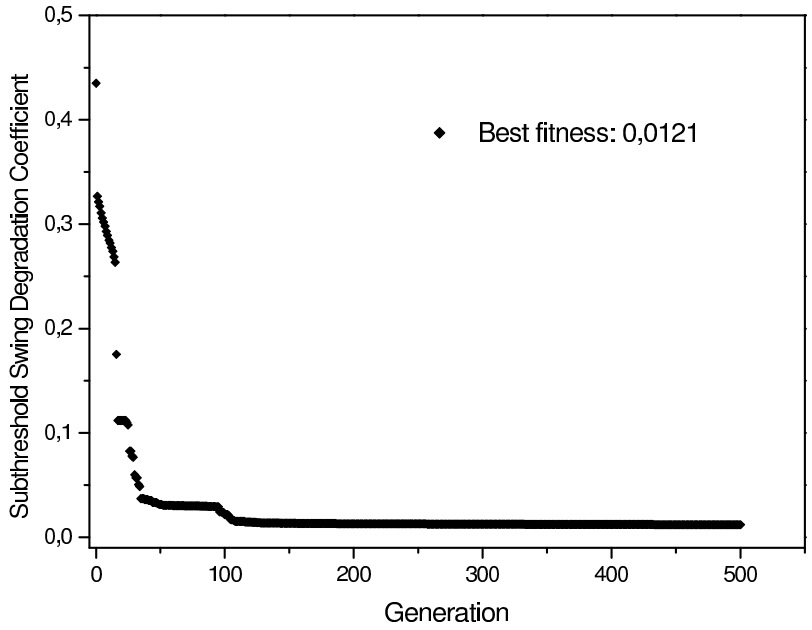


Figure 5.8: Variation of subthreshold swing degradation coefficient with generations

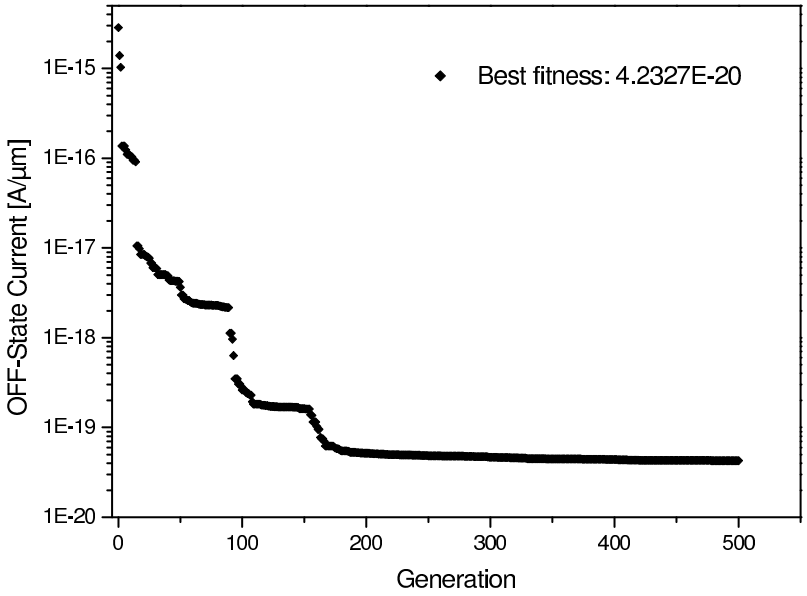


Figure 5.9: Variation of OFF-state current with generations

Figures 5.7, 5.8, 5.9 show the variation of minimum overall fitness function, optimized subthreshold swing degradation coefficient and optimized OFF-state current with generation for a maximum generation of 500.

The steady decrease in both subthreshold swing degradation coefficient and optimized OFF-state current of the best solution in each generation until it reaches a best possible value can be attributed to the selection procedure used namely tournament selection. Final optimized (GCGSDG) MOSFET parameters are summarized in Table 5.2, in which random device parameters are introduced to show the impact of the proposed approach on the improvement of the subthreshold behavior of GCGS DG MOSFET. As it is shown in Table 5.2, the obtained high-k dielectric material, for the optimized design, is the *SrTaxOz* alloy [176]. It is to note that the gate material used in our study is the n^+-Polysilicon with the work function $\phi_M = 4.2eV$, and all simulations were carried out in the subthreshold regime with $V_{gs} = 0.1V$ and $V_{ds} = 0.1V$.

Table 5.2: GCGSDG MOSFET design parameters for $V_{gs} = 0.1V$ and $V_{ds} = 0.5V$

		Random design (Case1)	Random design (Case2)	Random design (Case3)	**Optimized design**
Design parameters	NAH (cm^{-3})	10^{16}	5×10^{16}	8×10^{16}	**9.28** $\times 10^{16}$
	$N_A L$ (cm^{-3})	10^{15}	10^{15}	2×10^{15}	**5** $\times 10^{15}$
	t_{si} (nm)	8	5	10	**5.00**
	t_2 (nm)	2	1.5	2.5	**1.32**
	t1 (nm)	1.5	3	2.5	**1.00**
	L (nm)	12	20	30	**30.00**
	ε_2	40	35	20	**39.58**
	L_1 (nm)	6	8	15	**14.50**
Obtained Subthreshold performances values	S (mV/dec)	129.15	81.94	77.08	**60.60**
	I_{OFF} (A/ μm)	3.31×10^{-3}	3.06 × 10-8	7.01×10^{-9}	**4.23** $\times 10^{-13}$
	$V_{roll-off}$ (V)	-0.13	-0.036	-0.01	**-1.18** $\times 10^{-5}$
	DIBL (mV/V)	212.2	54.25	23.15	**0.06**
	I_{ON} (A/ μm)	3.87×10^{-3}	6.1×10^{-3}	6.48×10^{-3}	**8.3** $\times 10^{-3}$
	V_{th} (V)	0.45	0.46	0.53	**0.54**
	I_{ON}/I_{OFF}	1.16	1.99×10^5	9.24×10^5	**1.96** $\times 10^{10}$

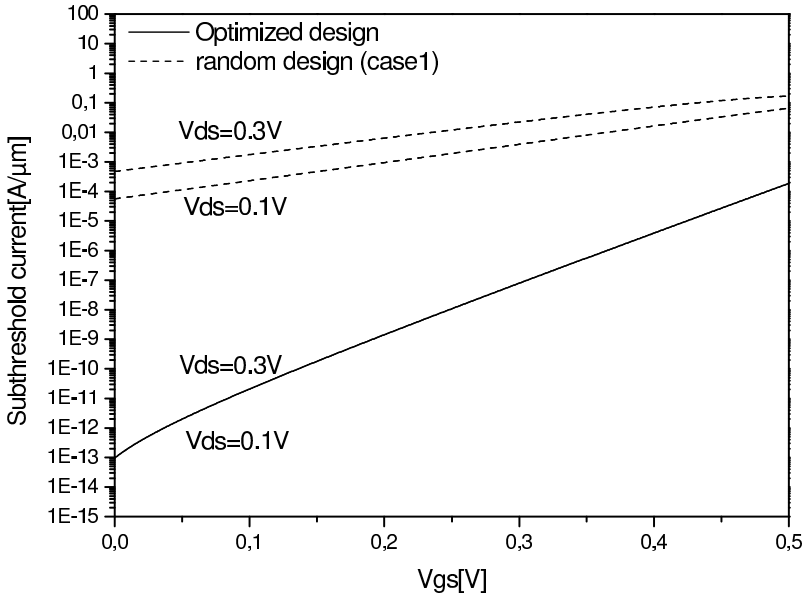


Figure 5.10: Subthreshold drain current variation as function of gate and drain voltages for different device configurations

Figures 5.10 shows the impact of our MOGAs-based approach on the subthreshold drain current behavior. An improvement at the level of the subthreshold current is observed in this figure where the OFF-current is reduced from 10^{-4} $A/\mu m$ to 10^{-13} $A/\mu m$ and the ration I_{ON}/I_{OFF} is increased that means, providing low power dissipation and better switching characteristic required for digital application. It is clear shown that our device configuration, optimized input vector, provides the better subthreshold electrical performances.

5.4 Junctionless Gate All Around MOSFETs

It's widely recognized that Gate-All-Around (GAA) MOSFETs are considered among the most probable choices to continue CMOS performance boost beyond the conventional scaling frontiers. Such device offers high electrical performance in the subthreshold domain, optimal subthreshold swing and a low leakage current, which are the predominant factor limiting how far the downscaling can be achieved. However, the formation of ultra-sharp and super shallow source/drain junctions to suppress SCEs still imposes a constraint about the doping techniques and thermal budget. To avoid these constraints, junctionless (JL) FETs designs are considered as straightforward structures to eliminate some technical limitations of the nanoscale transistors such as ultra-abrupt junctions, allowing the fabrication of even shorter channel devices [84, 177–179].

Achieving a high electrical performance and device reliability in the subthreshold regime and especially in deeply scaled devices is an engineering challenge due to the limitation of the carrier transport mechanism in accumulation mode [180].

Although several previously published literatures have reported the long-channel analytical model for JL double-gate and surrounding-gate [84, 178–182], no short-channel subthreshold swing and natural length models about the JL device have been proposed.

In this work, we present an analytical investigation to study the subthreshold behavior of junctionless GAA MOSFET for nanoscale CMOS analog/digital applications. Based on 2-D analytical analysis, new subthreshold swing and natural length models for

short-channel JLGAA MOSFETs are proposed. The analytical analysis has been used to calculate the subthreshold swing and to compare the performance of the investigated design and conventional GAA MOSFET.

In the JLGAA MOSFET design, the channel region has the same doping polarity as the source and drain. So, the investigated design has no junctions and less variability in comparison to the conventional GAA MOSFET. The analytical models have been validated by 2-D numerical simulations [76]. The proposed analytical models are used to formulate the objectives functions, which are the pre-requisite of genetic algorithm computation. The overall objective function is formulated by means of a weighted sum approach to search for the optimal electrical and dimensional device parameters. The effect of different design parameters on each subthreshold parameter, especially the swing factor and the scaling capability, has been analyzed to determine which design model meets the ULP requirement closely for nanoscale CMOS-based applications.

It is to note that the quantum effects are important for a silicon thickness of less than 10 nm, which lead to reduce the channel charge density and to increase the threshold voltage [183]. These effects have not been taken into account in our work due to the excellent gate control of the channel, for thinner structures, which makes the electron distribution insignificant. Therefore, the quantum correction to the subthreshold swing is much smaller and becomes negligible [173].

5.4.1 Description of the studied structure

A cross-sectional view of nanoscale JLGAA MOSFET is shown in Figure 5.11, where N_D represents the high doping concentration of the channel, L is the channel length of the transistor. The structure is symmetric.

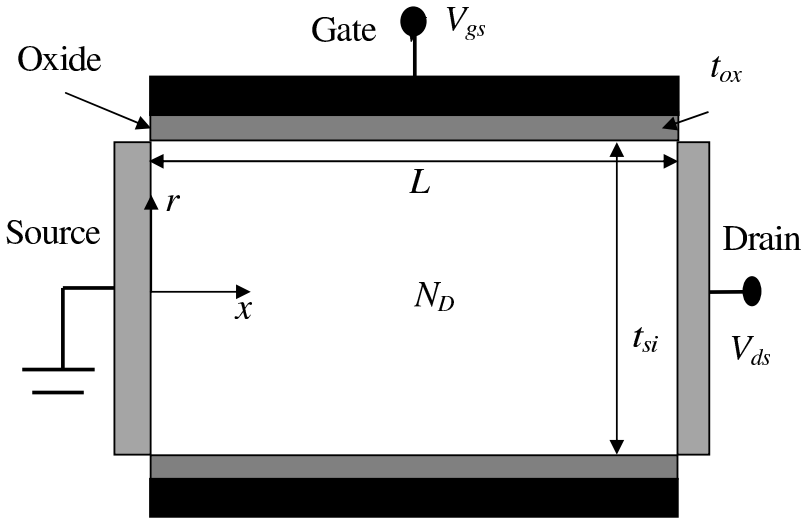


Figure 5.11: Cross-sectional view of the investigated JLGAA MOSFET, and the coordinate system

5.4.2 Model formulation

Referring to Figure 5.11, by accounting for the angular symmetry of the JLGAA MOSFET; the channel electrostatics potential is governed by the following 2-D Poisson equation:

$$\frac{\partial^2 \psi(x,r)}{\partial r^2} + \frac{1}{r}\frac{\partial \psi(x,r)}{\partial r} + \frac{\partial^2 \psi(x,r)}{\partial x^2} = \frac{-q \cdot N_D}{\varepsilon_{si}} \tag{5.39}$$

where $\psi(x,r)$ represents the 2-D channel potential, ε_{si} is silicon permittivity and q represents the electron charge. The boundary conditions for ψ are found by satisfying continuity of both the normal component of the electric displacement at the (Si/SiO_2) interfaces, and the potential at the source/drain sides.

Using the same parabolic potential profile in vertical direction as in [12,13] and applying the symmetry condition of $\partial\psi(x,r)/\partial r = 0$ for $r = 0$, we obtained the following expressions of 2-D channel potential for the investigated design as,

$$\psi(x,r) = \psi_s(x) + \frac{C_{ox}t_{si}}{4\varepsilon_{si} - 2C_{ox}t_{si}}\left(\psi_s(x) - V_g^*\right)r - \frac{2C_{ox}}{2\varepsilon_{si}t_{si} - C_{ox}t_{si}^2}\left(\psi_s(x) - V_g^*\right)r^2 \tag{5.40}$$

where $\psi(x)$ represents the surface potential (the potential at the Si/SiO_2 interface), ε_{ox} is

the oxide permittivity, t_{si} and t_{ox} are thicknesses of silicon channel and oxide, respectively. C_{ox} represents the gate oxide capacitance per unit area $C_{ox} = \frac{2\varepsilon_{ox}}{t_{si}\ln\left(1+2\frac{t_{ox}}{t_{si}}\right)}$, where V_g^* is the effective applied gate voltage given by $V_g^* = V_{F,eff} = V_{B,eff} = V_{gs} - \phi_{MS}$, with V_{gs} and ϕ_{MS} represent the applied gate voltage and the gate work function referenced to intrinsic silicon, respectively. For the symmetric structure, the electric field in the radial direction is symmetric with respect to $r = 0$.

In Eq. (5.40), accounting for effective conducting path effect (ECPE), where the most leakage path $r = d_{eff}$ is at the position between surface of $r = t_{si}/2$ and channel center of $r = 0$. For the high doping channel, which is our case, the ECP is given at the (Si/SiO_2) interface as $d_{eff} = t_{si}/2$ [184]. Therefore, our investigation will be focused on studying the surface potential behavior. In this context, an accurate surface potential modeling leads to the development of compact subthreshold swing and scaling length models.

Substituting Eq. (5.40) in Eq. (5.39), we obtain the differential equation that deals only with surface potential as follows,

$$\frac{d^2\psi_s(x)}{dx^2} - \frac{1}{\lambda^2}\cdot\psi_s(x) = D \tag{5.41}$$

where $D = \frac{-q\cdot N_D}{\varepsilon_{si}} - \frac{1}{\lambda^2}\cdot V_g^*$

From Eq. (5.41), the scaling natural length of the device can be given as $\lambda = \sqrt{\frac{2\varepsilon_{si}t_{si} - C_{si}t_{si}^2}{2\cdot C_{ox}}}$. It should be noted that for $t_{si}/2 >> t_{ox}$ (if $t_{si}/2 >> t_{ox}$ then $\ln(1+2t_{ox}/t_{si}) \approx 2t_{ox}/t_{si}$), a new expression of the scaling length for the JLGAA MOSFET can be reduced as,

$$\lambda = \sqrt{\frac{t_{si}\left(2\varepsilon_{si}t_{ox} + \varepsilon_{ox}t_{si}\right)}{8\varepsilon_{ox}}} \tag{5.42}$$

In Eq. (5.42), the scaling natural length is derived. It is worthy to point out that λ is dependent on the depth of the effective conducting path of d_{eff} corresponding to the channel doping and can be used to adjust the scaling design for different silicon channel doping.

The boundary conditions of the surface potential Figure 5.11 are given as,

$$\psi_s(x=0) = 0 \tag{5.43a}$$

$$\psi_s(x=L) = V_{ds} \tag{5.43b}$$

The general solution of the differential equation given in Eq. (5.42) can be found as,

$$\psi_s(x) = ae^{\frac{x}{\lambda}} + be^{-\frac{x}{\lambda}} - \lambda^2 D \tag{5.44}$$

Using the boundary conditions given in Eqs. (5.43a) and (5.43b), the coefficients a and b can be obtained as $a = (1-\alpha)\lambda^2 D + \beta V_{ds}$ and $b = \alpha\lambda^2 D - \beta V_{ds}$ where $\alpha = \frac{e^{\frac{L}{\lambda}}-1}{2\sinh\left(\frac{L}{\lambda}\right)}$ and $\beta = \frac{1}{2\sinh(L/\lambda)}$

After some mathematical manipulations, a closed form of the surface potential can be expressed as,

$$\psi_s(x) = \frac{\left[\sinh\left(\frac{x}{\lambda}\right) - \sinh\left(\frac{x-L}{\lambda}\right) - \sinh\left(\frac{L}{\lambda}\right)\right]\lambda^2 D + \sinh\left(\frac{x}{\lambda}\right)V_{ds}}{\sinh\left(\frac{L}{\lambda}\right)} \tag{5.45}$$

To calculate the subthreshold swing, we need to find the potential minimum along the channel. The position of minimum surface potential, x_{min}, is calculated by differentiating Eq. (5.44) and equating the resulting expressions to zero. The position of the minimum surface potential and minimum surface potential are then obtained from Eq. (5.44) as,

$$x_{\min} = \frac{\lambda}{2}\ln\frac{b}{a} \tag{5.46}$$

$$\psi_{s\,\min} = 2\sqrt{ab} - \lambda^2 D \tag{5.47}$$

One of the biggest challenges in downscaling of deep submicron scale FETs designed for ultra-low power and high speed application is the control of subthreshold drain current for deep submicron channel lengths. A steep subthreshold slope is attractive for the ease of switching the transistor current off. In this context, the subthreshold swing parameter is considered an important factor which affects the turn-off characteristic of the device.

Assuming that the subthreshold drain current is proportional to the total amount of the free carrier at the virtual cathode and their density $n_{\min}(r)$ follows the Boltzmann function, a general subthreshold swing (S) model is obtained [185, 186] as,

$$S = \frac{kT}{q}\ln(10)\left[\frac{\partial \psi_{s\,\min}}{\partial V_{gs}}\right]^{-1} \tag{5.48}$$

where k and T represent the Boltzmann constant and the temperature, respectively.

From Eq. (5.47) and Eq. (5.48), a closed form expression for subthreshold swing the JLGAA MOSFETs is obtained by Eq. (5.49a) and for $L > \lambda$ a simplified expression of S can be given by Eq. (5.49b).

$$S = \frac{kT}{q}\ln(10)\left[1 + \frac{2\alpha\left(\alpha-1\right)\lambda^2 D + \left(1-2\alpha\beta\right)V_{ds}}{\sqrt{\alpha\left(1-\alpha\right)\lambda^4 D^2 - \beta^2 V_{ds}^2 + \left(2\alpha\beta+\beta\right)\lambda^2 D V_{ds}}}\right]^{-1} \tag{5.49a}$$

$$S_L = \frac{kT}{q}\ln(10)\left[\frac{\sqrt{e^{\frac{L}{\lambda}} q N_D^2 V_{ds} - V_{ds}^2}}{V_{ds}e^{\frac{-L}{\lambda}} + \sqrt{e^{\frac{L}{\lambda}} q N_D^2 V_{ds} - V_{ds}^2}}\right]^{-1} \tag{5.49b}$$

From Eq. (5.49b), it is clearly shown that for long channel devices ($L >> \lambda$) the subthreshold swing reaches its ideal value (S=60mV/dec) [187].

5.4.3 Results and discussion

To validate the proposed models, the 2-D device simulator (SILVACO) is used to simulate the device [139]. Figure 5.12 plots the subthreshold swing as a function of the device dimensions, length and thickness, calculated from our analytical model. The subthreshold swing is predicted for both designs, JL and conventional GAA MOSFETs, and compared for equal electrical and geometrical parameters.

It is clearly shown that the subthreshold swing is improved by the increasing of channel length. In comparison to the thick silicon film with $t_{si} = 10nm$, the thin one with $t_{si} = 5nm$ will efficiently improve the subthreshold swing, particularly when the effective channel length is further scaled to $10nm$. It can also be shown that the subthreshold

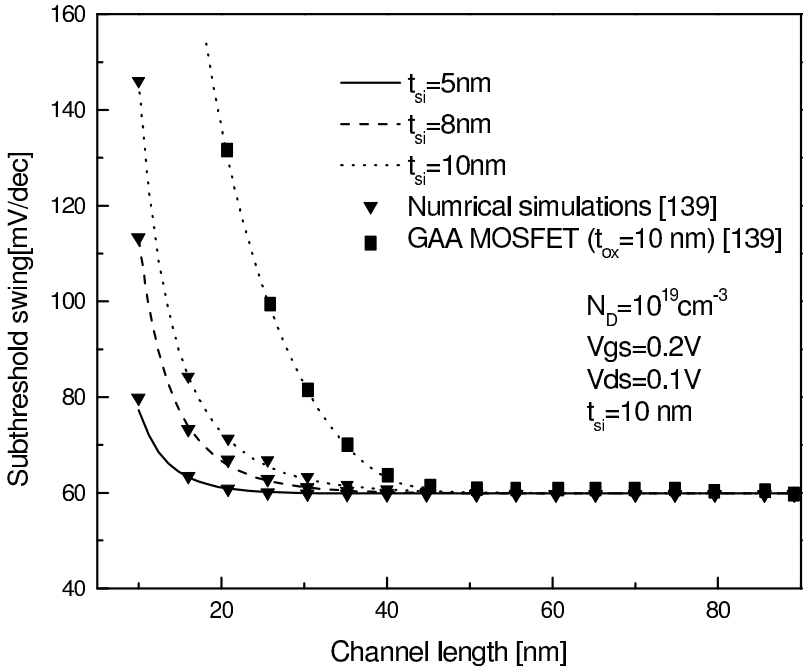


Figure 5.12: Subthreshold swing versus channel length with various silicon thicknesses ($t_{ox} = 3nm, N_D = 10^{19}cm^{-3}, V_{gs} = 0.2V$ and $V_{ds} = 0.1V$

swing decreases slowly as the JLGAA MOSFET length up to high values, where the subthreshold swing reaches its optimal, better, value ($S = 60mV/Dec$) for Channel length $L \geq 35nm$. Contrary, the subthreshold swing decreases rapidly with the increasing of the channel length, in the case of the conventional GAA design. In this case, the subthreshold swing reaches its better value ($S = 60mV/Dec$) for Channel length $L \geq 40nm$. Due to no source/drain overlap on the channel region, the JLGAA design will suffer less SCEs and induce less subthreshold swing degradation than the GAA MOSFET. Therefore, the JLGAA exhibits better performance for subthreshold regime in comparison to the GAA MOSFET devices.

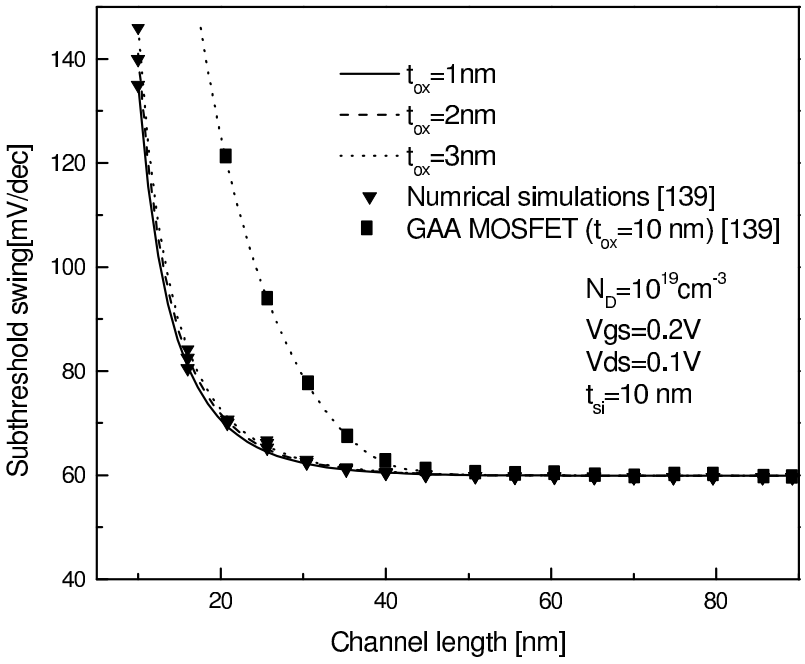


Figure 5.13: Subthreshold swing versus channel length with various oxide thicknesses ($t_{si} = 10nm, N_D = 10^{19}cm^{-3}, V_{gs} = 0.2V$ and $V_{ds} = 0.1V$

Figure 5.13 plots the subthreshold swing versus the channel length for different gate oxide thicknesses. The thinnest gate oxide thickness of $t_{ox} = 1nm$ exhibits the smallest subthreshold swing among the three oxide thicknesses of $t_{ox} = 1nm$, $2nm$ and $3nm$. Without the source/drain depletion regions in the channel, the JLGAA device increases the channel potential barrier and suppresses the SCEs more efficiently than the conventional GAA device. The obtained results from both designs (JLGAA and GAA MOSFETs) show that the JLGAA device offers significant improvement, in terms of subthreshold swing and scaling capability. Therefore, as device dimensions penetrate into the deep submicron domain, the improved obtained performance makes the JLGAA MOSFET a better choice for nanoscale ultra-low power CMOS-based applications.

5.4.4 Scaling capability

A small subthreshold swing is required to provide adequate values of the commutation speed and subthreshold transconductance, for ultra-low power application, so that

a JLGAA MOSFET can effectively work as switch or voltage amplifier in subthreshold regime. The subthreshold swing of a long channel JLGAA MOSFET has an ideal value ($S = 60mV/dec$). To have an acceptable performance, the subthreshold swing has to be close to the ideal value. The predicted results of analytical model are used to form a graphical abacus which allows the study of the scaling capability of the JLGAA MOSFET and the conventional GAA MOSFET as it is illustrated in Figure 5.14.

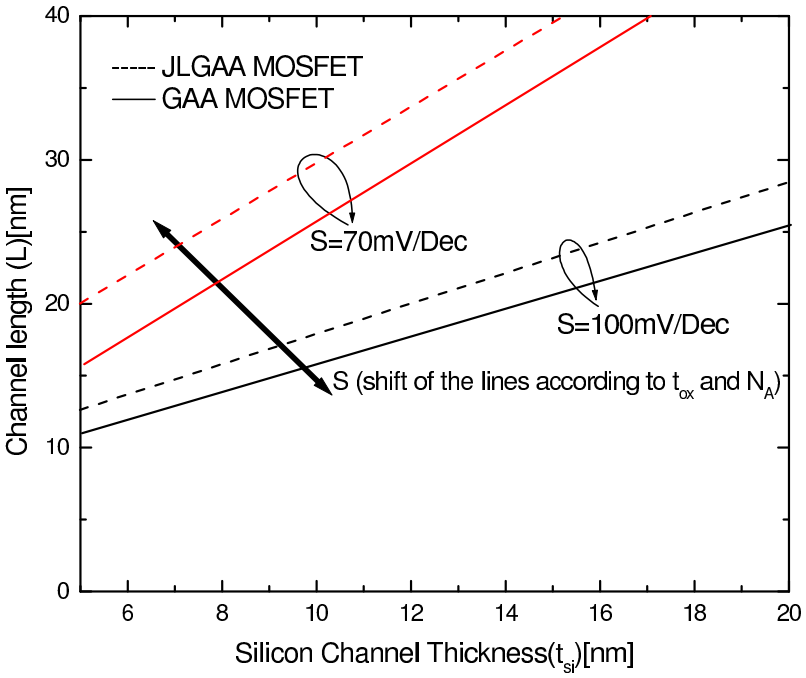


Figure 5.14: Design space for channel length versus silicon thickness for both JLGAA and GAA designs

The evolution of the subthreshold swing for the JLGAA MOSFET shows the effect of the junctionless design on the law of scaling capability of the GAA transistors. Clearly, $10nm$ JLGAA MOSFETs are likely to be used for the condition where $S = 70mV/dec$ is tolerable. The scaling capability is predicted for both designs and compared in Figure 5.14 for equal electrical and dimensional parameters. Clearly, the JLGAA MOSFET provides better scaling capability with respect to the conventional GAA MOSFET due to the better immunity to SCEs and small value of the scaling length. Also, the SCEs are improved as the transistor thickness is thin due to the higher gate to channel coupling

relative to source/drain to channel coupling.

The most important conclusion is that the JLGAA MOSFET can satisfy the same subthreshold swing value ($S = 70mV/dec$) as conventional GAA MOSFET with channel 10% shorter than that given by GAA MOSFET. This makes the JLGAA MOSFET a promising candidate for future technology nodes.

5.4.5 Multiobjective-based optimization

During the last decade, there has been a growing interest using evolutionary algorithm to optimize a variety of single and multi-objective problems in the field of engineering [148, 155, 156, 188]. Genetic algorithms have been shown to solve nonlinear and multivariable problems by exploring all regions of state space and exponentially exploiting promising areas through genetic operators like: selection, crossover and mutation, which will be applied to individuals in populations. In this part, we propose an approach based on Multiobjective Genetic Algorithms (MOGAs) computation used previously in Chapter 4 to optimize the subthreshold swing and the scaling capability of the JLGAA MOSFET for low power and analog applications. In our multi-objective optimization problem, multi-objective functions need to be optimized simultaneously. The implementation of the MOGA-based optimization follows the algorithm 3 used in Chapter 4.

The optimization process was performed for 20 population size using the following genetic operators: tournament selection, scarred crossover and uniform mutation. Two objective functions, which affect the device behavior for analog application, are considered in this study, i.e. subthreshold swing and the scaling length. The optimization of these parameters provides the best electrical performance, for analog applications, by satisfying of the following objective functions:

- Minimization of the subthreshold swing coefficient S.
- Minimization of scaling length λ.

The input normalized electrical and dimensional variables vector, which will be optimized using our approach, is given as $X = (t_{si}, L, t_{ox}, N_D, V_{gs}, V_{ds})$.

The constraints to be satisfied are:

- $g_1(x) : x \in [x_{i\,\min}, x_{i\,\max}]$, $x_i \in X$ (each design variable is confined within a given range).
- $g_2(x) : L > 2t_{si}$ (ensure the good coupling between the channel and the gate).
- $g_3(x) : V_{DD} \leq V_{th}$ (for subthreshold-circuit-based applications, ultra-low power devices).

It is to note that the input vector can be extended to include other design parameters, such as metal contacts, parasite capacitances, channel doping profile, and insulator materials.

The overall objective function is obtained by a given weightage based on the "weighted sum approach method" as follows,

$$F(X) = w_1 S + w_2 \lambda \tag{5.50}$$

If high scaling capability and high commutation speed transistor, for analog applications, are the required factors by the device designer, subthreshold swing and the scaling length are equally important. Hence, $w_i (i = 1, 2)$ can be assigned equal values as 0.50. A lower value of scaling length and subthreshold swing are needed to design a transistor with high scaling capability and commutation speed values.

The MOGA parameters were varied, and the associated optimization error was recorded. For the optimized configuration, the overall objective function was 4.49×10^2, and almost 100% of the submitted cases were learned correctly.

Figure 5.15 shows the variation of overall objective function as a function of the generation number, where the minimum objective function can be reached for 10000 iterations. The steady decrease in the subthreshold and small-signal parameters of the best solution in each generation (until it reaches a best possible value) can be attributed to the selection procedure used. The final optimized JLGAA MOSFET parameters are summarized in Table 5.3.

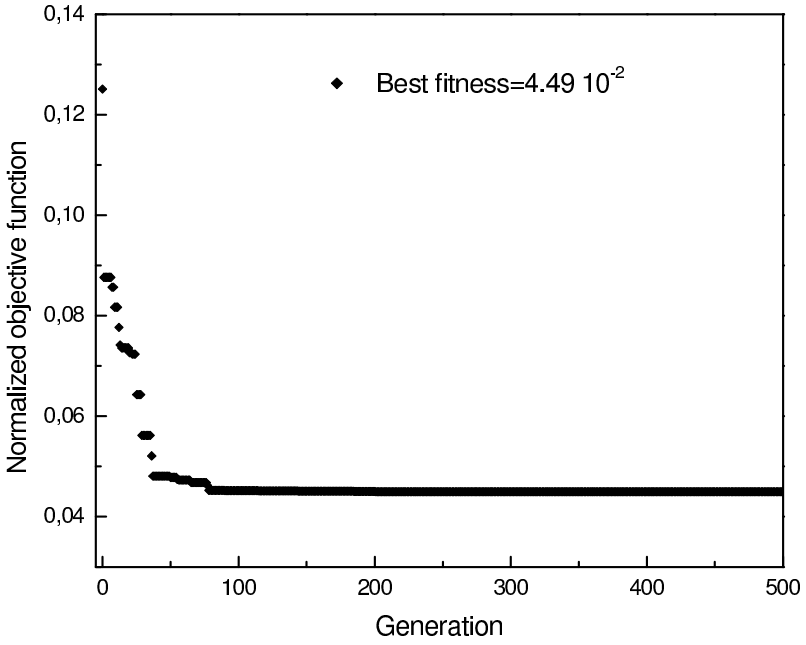


Figure 5.15: Variations of normalized overall objective function with generations

The developed MOGA-based approach can be used as the interface between device compact modeling and circuit simulators, such as Spice, Cadence and Synopsis, in order to optimize the electrical circuit performances.

Table 5.3: Optimized nanoscale JLGAA MOSFET design parameters.

Symbol	**Quantity**	**Random**	**Optimized**
V_{ds}	Drain source voltage	400 mV	0.10V
V_{gs}	Gate voltage	100 mV	0.25V
t_{si}	Silicon thickness	5 nm	3 nm
t_{ox}	thickness of the SiO_2	1 nm	1 nm
L	Channel length	50 nm	30nm
N_D	Channel doping	$1 \times 10^{18}\ cm^{-3}$	$9.8 \times 10^{18}\ cm^{-3}$
Objective functions:			
S	Swing factor	200 mV/dec	59.87 mV/dec
λ	Scaling length	1.90 nm	1.20 nm
g_m	Transconductance	11.50 μS	38.33 μS

5.4.6 Impact on nanoscale subthreshold circuit design

Subthreshold circuits operate with a supply voltage, V_{DD}, less than the threshold voltage of the MOSFET (V_{th}). Hence, the low applied biasing voltage leads to ultra-low power consumption. Since the subthreshold current is orders of magnitude lower than the drain saturation current and since the power supply is reduced, the subthreshold circuit dissipates ultra-low-power [22, 23]. In recent years, considerable research has been performed on subthreshold circuit design with various design methodologies and different technologies. In this context, this work will be focused on investigating of an ultra-low power voltage amplifier circuit, including our transistor optimization approach, in order to show the impact of the proposed MOGA-based approach on the design and optimization of the nanoscale subthreshold circuits. The voltage amplifier consists of a JLGAA MOSFET and a current generator, as shown in Figure 5.16.

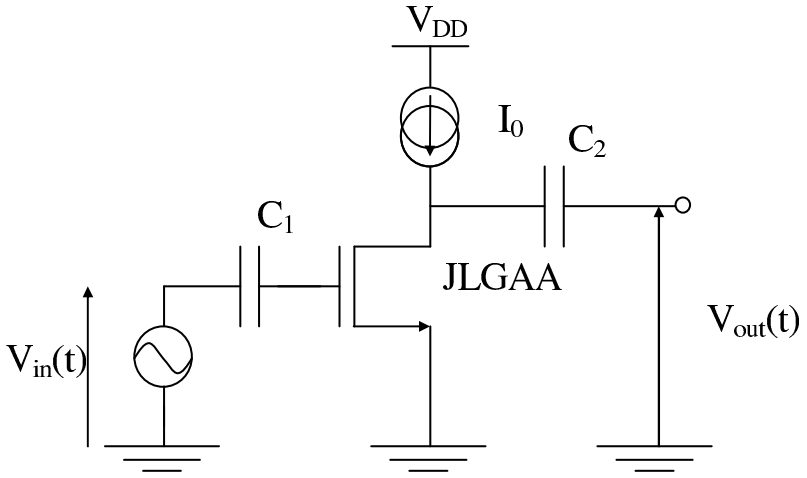


Figure 5.16: Nanoscale ultra-low power, JLGAA MOSFET, voltage amplifier

The current generator and supply voltage are set at $I_0 = 1A$ and $V_{DD} = 0.3V$, respectively, in order to satisfy the subthreshold working condition, and the gate voltage is set to give the adequate biasing condition of the transistor in the subthreshold region . The gain and cutoff frequency values of the nanoscale voltage amplifier with and without device optimization are shown in Table 5.4. The gain and cut-off frequency, for optimized

design, is about 11.45 and 127 GHz, respectively. However, the gain and cut-off frequency degraded to about 3.3 and 50 GHz, respectively, for device without optimization. The gain and cut-off frequency are given by $G_v = |g_m/g_{ds}|$ and $f_T = g_m/(2\pi C_{oxq})$, respectively.

Table 5.4: Optimized ultra-low power voltage amplifier design parameters

Symbol	**Quantity**	**Optimized design**	**Design without optimization**
V_{ds}	Drain source voltage	0.1V	0.4V
V_g	Gate voltage	0.2V	0.1V
t_{si}	Silicon thickness	3 nm	5 nm
t_{ox}	thickness of the SiO_2	1 nm	1 nm
L	Channel length	30nm	50 nm
ND	Channel doping	$9.8 \times 10^{18}\ cm^{-3}$	$10^{18}\ cm^{-3}$
$Gain$	Gain voltage	11.45 V/V	3.30 V/V
f_T	Cut-off frequency	127GHz	50GHz

From Table 5.4, it is observed that an enhancement of circuit electrical performance, gain, and cutoff frequency, can be obtained by using the proposed approach as a design tool to optimize the nanoscale ultra-low power circuits.

5.5 Sammary

In this chapter, we have presented new mathematical models for short channel MuGFETs devices. The models are based on a surface potential formalism developed for those devices using adequate boundary conditions, from which we derived simple expressions for the subthreshold region in terms of the subthreshold swing and subthreshold current in order to investigate the scalability limits of these devices.

The developed models are dedicated to analyze the subthreshold behaviour of the new proposed structures where good agreement is found between the new developed models and the 2-D numerical simulations. The elaborated analysis in this chapter is mainly relied on mathematical modeling and assumption, taking the advantage of the low computation

complexity of the calculation.

Moreover, a MOGAs-based approach is proposed to improve the subthreshold behaviour of the proposed devices for digital and/or analog nanoscale CMOS-based applications. The proposed approach has successfully searched the best possible transistor performance and the input design parameters that can yield those specific performances in a specific working regime of the transistor for such circuit application. The efficiency of the proposed approach may provide an easy and fast way to investigate and design MuGFETs comprehensively.

The text of Chapter 5, in part, is a reprint of the material as it appears in "A two-dimensional semi-analytical analysis of the subthreshold swing behavior including free carriers and interfacial traps effects for nanoscale double-gate MOSFETs" by F. Djeffal, T. Bendib, and M. A. Abdi, Microelectronics Journal, Elsevier, 2011. The dissertation author was the primary investigator and author of this paper.

The text of Chapter 5, in part, is a reprint of the material as it appears in "Subthreshold behavior optimization of nanoscale graded channel gate stack double gate (GCGSDG) MOSFET using multi-objective genetic algorithms" by T. Bendib, F. Djeffal, and D. Arar, Journal of computational electronics, Springer, 2011. The dissertation author was the primary investigator and author of this paper.

The text of Chapter 5, in part, is a reprint of the material as it appears in "An optimized junctionless GAA MOSFET design based on multiobjective computation for high-performance ultra-low power devices" by T. Bendib, F. Djeffal, and M. Meguellati, Journal of Semiconductors, IOP Publishing, 2014. The dissertation author was the primary investigator and author of this paper.

Chapter 6

Conclusions and Future Research

Contents

6.1 Contributions and conclusion

As the technology scales, interest in alternative devices are growing to replace the conventional MOSFETs. Multiple-gate MOSFETs are competing with the conventional MOSFETs presently and it is expected that DG and GAA MOSFETs will be the future mainstream. Due to the strong dependence of circuit behaviour on the device characteristics in the alternative devices, it is necessary for circuit designers to understand the physics inside new design technology thoroughly. Based on the understanding, circuit designers should maximize the advantages of each device and control the undesirable effects. This dissertation presents a comprehensive study on the design and modeling of multi-gate MOSFETs, for nanoscale CMOS-based applications.

First of all, in chapter 3, a new approach for modeling semiconductor devices, nanoscale Double Gate DG MOSFETs, by use of the Gradual Channel approximation (GC) approach and soft computing techniques GA and FL have been presented. The proposed approach combines the universal optimization with fitting capability of soft computing approaches, GA and FL, and the cost-effective optimization concept of quantum correction, to achieve reliable, accurate and simple compact models for nanoelectronics circuit simulations. Our compact models give good predictions of the quantum capacitance, threshold voltage shift, quantum inversion charge density, electron mobility and drain current. These models have been verified with 2D self-consistent results from numerical calculations of the coupled Poisson-Schrödinger equations.

In chapter 4, a new approach for electrical performances optimization of semiconductor devices, nanoscale Double Gate (DG) MOSFETs, using Multi-Objective Genetic Algorithms (MOGAs) has been presented. The proposed optimization approach has been used as a design tool to study the nanoscale circuit electrical behavior in order to achieve reliable and optimized design of DG MOSFETs for nanoelectronics analog and digital circuits simulations. The dimensional and electrical parameters of the DG MOSFET such as threshold voltage roll-off, OFF-current, drain induced barrier lowering (DIBL), subthreshold swing (S), output conductance and transconductance have been ascertained

and compact analytical expressions including quantum effects and the channel length modulation effect developed in chapter 3 have been included in the computation. The developed compact models are used to formulate the different objective functions, which are the pre-requisite of multi-objective genetic algorithms optimization. The optimized design has been incorporated into single transistor amplifier to study and show the impact of our approach on the nanoscale CMOS-based circuits design where an enhancement in electrical performances of single transistor amplifier, the gain and the cut-off frequency has been observed.

In chapter 5, new MuFETs structures GCGSDG and JLGAA MOSFETs have been proposed to investigate their subthreshold behavior for nanoscale CMOS digital and analog applications. By focusing on the surface potential formalism, a new subthreshold swing models for short-channel MuFETs MOSFETs have been developed. The analytical analysis has been used to calculate the subthreshold swing and compare the performance of the investigated designs with conventional structures DG and GAA MOSFET, where the comparison of device architectures shows that the proposed MuFETs structures exhibit a superior performance with respect to the conventional ones in terms of fabrication process and electrical behavior in subthreshold domain. The core models agree with 2-D numerical simulations very well without using any fitting parameters. It demonstrates the inherent physical predictivity and scalability of the developed models. In this chapter, the work is extended to show the impact of the investigated devices on nanoscale CMOS application. Multi-objective genetic algorithms-based approach has been proposed where the overall objective function is formulated, using the developed models, by means of weighted sum approach to search the optimal electrical and dimensional device parameters. Performance assessment of the optimized designs of GCGSDG and JLGAA MOSFETs were projected for digital and ULP application respectively where better scaling capability and high electrical performances of these devices have been recorded.

In summary, the main contribution of this thesis are as follow:

- Understanding the unique device physics in the multi-gate MOSFETs comprehen-

sively.

- Proposing new Modeling methodologies/approaches to incorporate these unique multigate physics in their models.

- Proposing an accurate QM correction for DG MOSFET to simultaneously capture both threshold voltage V_{th} shift and gate capacitance C_{gs} degradation for the first time.

- Developing an accurate drain current model assuming the gradual channel approximation of nanoscale DG MOSFET including SCEs, for a very wide interval of geometrical and physical parameters.

- Proposing optimal DG MOSFET device structure for nanoscale CMOS digital and analog application to improve structure design in advanced transistor for such operation.

- Several important concept design of multi-gate based circuits are addressed to provide straightforward way to assess the scaling limit of different MuGFETs designs.

- Developing new subthreshold models by focusing on the surface potential formalism that capture V_{th} roll-off, DIBL, OFF-current and subthreshold swing degradation to investigate the subthreshold behavior for nanoscale CMOS digital and analog applications.

6.2 Suggestions for future work

The following research tasks are suggested as future work regarding advanced multi-gate devices:

- One of the priorities beyond this work would be the inclusion of more models for multi-gate MOSFETs. Examples of these models include but are not restricted to

1) gate tunneling current model, 2) noise model, 3) source/drain parasitic resistance model, 4) overlap capacitance model and 5) non-quasi-static model.

- For a high-K dielectric, the gate to channel tunneling current would still be considered as a major leakage current. Modeling and analysis of the gate to channel tunneling current are suggested for UTB transistors with/or without high-K dielectrics.

- Mobility degradation by phonon and Coulomb scattering in UTB should be addressed. In designing ultimately scaled ($Leff < 10nm$) DG devices, the Si film-thickness must be extremely reduced ($t_{si} \approx Leff/3$) to control SCEs. For such an extremely thin film ($< 5nm$) carrier mobility can be significantly degraded by enhanced phonon and Coulomb scattering, the latter being due to trapped charge in surface state.

- The developed DC models in this thesis are only applicable to static bias conditions. charge and capacitance model can be derived based on the present work in order to carry out the small signal AC and large signal transient simulation. Finally an algorithm to extract the model parameters should be developed to apply the model to circuit simulation.

- Although this work only discusses the multi-gate silicon MOSFET structure, the corrugated substrate can be used as a platform to explore advanced devices using Ge and III-V channel materials to improve the performance and scalability of other transistor designs.

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